Automatic Diagram Creation for Design and Testbenches

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SYSTEMS INITIATIVE™

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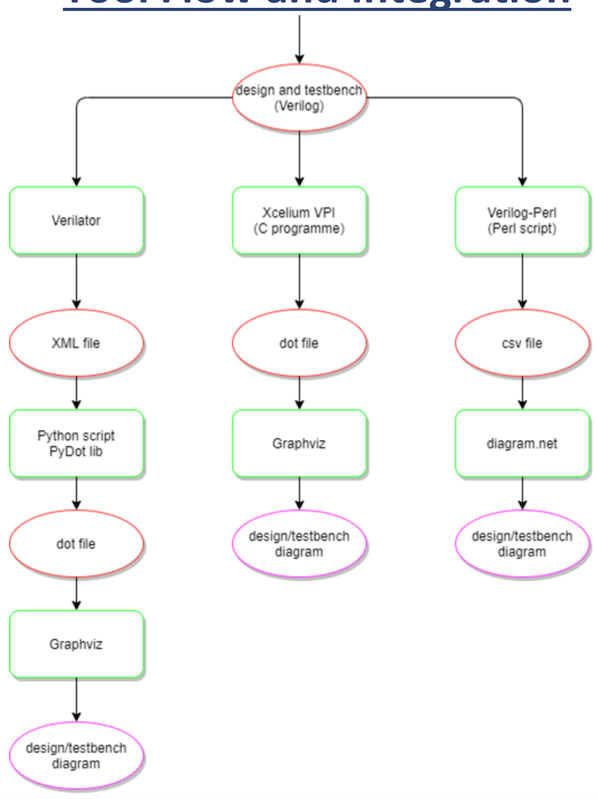
Automatic Diagram Creation for Design and Testbenches

- Open source tools
- Diagrams for specification and training purposes
- Integrated into design and testbench
- Diagrams regenerated throughout the design cycle
- Diagram types:
  - Design and testbench hierarchical diagrams
  - Clock and reset tree diagrams
  - Design connectivity diagrams
- No effective commercial tools available

Tool Flow and Integration



Verilog Procedural Interface (VPI) & Cadence Xcelium

- VPI[1] integrated into Cadence Xcelium simulator
- VPI[1] functions used:
  - vpi_scan() [2]
  - vpi_iterate() [2]
- Programme can be integrated into existing xrun script

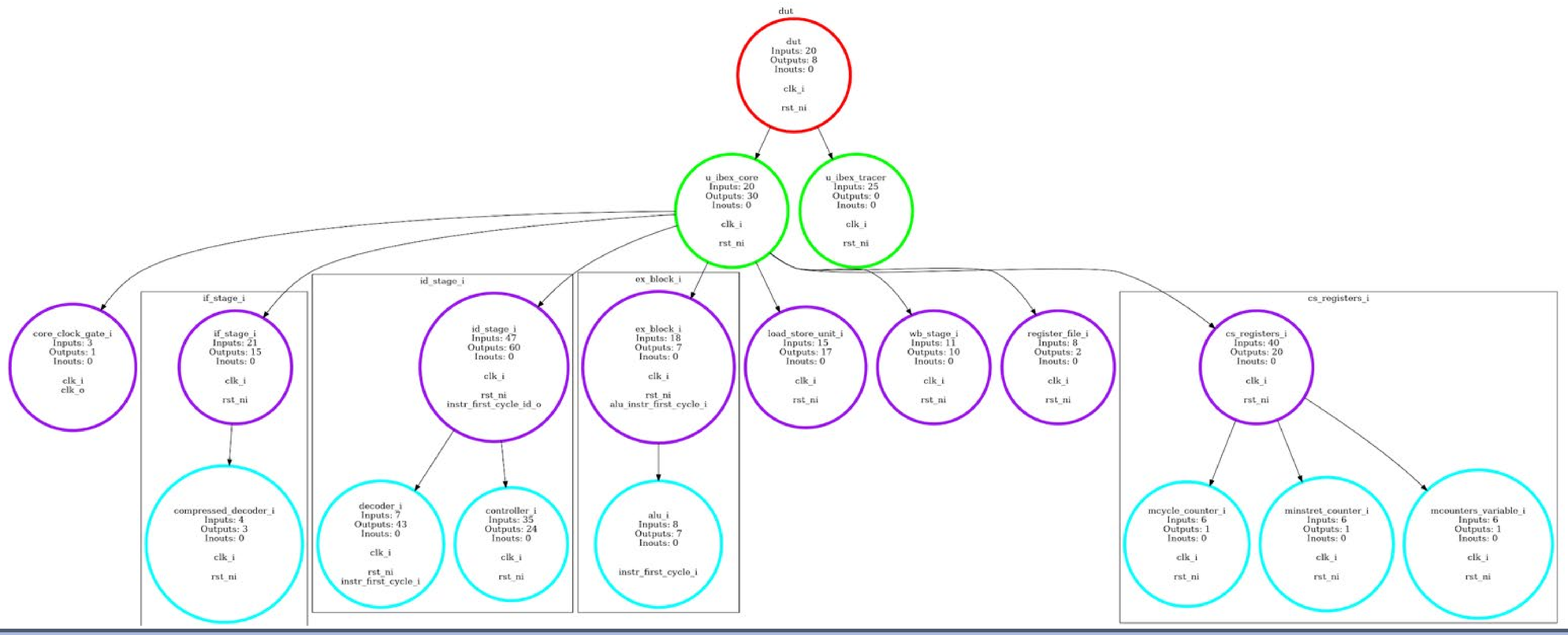
```
/* If the module has sub-modules, we have to print the sub-module details and execute walk_mod_hierarchy()
on each */
 if (ModuleI) {
  while ((SubModuleH = vpi_scan(ModuleI))) {
   _num_scope = 0;

   // NOTE: This includes tasks.
   objI = vpi_iterate(vpiInternalScope, SubModuleH);
   if (objI) {
    while (objH = vpi_scan(objI)) {
     vpi_mcd_printf( debug_file, "%s Internal Scope - %s\n",vpi_get_str(vpiName,SubModuleH),
vpi_get_str(vpiName,objH));
      _num_scope++;
    }
   }
```

Diagram Creation

- Graphviz[3]
  - Command line integration
  - Very fast generation
  - Automatic layout
  - Design and layout options
  - Diagrams are not editable
  - Dot layout
    - Design and testbench hierarchical diagrams
    - Clock and reset tree diagrams
  - Circo, Twopi, SFDP layouts
    - Design connectivity diagrams
- Diagrams.net[4]
  - Import in CSV or XML
  - Editable diagrams
  - Not automated

lowRISC Ibex Block Diagram (generated using our VPI script and Graphviz)



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References

[1] IEEE SystemVerilog_1800-2017 - LRM (Chapters 36-38 VPI)
[2] Cadence VPI examples hier_walker, count_args, dtran for tool version: XCELIUM_19.09.007 (tools.lnx86/inca/examples/vpi)
[3] Graphviz - https://www.graphviz.org/
[4] Diagrams.net diagram capture tool - https://www.diagrams.net