Automatic Diagram Creation for Design and Testbenches

- Open source tools
- Diagrams for specification and training purposes
- Integrated into design and testbench
- Diagrams regenerated throughout the design cycle
- Diagram types:
  - Design and testbench hierarchical diagrams
  - Clock and reset tree diagrams
  - Design connectivity diagrams
- No effective commercial tools available

Tool Flow and Integration

Verilog Procedural Interface (VPI) & Cadence Xcelium

- VPI[1] integrated into Cadence Xcelium simulator
- VPI[1] functions used:
  - vpi_scan[] [2]
  - vpi_iterate[] [2]
- Programme can be integrated into existing xrun script

```c
// If the module has sub-modules, we have to print the sub-module details and execute walk_mod_hierarchal() via each:
if (ModuleH) {
    while ((subModuleH = vpi_scan submodule)) {
        if (ModuleH) {
            while ((objH = vpi_scan obj)) {
                vpi_module_print_debug_file, "vs internal scope. vpi get str(vpi name sub module H), vpi get str(vpi name obj H), "
                num scope++;
            }
        }
    }
}
```

Diagram Creation

- Graphviz[3]
  - Command line integration
  - Very fast generation
  - Automatic layout
  - Design and layout options
  - Diagrams are not editable
  - Dot layout
    - Design and testbench hierarchical diagrams
    - Clock and reset tree diagrams
    - Circos, Twopi, SDFP layouts
    - Design connectivity diagrams
- Diagrams.net[4]
  - Import in CSV or XML
  - Editable diagrams
  - Not automated

lowRISC Ibex Block Diagram (generated using our VPI script and Graphviz)

References