Automated RTL Update for Abutted Design

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Challenge

- Key Factors of SOC(System On Chips) Design
  - Performance
  - Power
  - Area

- Area Reduction: Abutted Design
  - Chip area reduction by eliminating top level routing

- RTL update for abutted design
  - Divide-and-conquer integration to a lot of functional blocks for full chip RTL generation due to limitation of tool capacity or computing resources
  - Multiple functional blocks for abutted design should be updated due to divide-and-conquer integration
  - The updates should be performed without human error simultaneously.
  - Automation of RTL update for abutted design is inevitable.

Metadata Based Integration

- Metadata for SOC Design
  - IP-XACT (IEEE-1685 as IEEE Standard)

- IP-XACT base integration
  - IP Packaging using IP-XACT
  - Connect IPs with interface and port in IP-XACT
  - Integrate system level IPs with automation flow
  - Create top design by connecting blocks

Abutted Design

- Abutted Design
  - Area reduction by eliminating top channel routing

RTL Update Automation Flow

- RTL Update Automation Flow
  - Generate Abutted Information to metadata
  - Generate connection script for RTL update from the abutted information using automation solutions
    - Automation solutions are implemented with Python or JavaScript
  - Execute the scripts at functional blocks and top design
  - Generate updated RTL for functional blocks and top design

Pilot Result

- Pilot Result
  - Number of connection is increased due to abutted design.
  - The huge connections are automatically connected in a short time.
  - Function verification is performed at RTL level without abutted information due to no functional change due to abutted design.

<table>
<thead>
<tr>
<th>Port Connection</th>
<th>Change Rate</th>
<th>Update Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before</td>
<td>After</td>
<td>(Time)</td>
</tr>
<tr>
<td>(Secs)</td>
<td>(Secs)</td>
<td>(Secs)</td>
</tr>
<tr>
<td>Text mode control</td>
<td>7257</td>
<td>4944</td>
</tr>
</tbody>
</table>
| Data communication | 1024(1)     | 564.4(1)    | ▲ 1.2x  | 362s(1)
| Test signal from pad | 181         | 1248        | ▲ 0.6x  | 377s |

(1) Data channel is connected by bus interface(I2C)

Summary

- Conclusion
  - To reduce area of SOC design, abutted design is required.
  - For abutted design, a large amount of RTL code modification is required.
  - It is difficult to apply the abutted design as a manual method.
  - To prevent human error and reduce development time, automated RTL update solution is proposed and developed.
  - RTL changes could be made without any human error in a short time due to the proposed solution.

Enable automated RTL update for abutted design without manual process using metadata based automation flow