2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Automated Performance Verification to Maximize your ARMv8 pulling power

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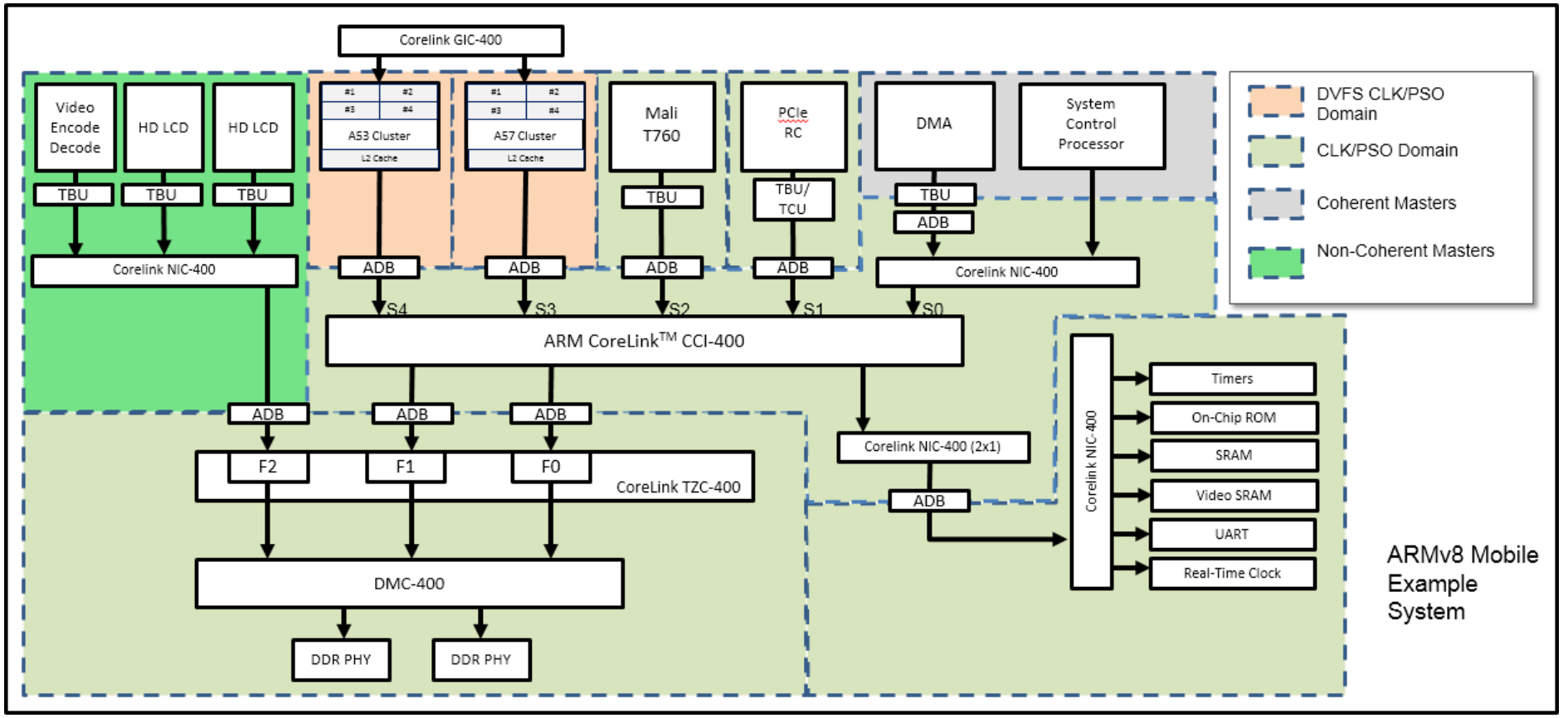
cadence®

ARM

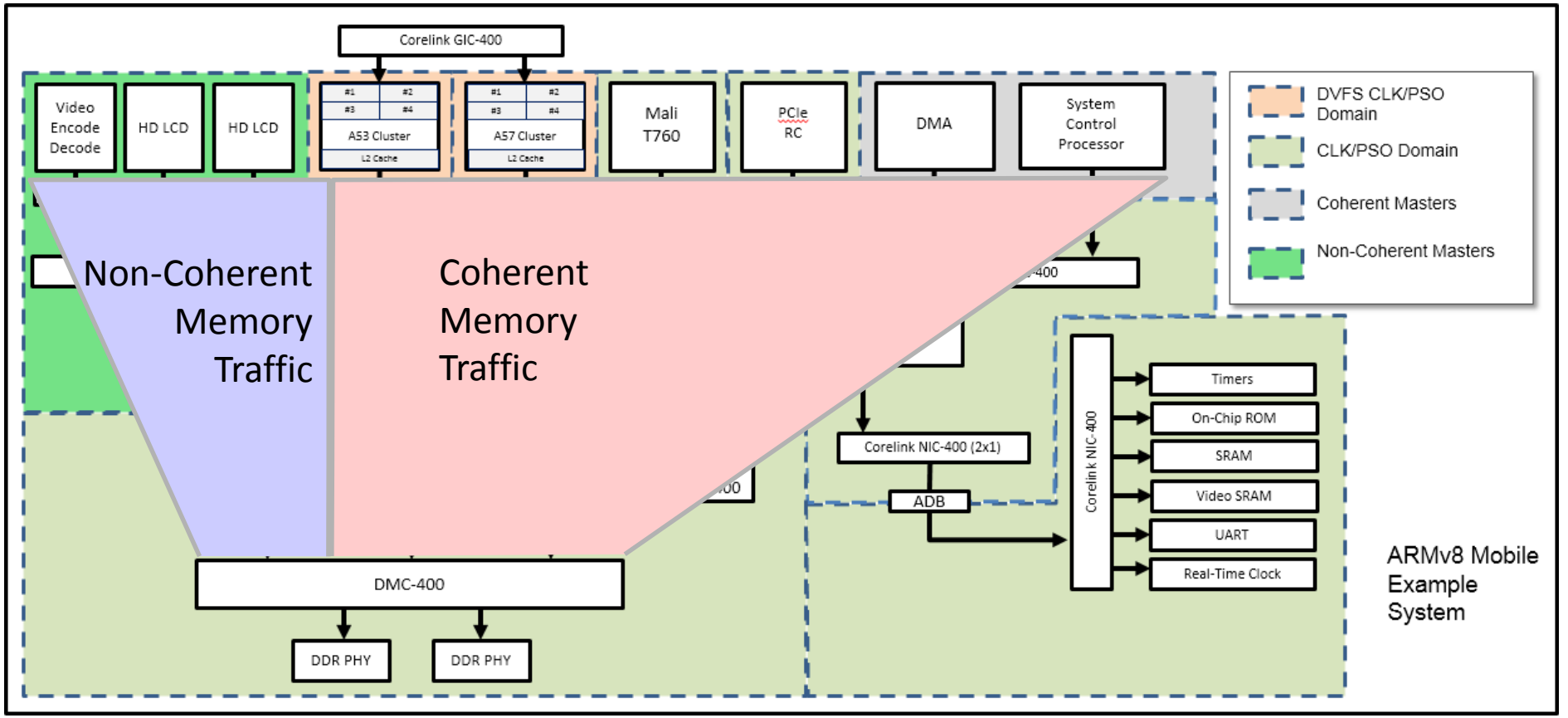
Agenda

- Introduction to ARM v8 CPU Subsystem
  - System Coherency
  - DDR Bandwidth and Latency Demands
  - Example Performance Use-case
- Building a testbench early performance exploration
  - Testbench Automation
  - Cadence Interconnect Workbench
  - Debugging Failing Use-cases
  - Visualizing System Back-pressure and DDR Events
- Summary

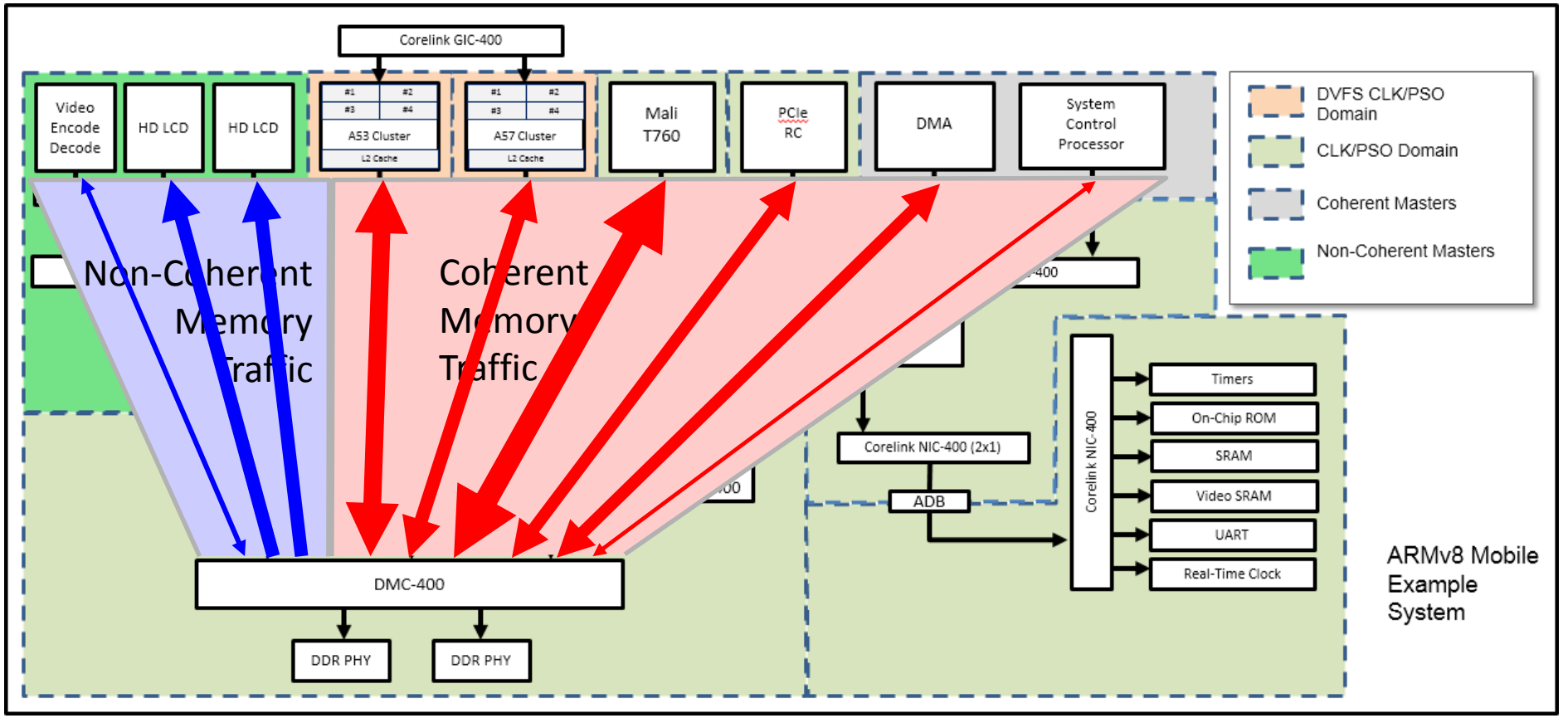
ARM v8 Compute Subsystem



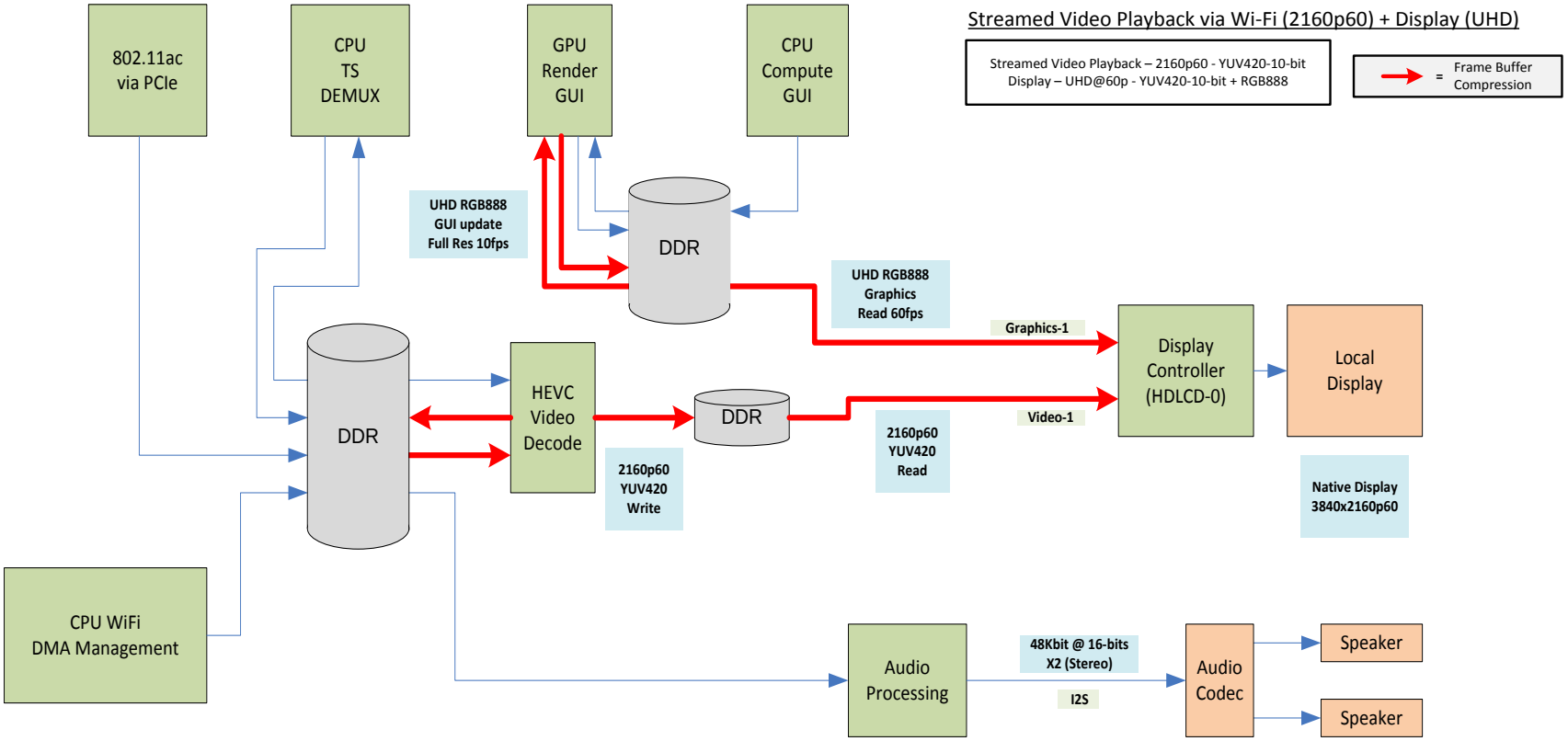
System Coherency



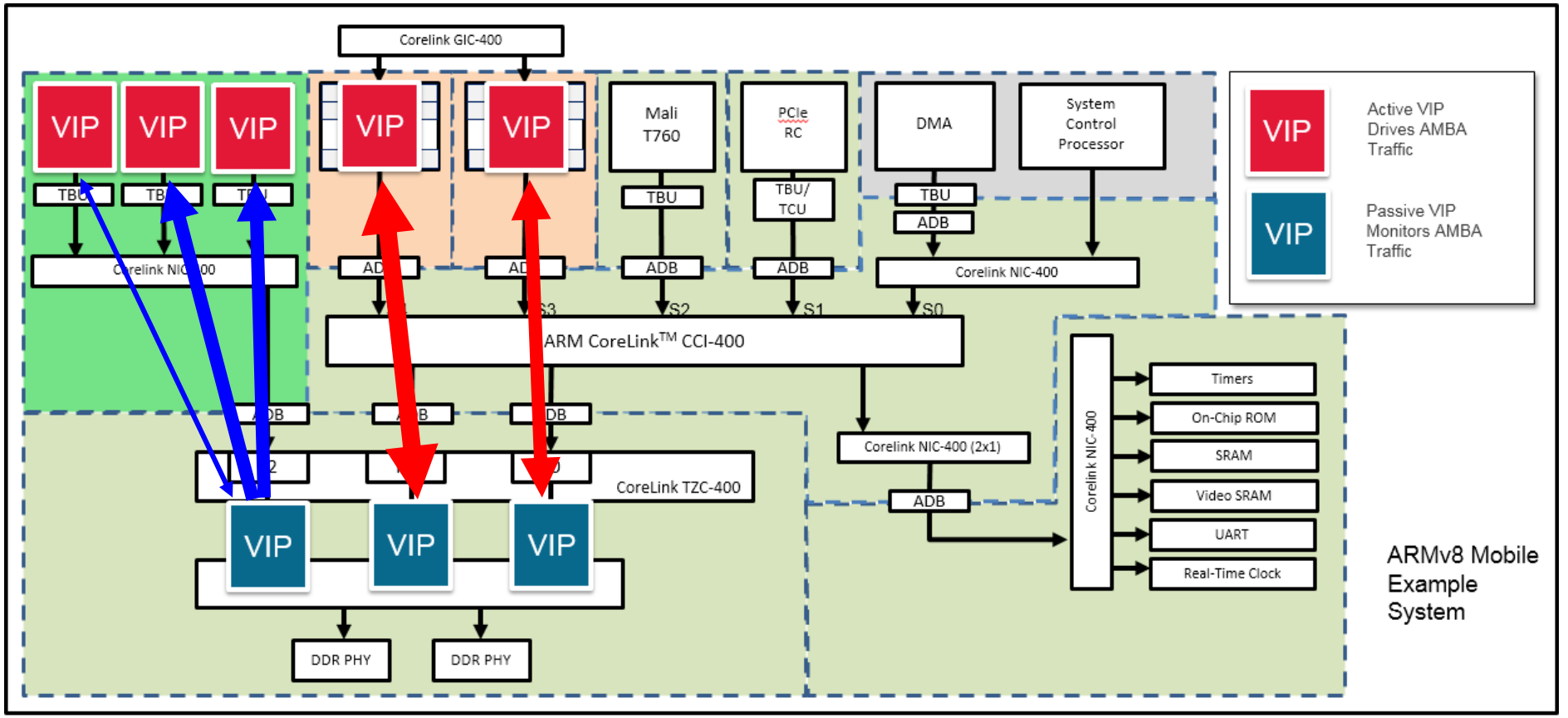
DDR Bandwidth and latency Demands



Example Performance Use-Case: Streamed Video Playback



Testbench for early analysis



Testbench Automation

RDVE FORMAT IWB 1.4

Interconnect Workbench
Master Spreadsheet
v1.4 (3rd February 2014)

Show / Hide Advanced Interface Parameters

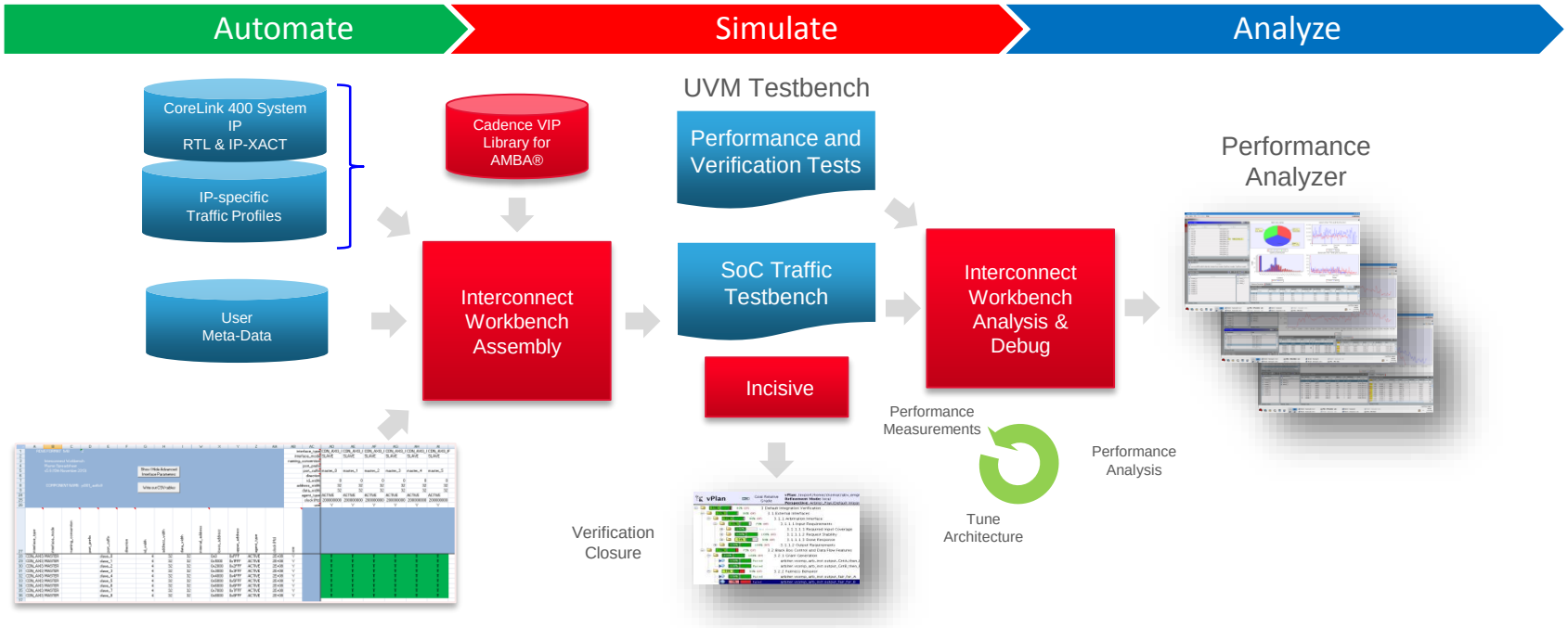
COMPONENT NAME:

Write out CSV tables

interface_type	CDN_AXI4_S1_IF	CDN_ACE_LITE_S1_IF	CDN_AXI4_S1_IF	CDN_AXI4_S1_IF	CDN_AXI4_S1_IF
interface_mode	SLAVE	SLAVE	SLAVE	SLAVE	SLAVE
naming_convention	UPPERCASE	UPPERCASE	UPPERCASE	UPPERCASE	UPPERCASE
port_prefix					
port_suffix	_pcie	_gpu	_hdlcd0	_hdlcd1	_video
direction					
id_width	8	8	8	8	8
address_width	44	44	44	44	49
data_width	128	128	64	64	128
ip_name	pcie	gpu	hdlcd0	hdlcd1	video
agent_type	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
clock (Hz)					
use	Y	Y	Y	Y	Y

interface_type	interface_mode	naming_convention	port_suffix	id_width	address_width	data_width	ip_name	lower_address	upper_address	agent_type	clock (Hz)	use					
CDN_ACE_LITE_S1_IF	MASTER	UPPERCASE	_0	13	40	128	dmc0	0x80000000	0xFFFFFFFF	PASSIVE		Y		stripe_4k_odd stripe_4k_even	stripe_4k_odd stripe_4k_even	F F	F F	F F
CDN_ACE_LITE_S1_IF	MASTER	UPPERCASE	_1	13	40	128	dmc1	0x80000000	0xFFFFFFFF	PASSIVE		Y						
CDN_ACE_LITE_S1_IF	MASTER	UPPERCASE	_2	13	40	128	dmc2	0x80000000	0xFFFFFFFF	PASSIVE		Y		F	F	T	T	T
CDN_ACE_LITE_S1_IF	MASTER	UPPERCASE	_3	13	40	128	dmc3	0x80000000	0xFFFFFFFF	PASSIVE		N		F	F	F	F	F

Cadence Interconnect Workbench

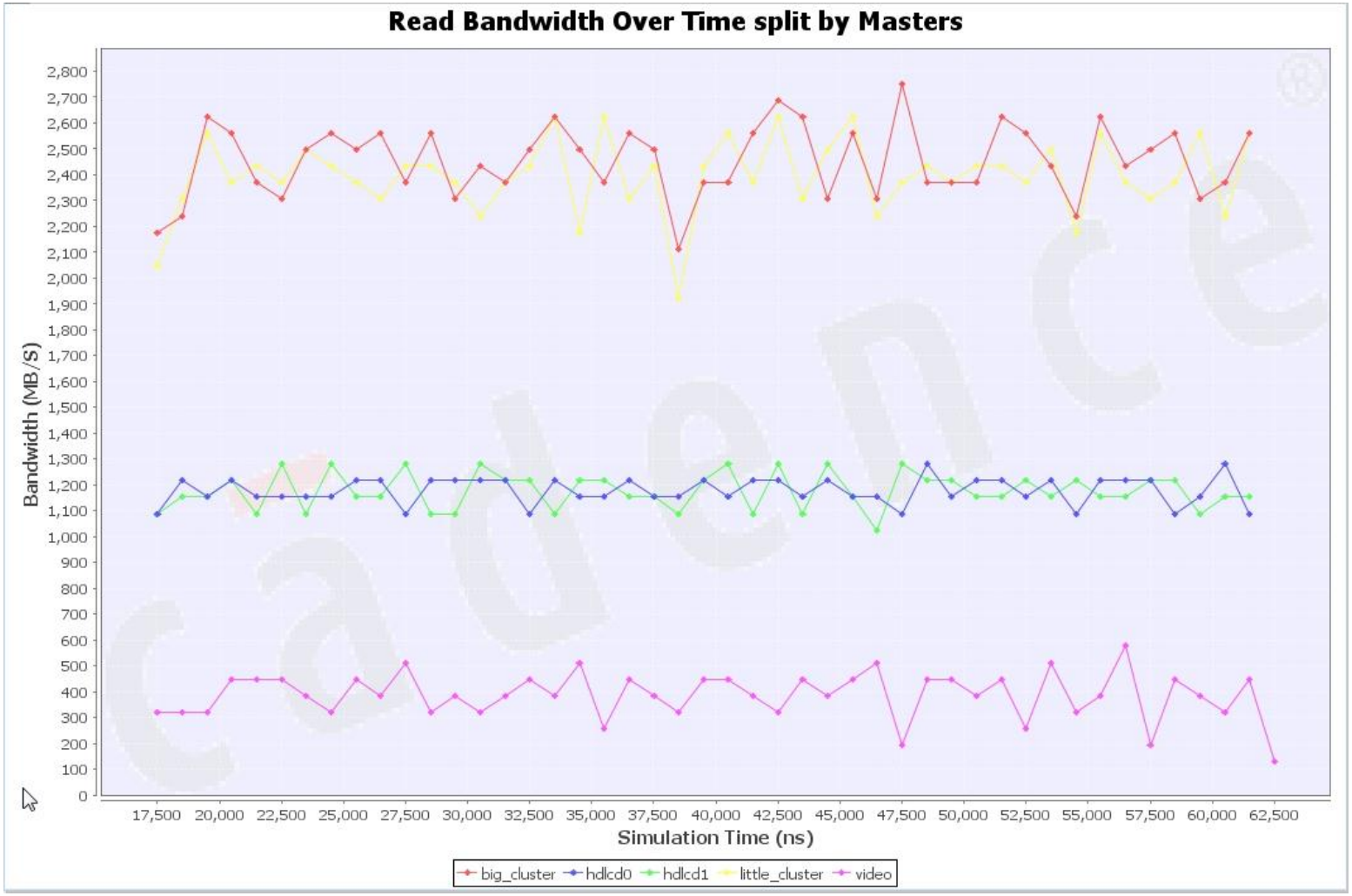


For Interconnect IP Integration
- Performance of use case traffic loads
- Verify configuration functionality

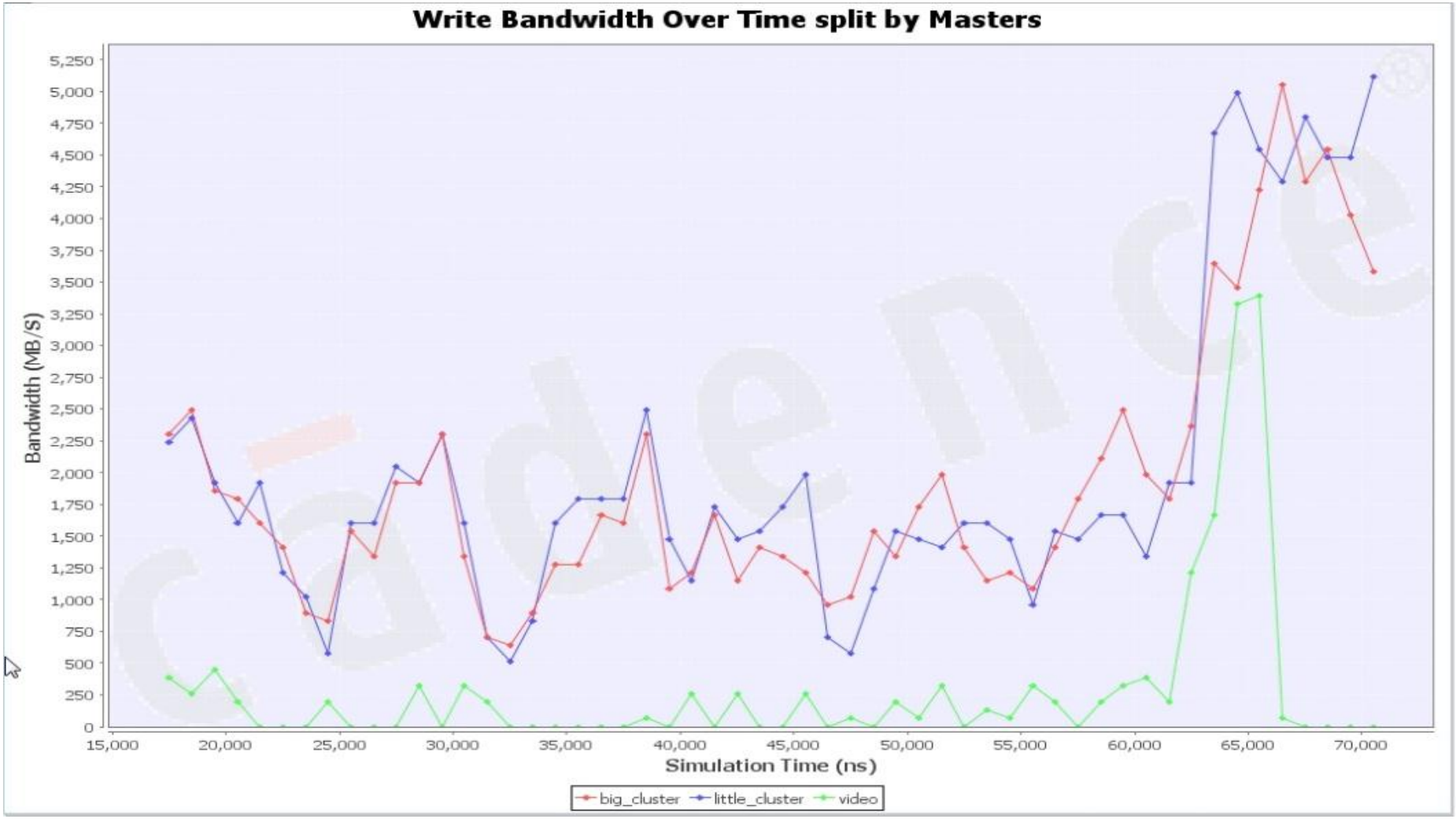
For SoC Integration
- Validate performance in context of IPs

Benefits
- Shorten performance tuning and analysis iteration loop from **days** to **hours**
- Reduce testbench development time from **weeks** to **hours**

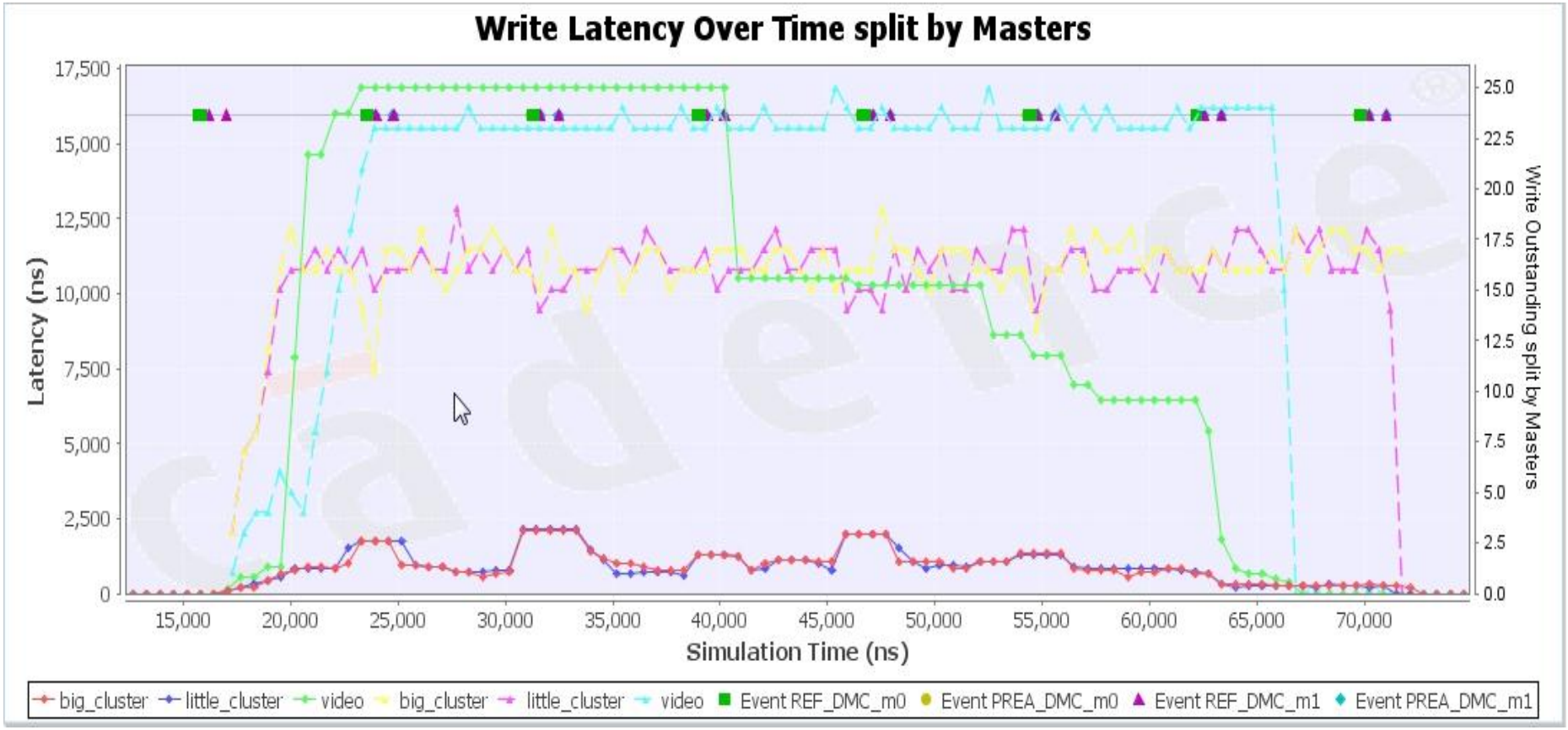
Modelled Use-case results



Debugging Failing Use-cases



Visualizing System back-Pressure and DDR Events



Summary

- CPU Subsystems are becoming more complex
- Sophisticated System IP provides powerful capabilities and configurability to ensure system performance can be achieved
- Analysis tools and automation are essential productivity aids for early exploration of system performance on the RTL.