Abstract

The decision criteria: Area and Power as measured by Cadence

Schedule: 3 months to complete the evaluation.

Questions to be answered:
- Can we use a SystemC model as basis for developing designs for DSP fabric?
- How effective is High Level Synthesis for this type of design activity?
- What is the cost of programmability?
- What are the best accelerator designs for one application (trellis decoder).
- Which software tools were unable to effectively use more than 2 accelerators?
- The overhead for using programmable accelerators was determined to be about 5x vs. a hard coded RTL implementation for one application (trellis decoder).
- The software tools were unable to effectively use more than 2 accelerators. Our automated flow could only find on the average 2 parallel instructions per basic block.
- 1 memory port per operand was sufficient for all of the applications we tested.
- The accumulator bus (40 bits) came with very low overhead and enabled ganging of accelerators.
- Advanced autonomous DSP configurations were relatively easy to define and evaluate using this design flow.
- For example the autonomous fir instruction, which enables instruction to stream data from memory without incrementing pc and gets coefficients from instruction memory, was easily expressed in SystemC and evaluated.
- Several of these were included in the final implementation since they effectively reduced latency and power for our target application.

Objectives

- Design a DSP fabric to achieve power reduction with increased throughput as shown below.

- Schedule: 3 months to complete the evaluation.

- Architectural parameters:
  - Number of parallel execution units
  - Propagation of unsaturated results between accelerators
  - Number of memory ports
  - Cost of advanced DSP instructions for FIR, Sum of absolute differences (SAD), Butterfly combinations.

- The decision criteria: Area and Power as measured by Cadence RTL design tools.

- Start from C code version of applications then measure:
  - Number Accelerators needed and their frequency
  - Instruction parallelism by basic block
  - Memory bandwidth (number of memory ports)

- Goals for programmability for one of our applications (run a case through to ASIC implementation).

Materials and Methods

SystemC model with the following variable parameters:

- Number memory ports
- Special DSP functions
- Number of accelerators.

- From SystemC simulations:
  - Function validation
  - RTL verification
  - HW/SW partitioning

- LLVM based compiler flow with optimization passes:
  - Balancer, SDC
  - Scheduling, matcher, instruction frequency driven packing using integer linear programming and assembly.

Results

<table>
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<tr>
<th>Software</th>
<th>Accelerators</th>
<th>Frequency</th>
<th>Instruction count</th>
<th>Instruction count</th>
<th>Latency (2.4 port)</th>
<th>Parasitism</th>
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<td>DC</td>
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<td>20</td>
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<td>9,9</td>
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<td>12</td>
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References


Acknowledgements

We thank the anonymous referees for their constructive feedback and acknowledge the helpful discussions with Edward Gazarian.

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