**INTRODUCTION**

TriCore™:
- Popular processor core in automotive MCUs
- Combines RISC, MCU and DSP instructions

AURIX™:
- 5th generation TriCore™
- Several cores in lockstep for increased reliability
- Entering market in 2014 and 2015

**OBJECTIVES**

- A fast and open virtual platform targeting Infineon’s AURIX™
  processor family using
  - TriCore™-based QEMU for fast CPU emulation
  - SystemC and TLM-2.0 for device emulation
  - Transaction Level Emulator (TLMu)[1] to interface QEMU and SystemC/TLM-2.0

**MILESTONES**

- Implement TriCore™ QEMU emulation and verify its correctness
- Extend TLMu to support the TriCore™ architecture (interrupt, ...)
- Create a SystemC testbench
- Run a complete software stack on the platform

**APPROACH**

- Build main line QEMU with TriCore™-based binary translator as a shared library loaded by SystemC
- Memory device in QEMU maps the whole address space to callbacks mapped to SystemC write/read accesses
- SystemC models send interrupts to TLMu memory device, which interrupts the TriCore™ CPU model

**RESULTS**

Comparison with TSIM

- Functional correctness through
  - C programs
  - randomly generated and selected asm programs
- Speed comparison:
  - Fibonacci program (C)
  - Add program (C)
  - Up to 880x faster than TSIM for considerably long-running programs

**CONCLUSIONS**

- TriCore™-support added to official QEMU repository [2]
- Functional correctness of TriCore™ architecture in QEMU validated
- Up to 880x faster compared to TSIM
- TLMu supports integration of TriCore™ QEMU into SystemC/TLM-2.0 platform model

All 16 bit TriCore™ instructions now available at [http://git.qemu.org](http://git.qemu.org)

**OUTLOOK**

- Add the remaining 200 of 700 TriCore™ instructions to QEMU
- Update TLMu to latest version of QEMU
- Test platform with Infineon’s AURIX™ test software

**REFERENCES**


---

Bastian Koppelmann, Bernd Messidat, Markus Becker, Christoph Kuznik
{kbastian, messi, beckerm, christoph.kuznik}@c-lab.de
C-LAB, University of Paderborn

Wolfgang Müller, Christoph Scheytt
{wmueller, cscheytt}@hni.uni-paderborn.de
HNI, University of Paderborn