

An Innovative Methodology for Verifying Mixed-Signal Components

Fabian Delguste,
Adiel Khan, Abhisek Verma
Synopsys
Fabian.Delguste@synopsys.com
Adiel@synopsys.com
Abhiv@synopsys.com

Graeme Nunn
Calvatec
Graeme.Nunn@calvatec.com

1. ABSTRACT

The traditional verification approach used in the analog world still lacks some key aspects that have been efficiently deployed to digital verification for years.

SPICE-based analog verification environments are usually hard to reuse at System on Chip (SoC) level, difficult to control and do barely bring the required simulation performances.

By leveraging from the well-proven VMM and UVM methodologies, the main scope of AMS-TESTBENCH is to provide analog designers and verification engineers with a methodology that allows them to,

- Introduce analog verification planning
- Introduce constraint-random verification for driving analog nodes
- Model analog stimulus as shaped transaction-based bus functional models
- Integrate reference models with various abstraction level
- Sample analog nodes to monitor incoming traffic
- Introduce assertions on analog nodes
- Introduce analog code coverage and functional coverage
- Introduce regression management

In conjunction to elaborating on above features, this paper describes a scalable and reusable methodology for verifying analog IPs. Reuse is made possible by correct modeling of verification models that can be stitched into the SoC.

These models can be implemented with HDL or Verilog-AMS. This depends upon the required accuracy.

This paper is a case study that explains the various aspects of this methodology that can be applied to VMM/ UVM, from verification planning to testbench implementation and coverage collection.

2. INTRODUCTION

New generation System on Chip invariably increases the analog IPs included. For example, it is becoming usual to see multiple standard interfaces such as USB, Ethernet, SATA, DDR, etc on a single chip.

Additionally, there is a need for more analog IPs to handle multiple power domains, clock generation (PLL) and conversion (ADC, DAC).

As the need to include more embedded analog IPs increases, it is becoming challenging to architect a verification environment that can accommodate digital and analog verification.

AMS-TESTBENCH technology provides a solution that helps to fill this gap. As shown in Figure1, AMS-TESTBENCH allows complementing a traditional digital verification environment with a few components that can drive some analog IPs such as ADCs or Clock generation.

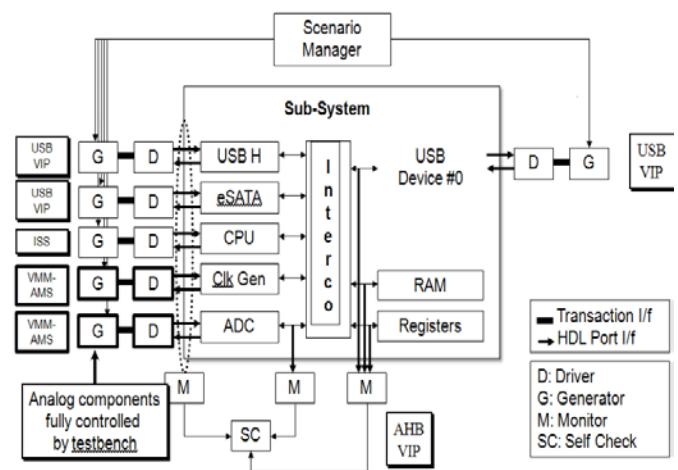


Figure 1: Verifying Digital and Analog Blocks

With this architecture, it is possible to decide when to start injecting analog traffic, when to stop and when to sample the output results.

For example, you can consider a typical scenario such as:

- Initialize and configure the subsystem registers
- Wait for the clock generation to stabilize
- Start injecting analog ramps to the ADC
- Read the internal converted digital output whenever the SoC receives an interrupt.

Certainly, other VMM or UVM base classes and applications can also be used by this architecture, such as RAL to initiate register traffic and VMM-LP to model the low-power domains.

Based on the desired accuracy, ADC can either be a transistor-level SPICE netlist or a reference model. The latter provides faster simulation performance but with less accuracy. This reference model can either be written in Verilog-AMS or SystemVerilog.

As shown in Figure2, AMS-TESTBENCH comes with the built-in base classes that allow the driving analog inputs with the given shapes such as sine, saw tooth, square and white noise. These source generators can be combined together to create specific shapes, for example, to add a sine waveform with a given maximum/minimum voltage and frequency with well distributed noise.

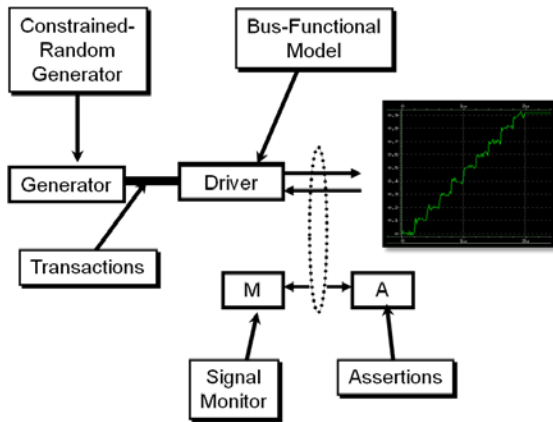


Figure 2: AMS-TESTBENCH Components

You can also use these base classes to model your own traffic shapes. An interesting application is to directly inject voltage waveform anywhere in your analog IP.

This is of particular interest for pipelined IPs or staged designs where you can skip the first stage and directly inject a given waveform to the second stage input. This approach allows you to speed up the simulation time without having to wait for the first stage to be ready.

However, as this waveform is modeled in SystemVerilog, you can model it in a few lines of code with specific traffic shapes, which in fact is difficult to achieve in SPICE.

3. ARCHITECTURE

The AMS-TESTBENCH technology allows easy connection between a top SystemVerilog environment and an analog netlist, which can be in Verilog-AMS or SPICE.

A very important aspect of this methodology is to enable the possibility to drive and sample an analog node directly from a SystemVerilog component or module. To achieve this, VCS comes with direct communication between a SystemVerilog real and an analog node.

With this communication, it becomes possible to have fine grain resolution to,

- Drive a SPICE electrical node by connecting it to a SystemVerilog real
- Sample a SPICE electrical node by converting it to a SystemVerilog real

Similarly, it is also possible to convert electrical to logic, i.e.,

- Drive a SPICE electrical node by connecting it to a Systemverilog logic
- Sample a SPICE electrical node by converting it to a Systemverilog logic

It is important to understand that the overall communication between SystemVerilog and SPICE is done with real. Therefore, all analog DUT nodes can be grouped in a single SystemVerilog interface.

So as in digital verification, SystemVerilog modports and clocking blocks can be introduced to determine analog node directions (input,

output, inout) and synchronization against a reference node such as a clock.

As stated in the assertion section, it also becomes possible to gather analog assertions in this interface.

This approach allows modeling interfaces efficiently that are easily reusable between projects and higher level of integration (i.e. from IP-level to SoC-level).

Now that we've solved the interfacing between SPICE and SystemVerilog, all verification techniques that are usual in digital verification can be fully leveraged. For instance, the verification environment can be architected with,

- Interfaces for electrical to real, real to electrical
- Generators to drive analog inputs
- Samplers to strobe analog outputs, these samplers can be combined with scoreboard or reference models to ensure the SPICE DUT is behaving as expected
- Configurations, which can be shared with the SPICE DUT
- Assertions that can be on SPICE boundary nodes or internal

However, it is also possible to cover analog nodes. A typical situation is explained to ensure some nodes are properly toggling. For instance, if an analog node is known to swing between 0.4V to 0.8V, it is fairly simple to associate this variation to toggle coverage and ensure this signal has moved as expected.

Figure3 shows a typical architecture based on AMS-TESTBENCH to verify an analog IP.

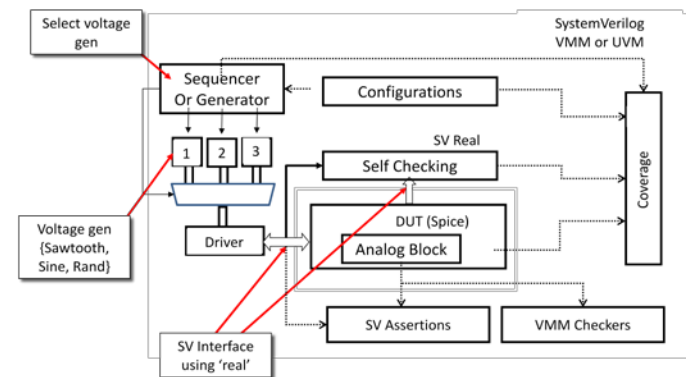


Figure 3: AMS-TESTBENCH for Analog IP

Extra attention is required during the self-checking capability of this testbench.

If the analog block is simply a transfer function - i.e. $y = f(x)$ - then the reference model can be written in SystemVerilog with the help of real scalars to model x , y and the transfer function.

If the analog block is more complicated, then it makes sense to use a language such as Verilog-AMS.

4. AMS ASSERTIONS

AMS-TESTBENCH technology makes it possible to write assertions with digital or analog nodes. The latter usually trigger events that are necessary for creating immediate, concurrent assertions or sequences.

4.1 Immediate Assertions

Analog assertions can be modeled with immediate assertions that consist of a sampling event and a property to be verified. The sampling event is usually a digital clock and the property is a combination of expressions applied to SystemVerilog real scalars.

As shown in Figure4, properties can simply be modeled as synchronous immediate assertion which checks whether an analog node remains below 1.8V on each rising edge of clk.

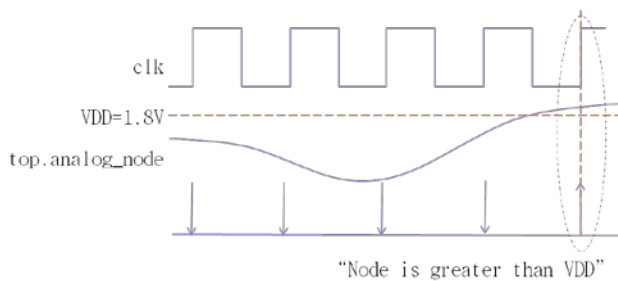


Figure 4: Analog Assertion

This can typically be used to make sure a DUT voltage reference always remains under a given value.

For example, the following pseudo code shows how to verify the above property:

```
always @(posedge clk)
  assert(top.analog_node <= 1.8)
  else $error("Node is > VDD");
```

Note that you can write assertions which are asynchronous in nature by using analog events.

4.2 Concurrent Assertions

Concurrent assertions are used to check more complicated behaviors.

These are statements that assert specified properties must be true. Such properties are usually needed for verifying well-defined protocols or behaviors.

For example, a PLL should be locked to the main frequency after a given time frame that can be expressed in terms of clock cycles.

Another example would be to verify relations between analog nodes. For instance, when *i* (analog node of interest) value is bigger than 90% of VDD=1.80V, *z* must be above 90% of VDD on the next clock or the following clock.

To assert such a property the assertion can be written as follows:

```
assert property @(posedge clk)
  (i>1.62) |-> ##[1:2] (z>1.62);
```

4.3 Sequences

Analog assertions can be explicitly specified in a sequence by using the non-overlapped operator `|->`, subsequent sequences are evaluated one after the other after each analog event.

The following example shows how to write a non-overlapped implication. The first element of the *s* sequence expression is evaluated on the next occurrence of `top.analog_clk`:

```
wire clk;
assign clk = top.analog_clk;

sequence s;
  @(posedge clk)
    (i>V_HIGH) |-> (z>V_HIGH);
endsequence

property p;
  (a<V_LOW) |-> s;
endproperty

assert property(p);
```

Analog assertions can be explicitly specified in a sequence by using an overlapped operator `|=>`. The subsequent sequences are evaluated one after the other during the same analog event. The following example shows how to write an overlapped implication:

```
property p;
  @(posedge clk)
    (i>V_HIGH) |=> (z>V_HIGH);
endproperty

assert property(p);
```

Here, *i* condition is first evaluated, if it is true then the *z* condition is evaluated at the same time.

4.4 Analog Events

The previous section explained how to trigger assertions with a digital clock.

Though the triggering event was an analog event, it was converted to a Verilog wire, making it easier to trigger sequences.

It is also possible to directly use the analog event as the triggering event.

```
always @(analog_clk)
  assert(top.analog_node <= 1.8)
  else $error("Node is > VDD");
```

5. AMS CHECKERS

As AMS-TESTBENCH provides the foundation for implementing analog assertions, it is natural to define some common analog checkers.

These common analog checkers can be modeled as Verilog modules, which can be easily instantiated and bounded to any analog node.

AMS-TESTBENCH also provides these checkers modeled as transactors extending from `vmm_xactor` and `uvm_component`. The main advantage of these components is that they can be controlled from the overall VMM/UVM environment. It becomes possible to decide when to start or stop them and get them implicitly controlled with other components.

5.1 Threshold Checker

There are many cases where one would like to ensure an analog signal remains within a given range.

For instance, some outputs should never go above a given voltage otherwise it might destroy the subsequent stages while overshooting.

Another example could be when an input of a given stage becomes negative or superior to a given threshold. This situation could occur when two stages have different power domains and there are no adequate level shifters.

AMS-TESTBENCH provides such a checker that verifies an analog node remains within a given high and low threshold. This check can be performed synchronously or asynchronously.

This is illustrated in Figure5. The first checkpoint is valid as the voltage is within the expected ranges; however, the second checkpoint will fire off an error as the voltage becomes higher than expected.

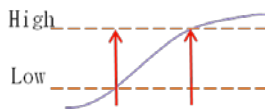


Figure 5: Threshold Waveform

5.2 Window Checker

There are situations where one would like to ensure an analog signal remains stable with a given tolerance. For instance, voltage references or band gaps should continue sinking a stable voltage reference independently of process, supply voltage and temperature.

AMS-TESTBENCH provides such a checker that verifies an analog node remains stable below or above a given threshold.

This is illustrated in Figure6. The first checkpoint is invalid as the voltage is not within the expected tolerances, therefore, the checker will fire off an error.

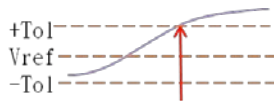


Figure 6: Window Checker

5.3 Slew Rate Checker

There are situations where one would like to ensure the slew rate of an analog signal remains below or above a given value. For instance, comparators have a minimal output slew rate that must be respected independently of process, supply voltage, temperature.

AMS-TESTBENCH provides such a checker that verifies an analog node slew rate (+/- tolerance) remains below or above a given value.

This is illustrated in Figure7, which shows how this checker operates. The first checkpoint is valid as the voltage slew rate is greater than the expected dV/dt . However the checker will fire off an error on the second checkpoint.

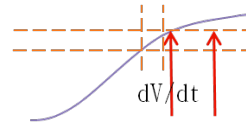


Figure 7: Slew Rate Checker

5.4 Frequency Checker

There are situations where one would like to ensure the frequency of an analog signal remains within a given tolerance. For instance, PLLs are supposed to output stable frequency once they are locked for any valid variations of {process, voltage, temperature}.

AMS-TESTBENCH provides such a checker that verifies an analog node frequency remains stable (+/- tolerance).

This is illustrated in Figure8, which explains how this checker operates. The first checkpoint is valid as the voltage frequency is as expected. However, the checker will fire off an error on the fourth checkpoint as the period decreased.

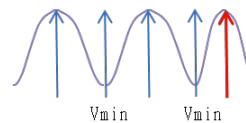


Figure 8: Frequency Checker

6. VOLTAGE REFERENCES

AMS-TESTBENCH contains a few source generators that can be bound to internal or external analog nodes. These generators are responsible for driving a particular traffic to your analog IP.

For example, the sine source generator can drive a well-defined sine with determined minimum/maximum voltages at a given frequency. Other source generators such as saw tooth, square are also available. Injection of random voltage is also possible.

As shown in the following diagram, it is possible to pick a generator followed by another one and so on.

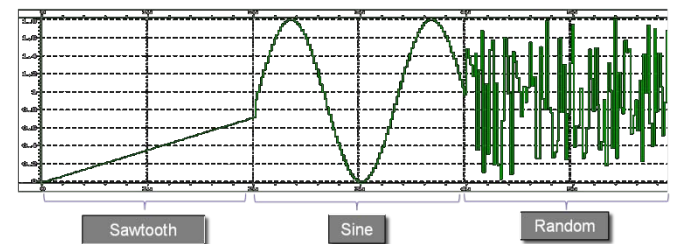


Figure 9 Multi-generation modulation

Additionally, source generators can be combined together to inject more complicated traffic.

A typical situation is to add white noise on top of a carrier, which is a generated sine source. This can be useful to model external perturbation or to determine the common-mode rejection ratio (CMRR) of a differential amplifier (or other device), which is the tendency for the device to reject input signals common to both input leads.

As shown in Figure10, the signal of interest can be represented by a small voltage fluctuation superimposed on a voltage carrier.

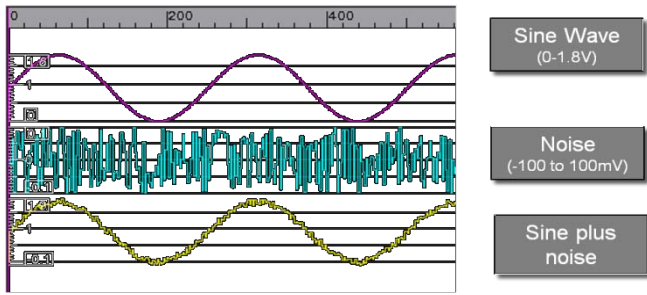


Figure 10: Carrier with Noise

As these generators do output voltages at a regular pace, it is important to ensure the signal shape is accurate enough without slowing down the simulation too much. An acceptable tradeoff is to output 10 samples / period (e.g. sample rate = 10X frequency).

6.1 Standard Voltage Generator

It is typical in SPICE to drive analog nodes with a saw-toothed or triangle shape, which can be done with the SAWGEN directive.

AMS-TESTBENCH proposes a saw tooth source generator that provides a real value which can be used to drive analog voltage node with a saw tooth shape. You can specify min and max voltages V_{min} , V_{max} and the frequency f . This is shown in Figure11.

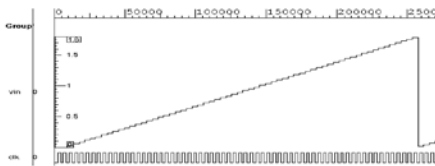


Figure 11: Sawtooth Waveform Generator

Another very important generator is the sine waveform generator.

AMS-TESTBENCH provides a real value waveform generator that can be used to drive analog voltage node with a sine shape. You can specify min and max voltages V_{min} , V_{max} and the frequency f . These values can be changed during the simulation time. This is shown in Figure12.

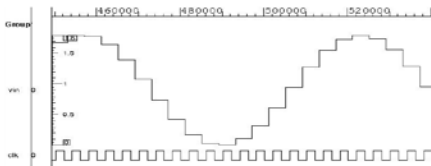


Figure 12: Sine Waveform Generator

Similarly, AMS-TESTBENCH provides a real value waveform generator that can be used to drive analog voltage node with a square shape (which can be done with the PWL directive in SPICE).

You can specify min and max voltages V_{min} , V_{max} , the frequency f and the duty cycle. These values can be changed during the simulation time. This is shown in Figure13.

The square voltage source generator provides a real value that can be used to drive analog voltage node with a square shape.

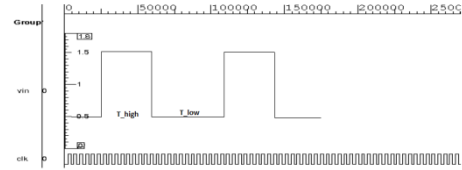


Figure 13: Square Waveform Generator

In addition, AMS-TESTBENCH provides a random voltage generator provides a real value that can be used to drive analog voltage node with a random shape.

This can be useful when combined with other standard source generators. For instance, it can be used to inject errors, distortion or perturbation to a given known good signal. It can also be used for adding noise on top of a carrier or directly in a voltage reference.

You can specify min and max voltages V_{min} , V_{max} . These values can be changed during the simulation time. This is shown in Figure14.

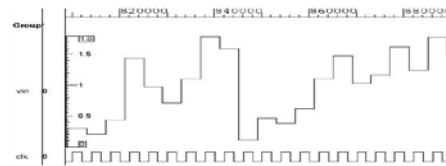


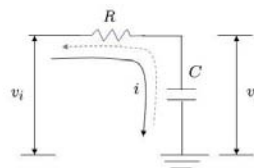
Figure 14: Random Waveform Generator

6.2 Custom Voltage Generator

In addition to pre-defined voltage shapes, it is possible to write custom voltage source generators.

For example, to model a RC low pass filter governed by the following equation:

$$V_{out} = (V_{max} - V_{min}) \times e^{-\frac{t}{RC}}$$



This generator can then be controlled and initialized to output voltage as illustrated in Figure 15: RC Waveform Generator where $V_{min}=-1V$, $V_{max}=1V$, $F=1MHz$, $RC=200ns$:

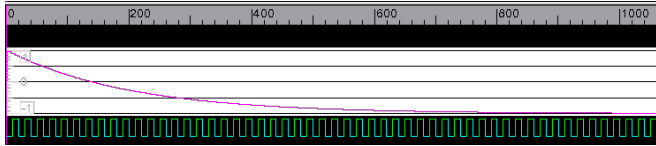


Figure 15: RC Waveform Generator

For more details, refer to AMS-TESTBENCH user guide.

6.3 Voltage Generator Control

As described in the previous sections, all the source generators are easily constructed and their analog value is deposited to analog node by explicitly calling their `get_voltage()` method at regular times.

AMS-TESTBENCH use model is easy but can be further simplified with the generic VMM source generator, which is based on `vmm_xactor`.

AMS-TESTBENCH provides better integration, direct access to pre-defined SystemVerilog interface and better controllability (hence reuse at SoC for example). Additionally, this component comes with pre-defined notification that indicates when its embedded source generator reaches its half period. This is useful for changing its parameters in a well defined way, i.e. when the source generators reach a given state.

Further, the source generator can be started and stopped on purpose by using the VMM `start_xactor` and `stop_xactor` methods.

7. CASE STUDY

To prove that a generic AMS-TESTBENCH solution built on top of VMM or UVM would be viable, a simple Amplifier DUT and its verification environment were developed.

The objective of the case study was to replace Calvatec's existing SystemVerilog testbench and the AMS base classes by using more mainstream methodology such as Synopsys AMS-TESTBENCH built on Accellera UVM code.

The criterion for the case study was to leverage the pre-defined standard voltage generators which in turn would leverage the built-in math functions.

UVM was used as the underlying SV base class library and the simulations were executed in the following two modes.

- Mode 1: Pure digital simulation with VCS only.
- Mode 2: Mixed signal simulation with VCS and Nanosim

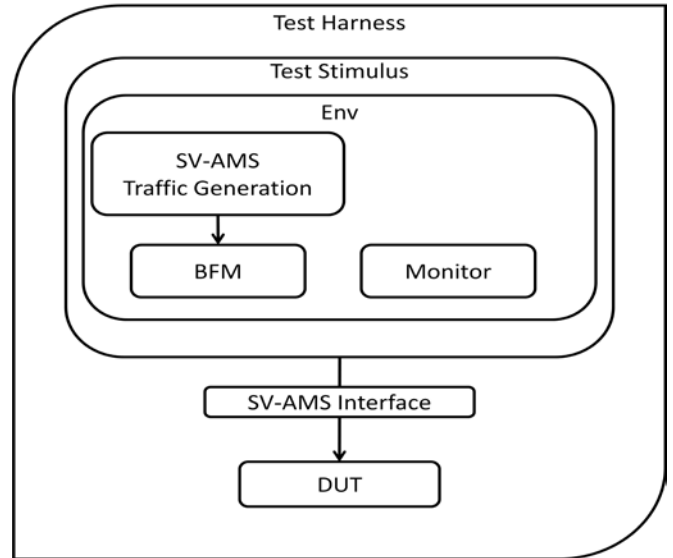


Figure 16: Architectural Overview

As shown in Figure16, SystemVerilog interface was used to carry the AMS signal information. The default `ams_interface` was placed in the UVM resource database, and then used by the verification environment to drive the signal into DUT. We used the built-in AMS-TESTBENCH checkers to ensure signal was correct at the monitor.

Adding more classes such as agents, tests, configurations, sequencers etc. were superfluous to the objective of understanding how the AMS-TESTBENCH generation would verify DUT.

Waveforms below show that by connecting the environment together and using a sine wave traffic generator, DUT does perform amplification at the required gain of 2.5x. The electrical representation is done using a sampling signal which provides the accuracy of the digital signals.

In Mode 2, the gain was set as 1 and here the analog code was simulated by using VCS and Nanosim.

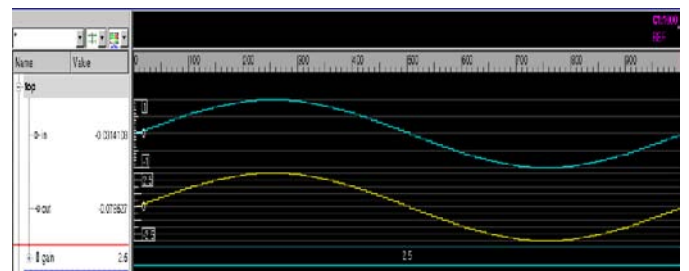


Figure 1: Mode 1 with Gain of 2.5

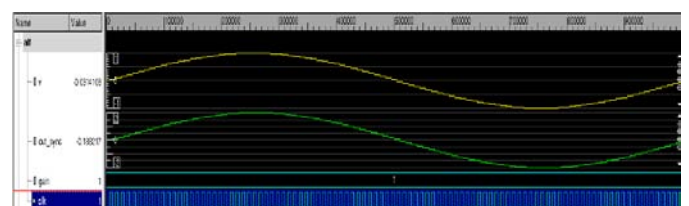


Figure 2: Mode 2 with Gain of 1

By successfully proving that the setup and code runs as expected, the case study example could be developed upon to have multiple agents with multiple BFMs and monitors in the verification environment.

Therefore, Calvatec will now have an access to the complete benefits of UVM and AMS-TESTBENCH without having to maintain their own internal base classes.

This also means they can leverage the built in checkers and techniques used to verify Mixed-Signal DUT's.

The key advantage of having both the modes, pure digital and mixed-signal simulations means that you can control the performance and accuracy of the simulations.

For certain parts of verification it is perfectly legitimate to run with very low accuracy but high performance enabling much better regression throughput. Then by enabling more accuracy for other types of tests without a change to the infrastructure gives us confidence in other areas of DUT.

All of this coupled with the built in coverage models delivered with AMS-TESTBENCH makes it a robust solution offering increasing confidence in the design while mitigating risk.

As shown in Figure17, the cp_vmax analog voltage nodes can be broken down into ranges {min, typ, max} and crossed with another node cp_vi. This is an efficient way of verifying that all possible combinations are covered. In this case, it's easy to see that cp_vi didn't fully address all expected values.

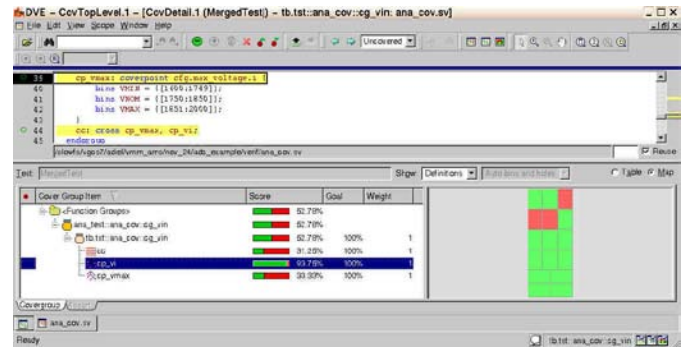


Figure 17. Analog Functional Coverage

8. REFERENCES

- [1] Synopsys. "VMM 1.2 User Guide"
- [2] Accellera VIP. "UVM 1.0 User Guide"
- [3] IEEE-1800-2009
- [4].Shyam Rapaka, Tapan Halder, Vikas Chandra. "A SystemVerilog Approach for Analog/Mixed-signal Verification". DVCON'09