An efficient requirements-driven and scenario-driven verification flow

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Outline

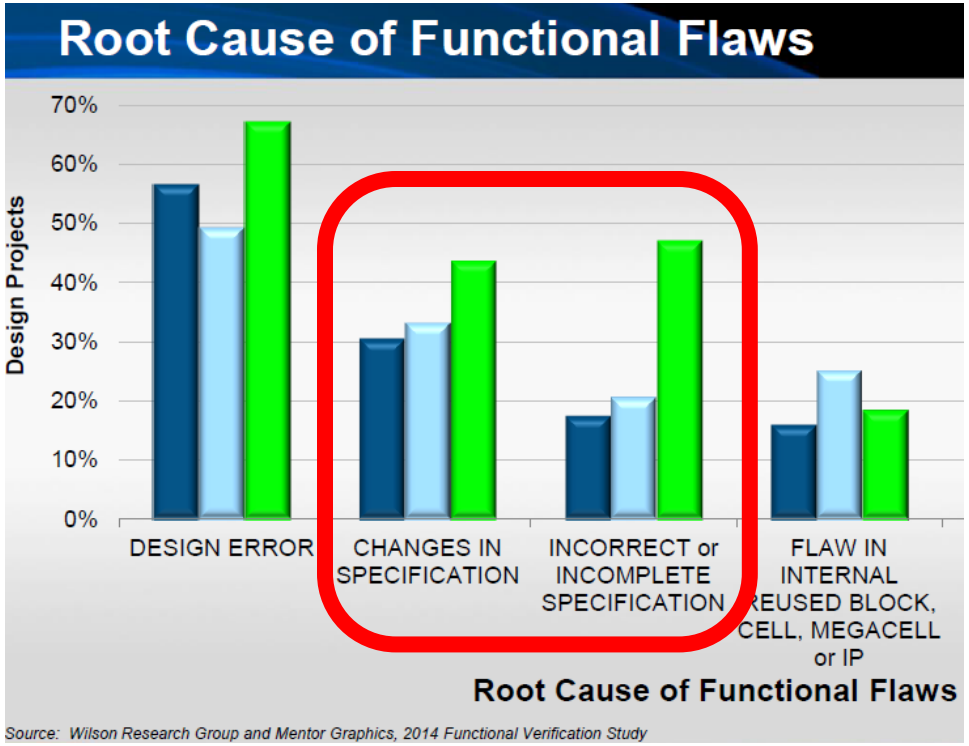
- Motivation
- Verification methodologies
- Combining Requirements Based verification (RBV) and Metric-Driven Verification (MDV)
- Scenario modeling for top-level verification
- Conclusions / acknowledgement

Motivation

- Test specification setup and maintenance effort must be reduced. (x1000 spec items)
- Long and detailed specification lists weaken the overview.

Opportunities to improve:

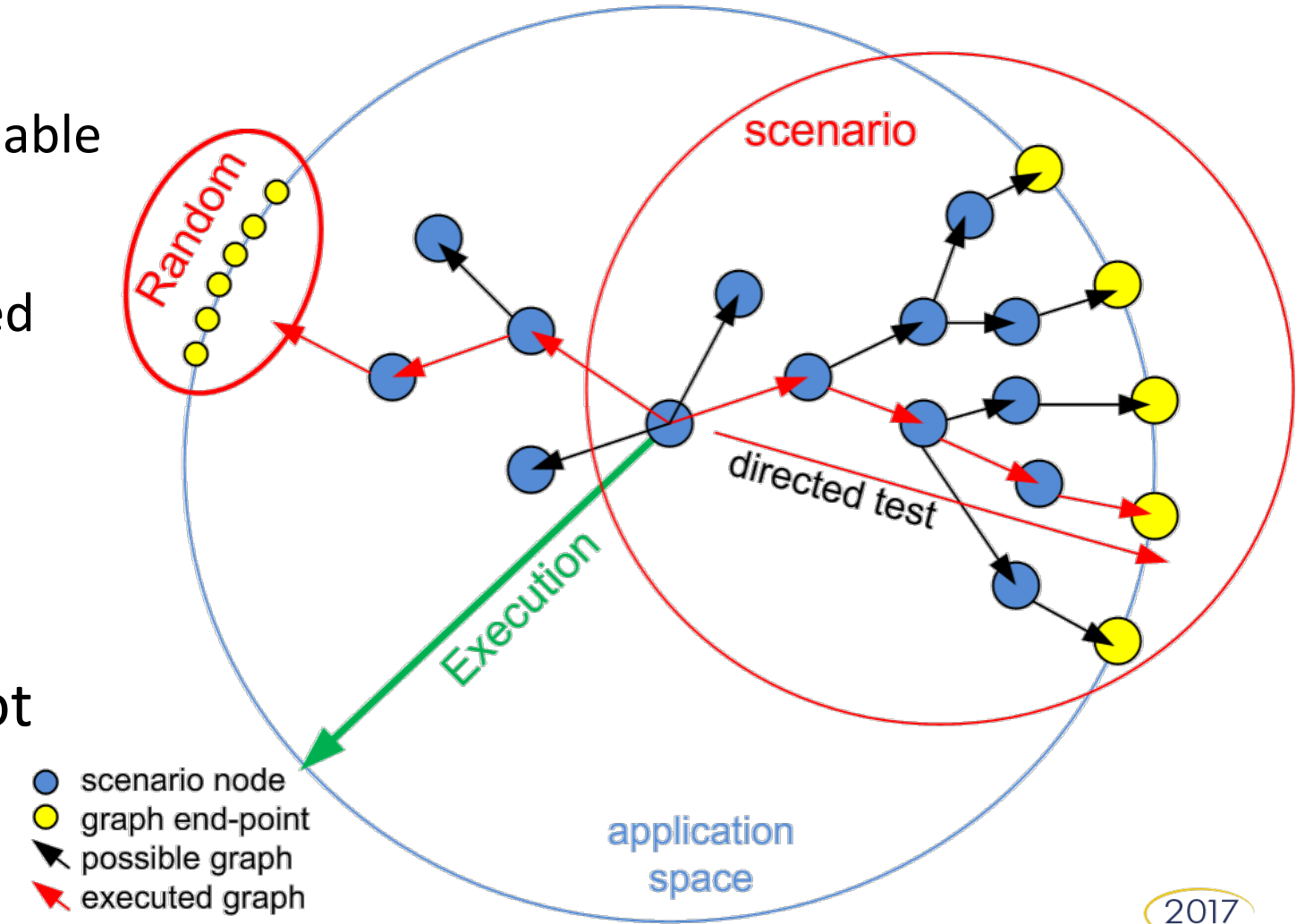
- Efficient test specification flow must be functional verification aware.
- Coverage of IP must contribute to top-level verification quality proof.
- Automated test creation



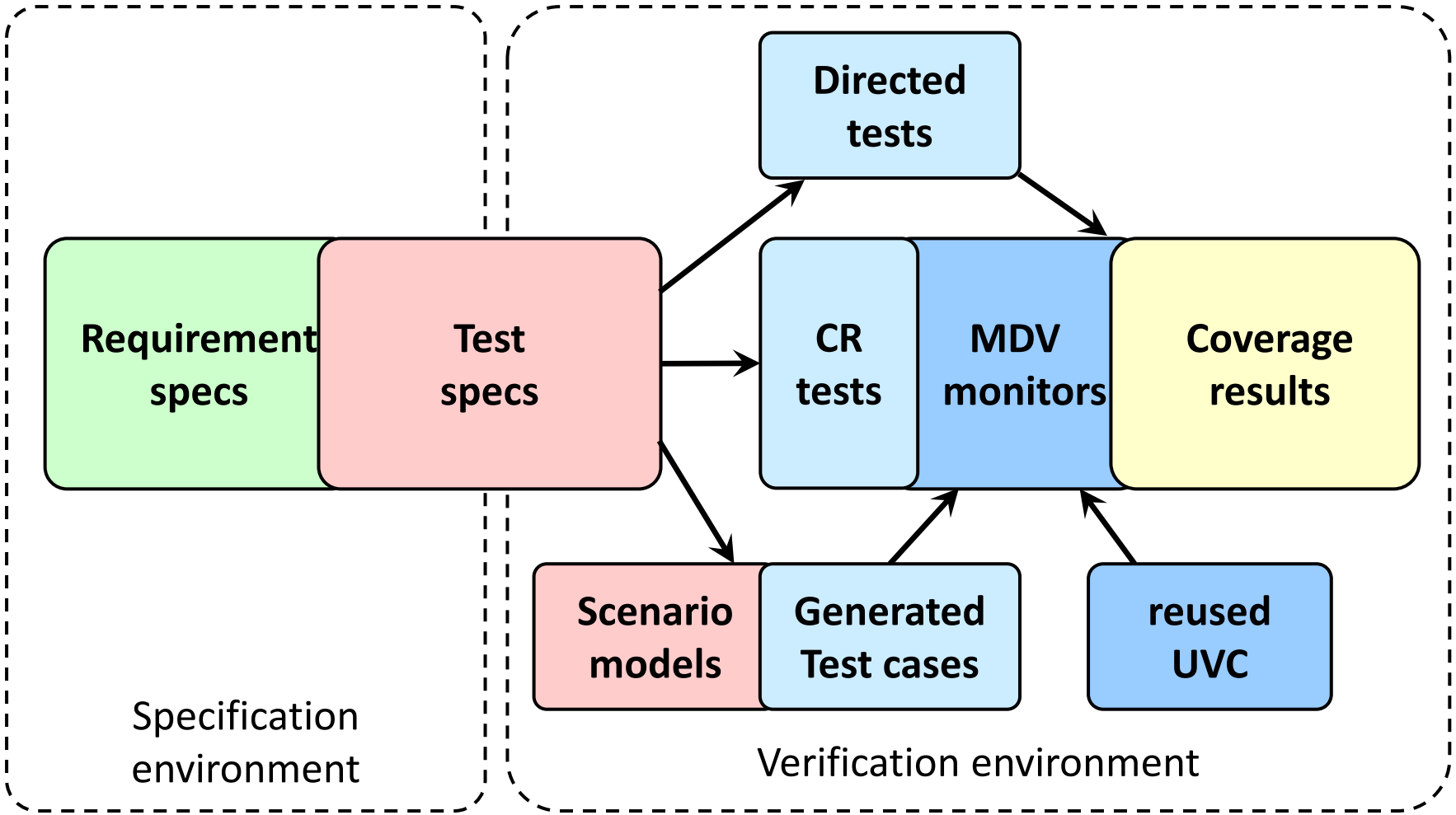
Verification methodologies

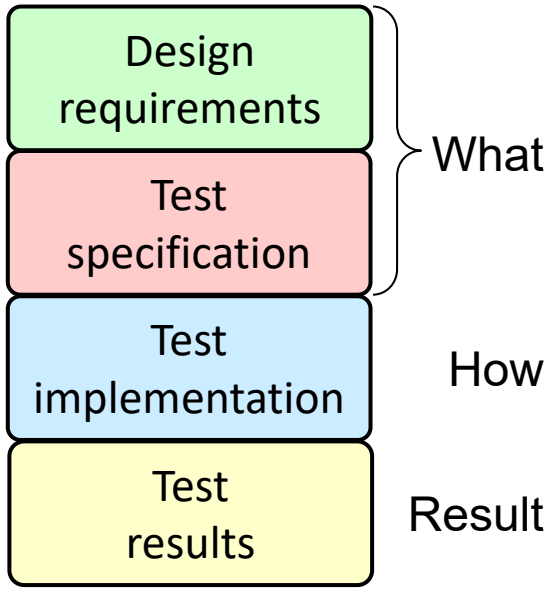
- Directed test
  - Traditional, corner-cases, traceable
- Constraint Random
  - IP verification, UVM, automated
- Scenario-driven
  - Constraint random at top-level
  - Design intent

Top-level verification sweet spot is proper combination

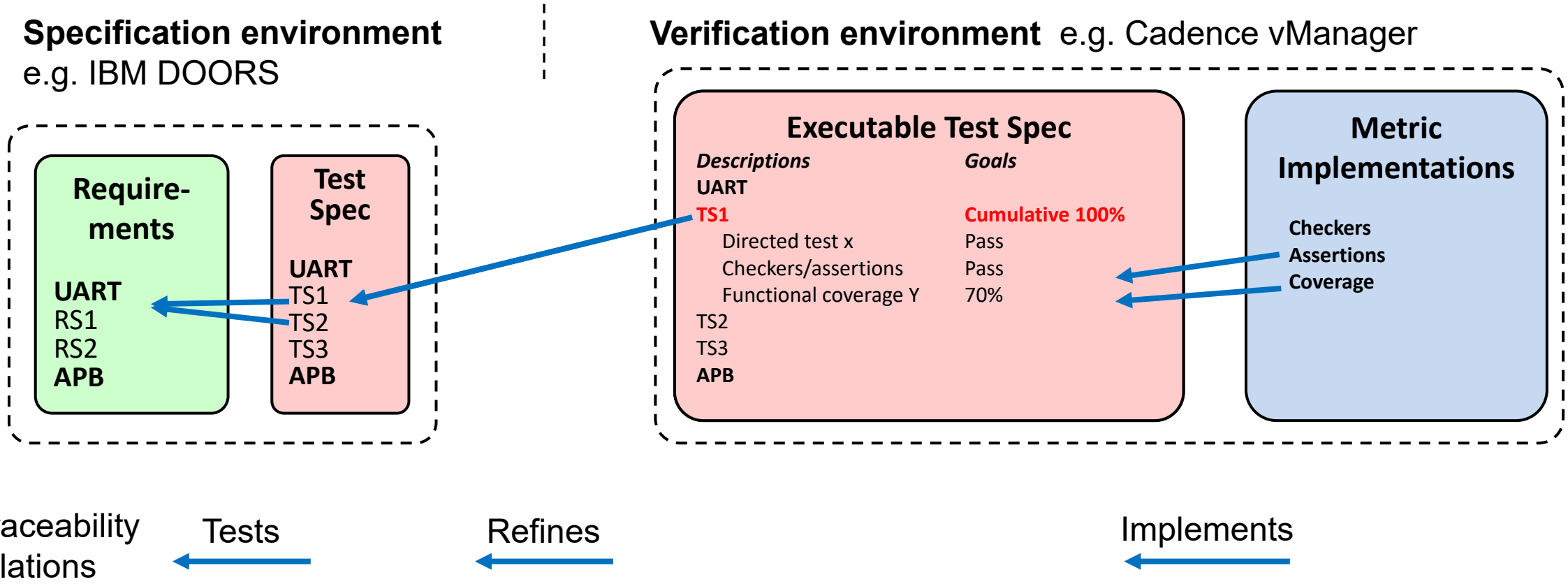


RBV and MDV for top-level verification





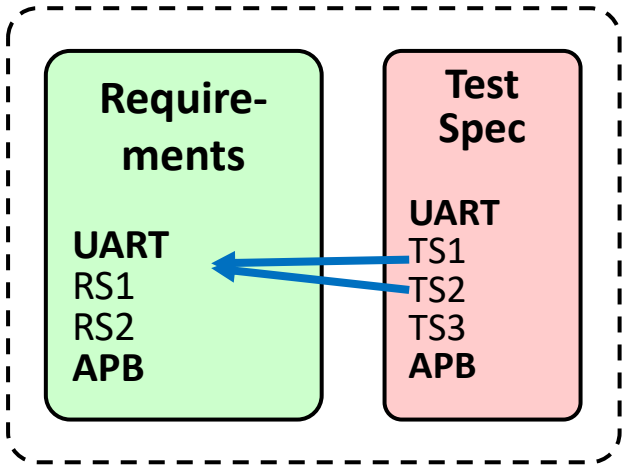
Traceability relations: Requirements to Test results



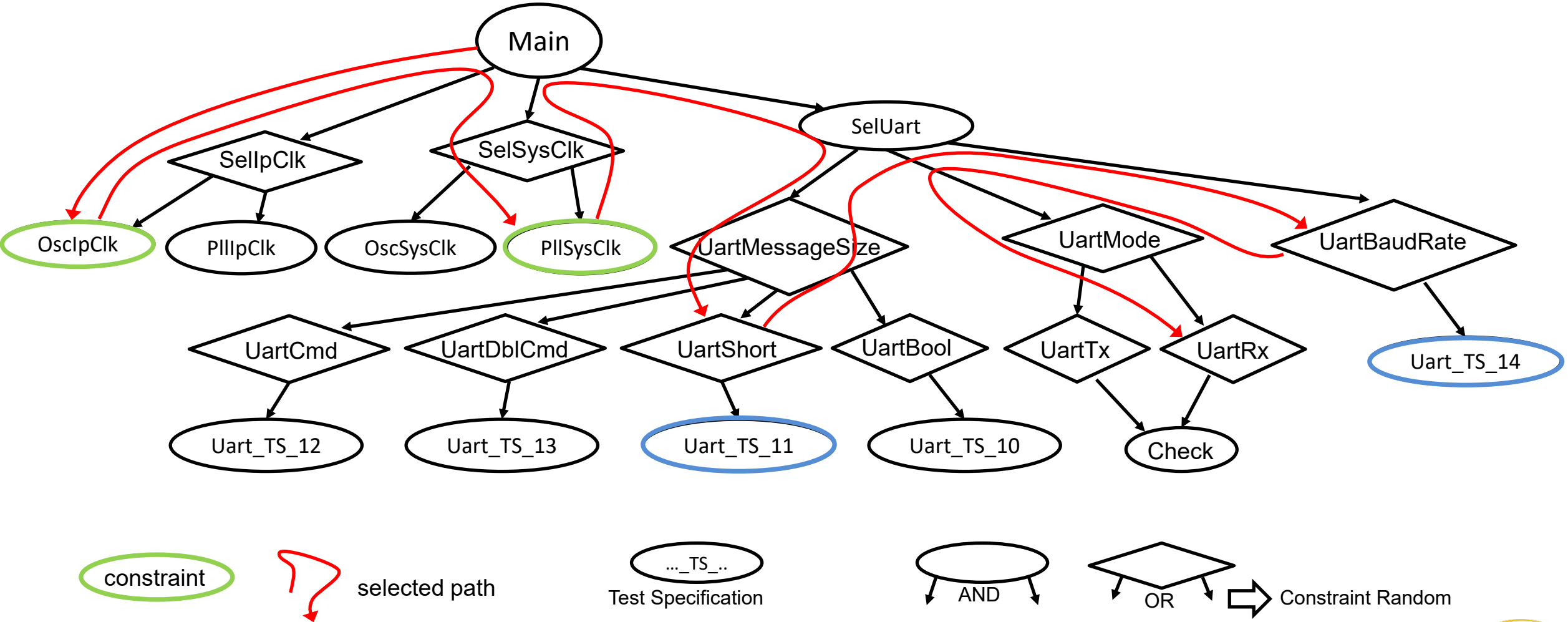
Test Cases on TopLevel

Move from directed/use case driven to scenario driven as:

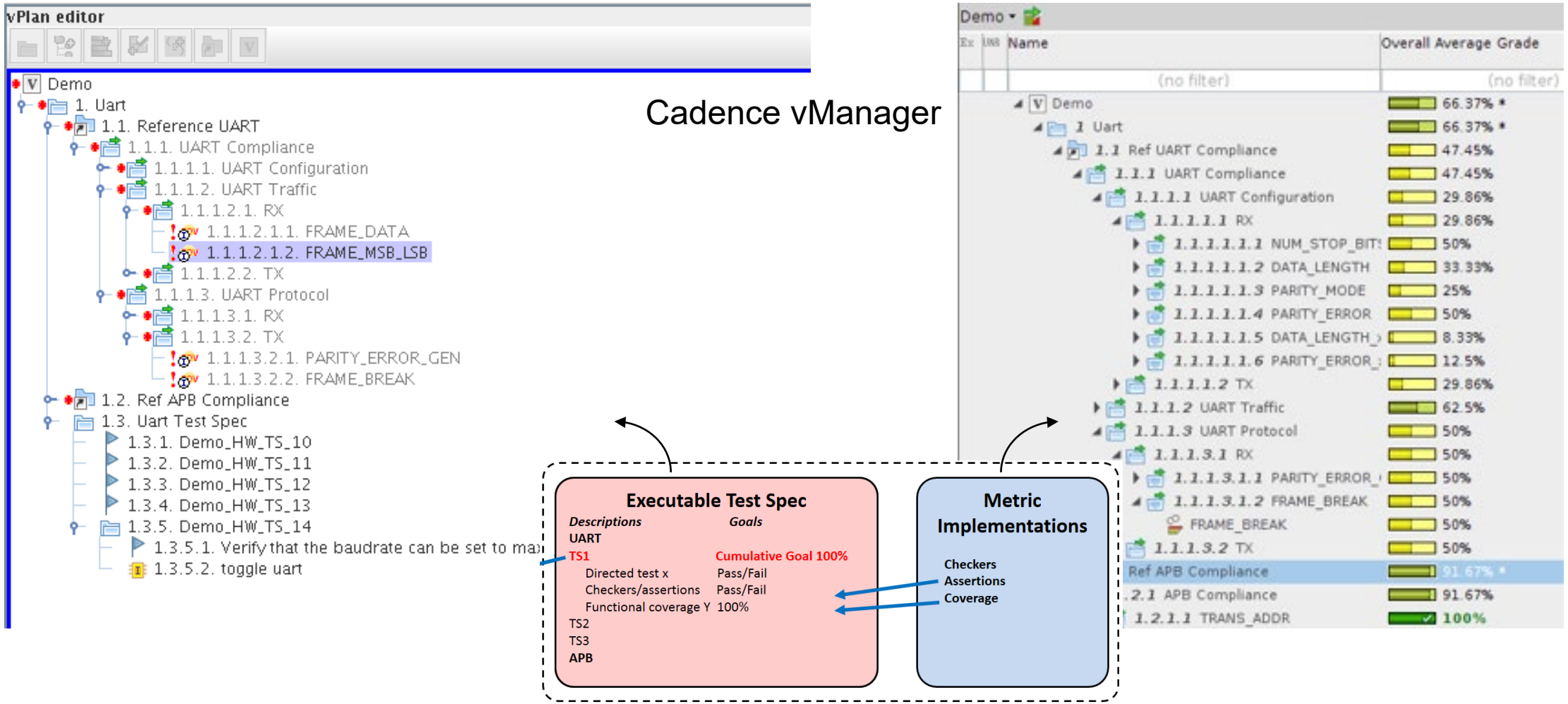
- Scenarios specify the behavior of the system
- Scenarios define the intent of the design
- Functional End Points known, but paths can vary
- End Points can be linked to Test Spec Items for early traceability!



Simple top-level scenario for UART



Results of one scenario and it's IP coverage results



Conclusions

- Executable Test Specification, is proper place to refine test specifications.
- Scenario modeling increases confidence of completion in top-level verification.
- Reuse from IP to Top-level verification can be achieved by passive Verification Component.
- This methodology concept has been applied successfully.
- The overview of verification quality and coverage has increased.

Acknowledgment

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  - Walter Tibboel
  - Shuang Han for UVM support
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Questions?