

An efficient requirements-driven and scenario-driven verification flow

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Outline

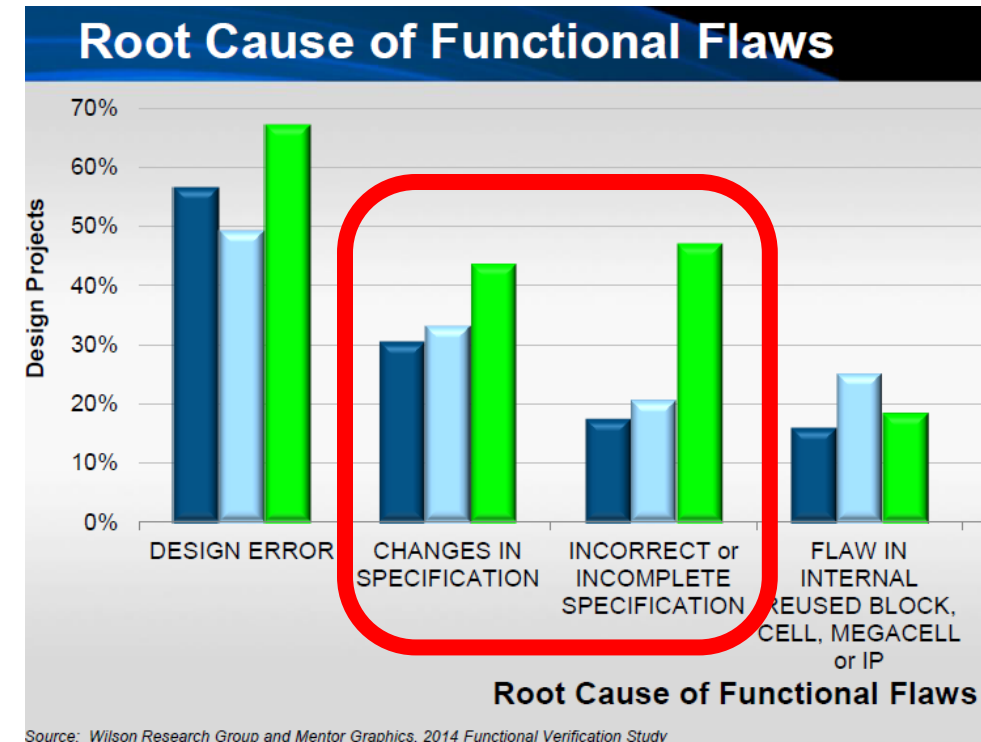
- Motivation
- Verification methodologies
- Combining Requirements Based verification (RBV) and Metric-Driven Verification (MDV)
- Scenario modeling for top-level verification
- Conclusions / acknowledgement

Motivation

- Test specification setup and maintenance effort must be reduced. (x1000 spec items)
- Long and detailed specification lists weaken the overview.

Opportunities to improve:

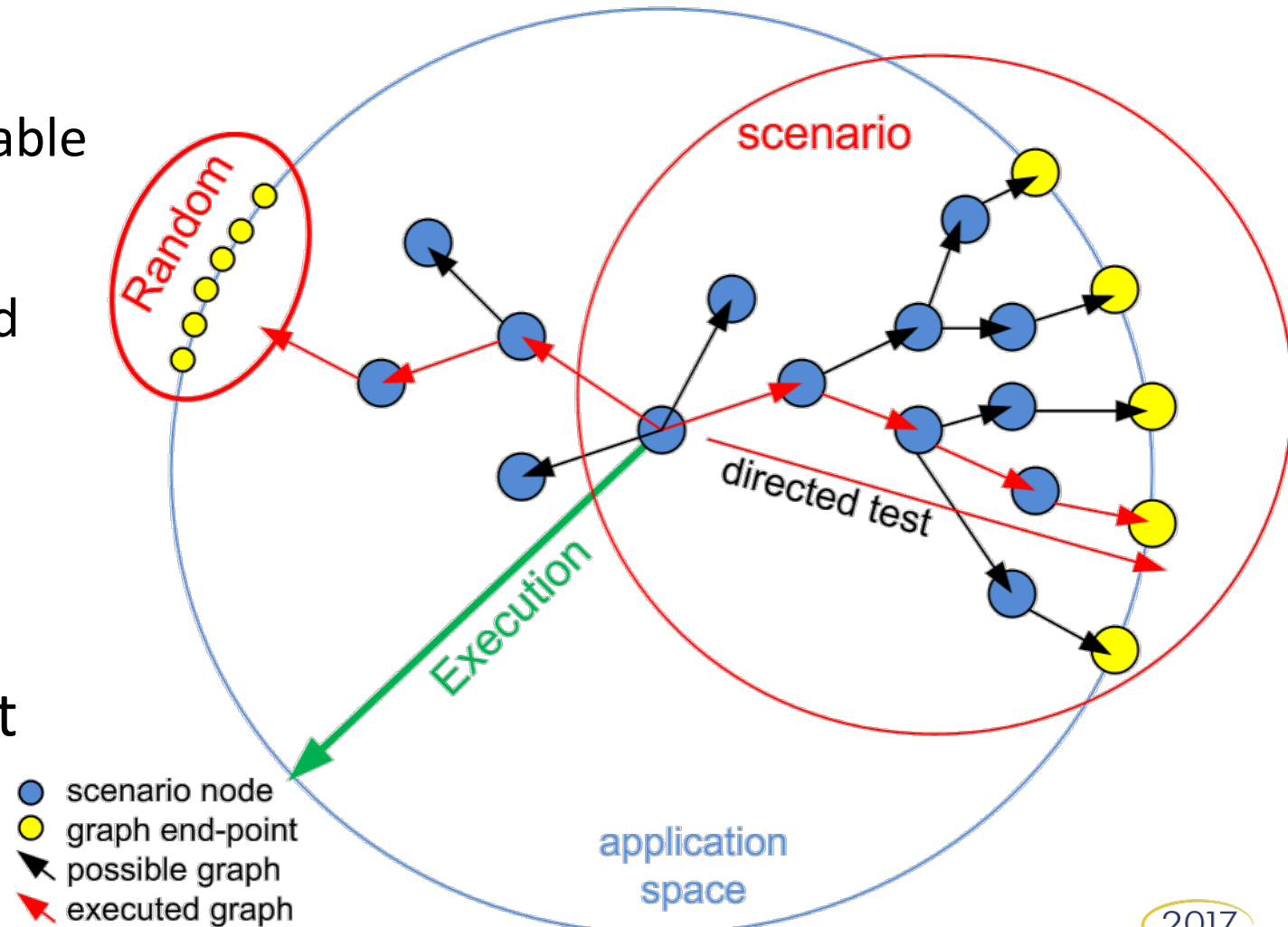
- Efficient test specification flow must be functional verification aware.
- Coverage of IP must contribute to top-level verification quality proof.
- Automated test creation



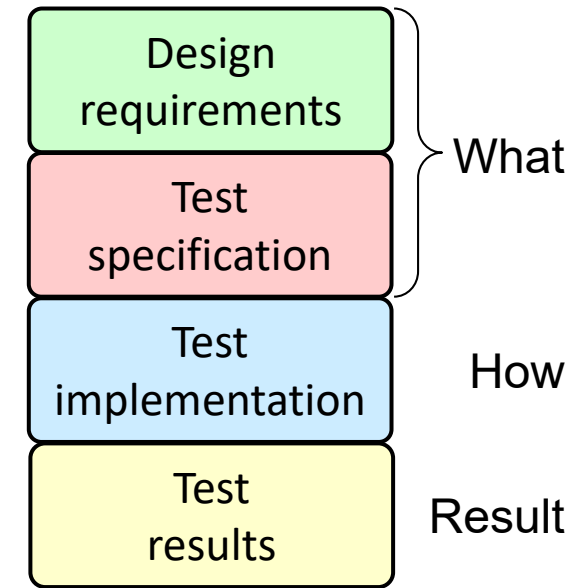
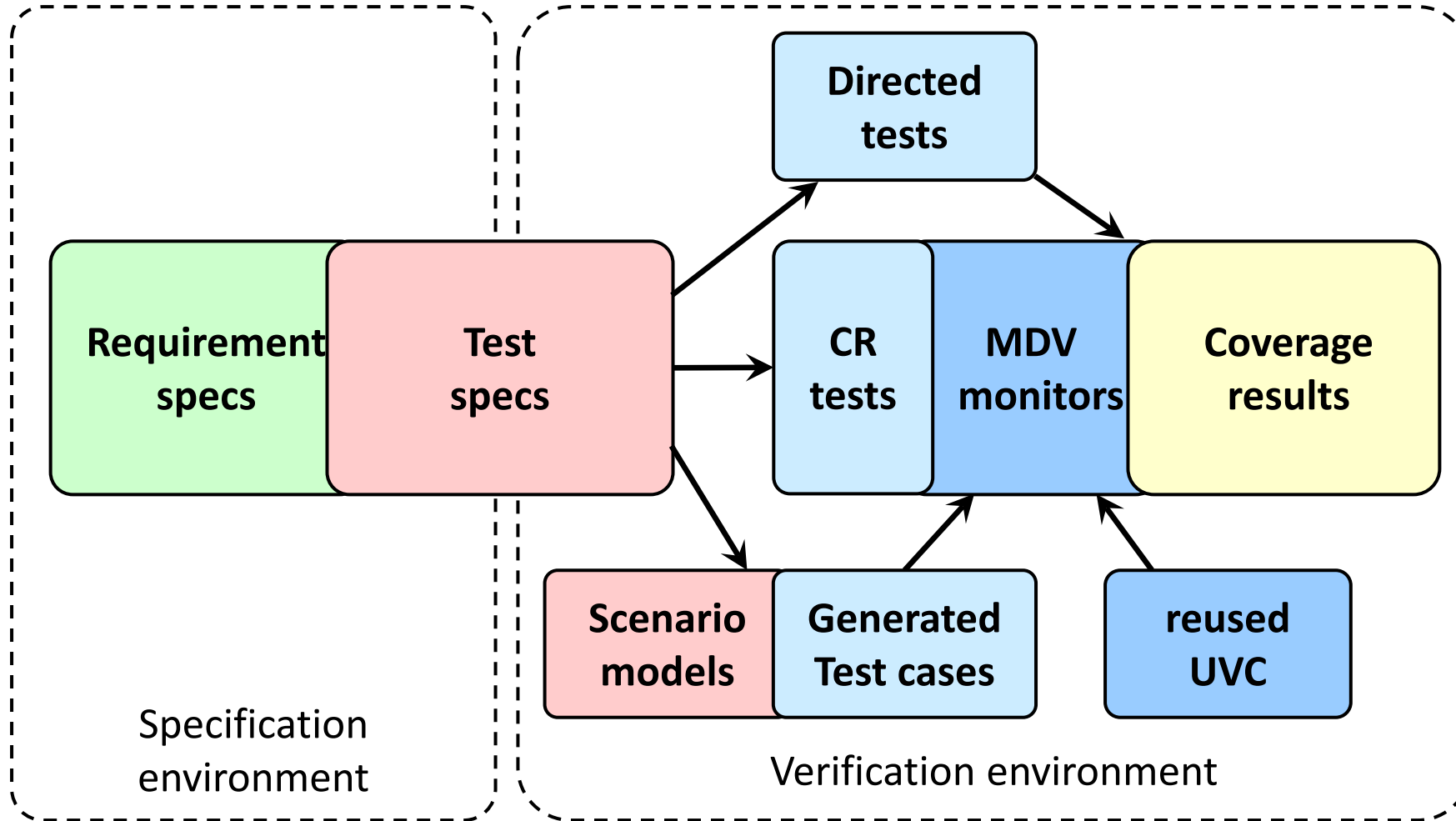
Verification methodologies

- Directed test
 - Traditional, corner-cases, traceable
- Constraint Random
 - IP verification, UVM, automated
- Scenario-driven
 - Constraint random at top-level
 - Design intent

Top-level verification sweet spot
is proper combination

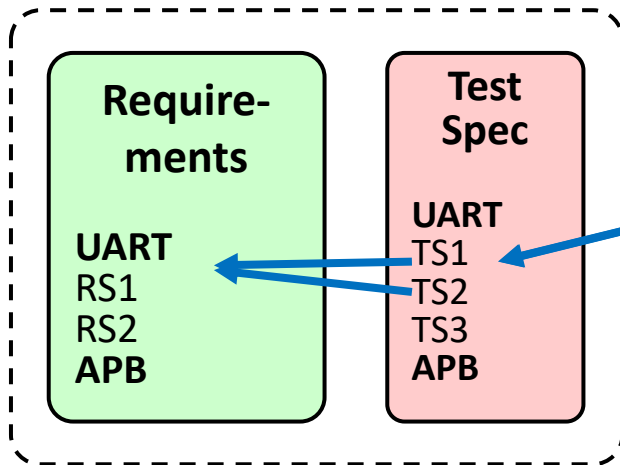


RBV and MDV for top-level verification

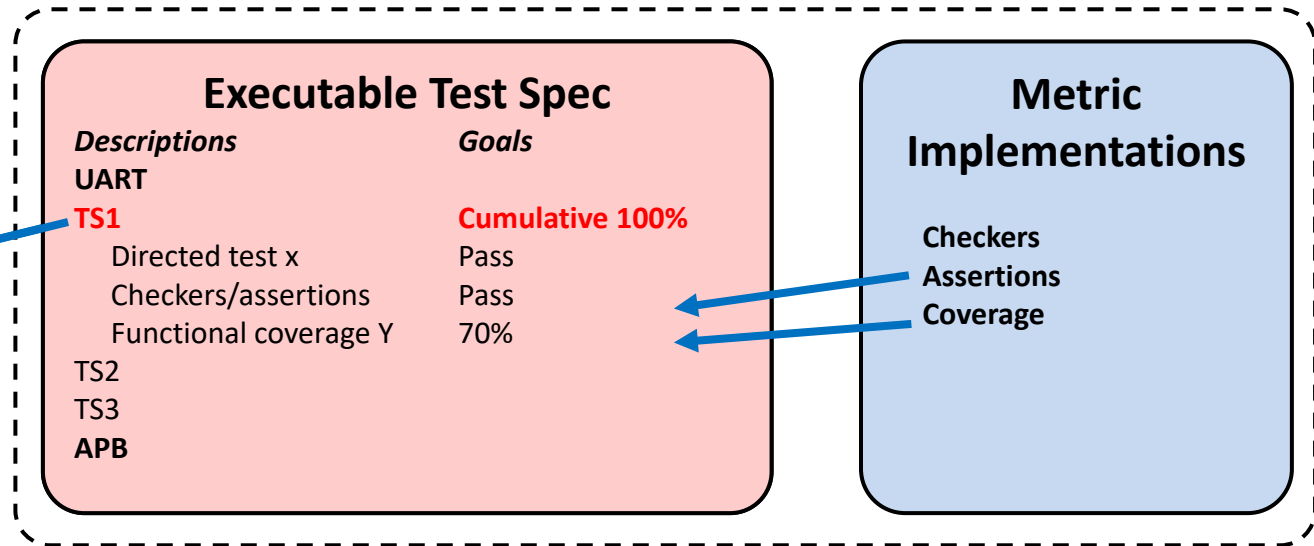


Traceability relations: Requirements to Test results

Specification environment
e.g. IBM DOORS



Verification environment e.g. Cadence vManager



Traceability relations

← Tests

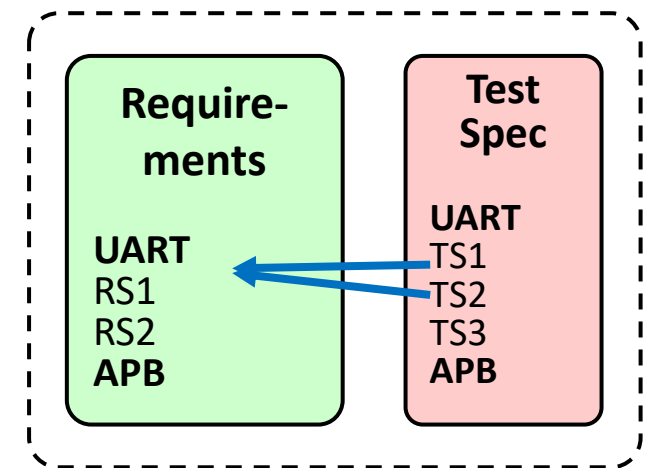
← Refines

← Implements

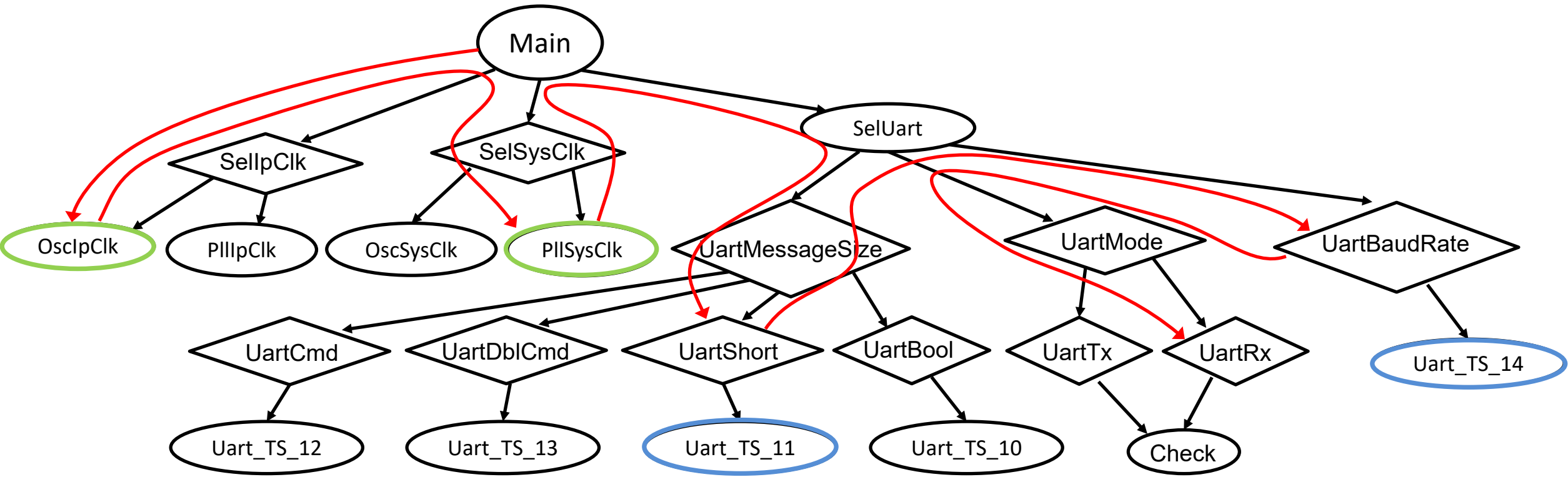
Test Cases on TopLevel

Move from directed/use case driven to scenario driven as:

- Scenarios specify the behavior of the system
- Scenarios define the intent of the design
- Functional End Points known, but paths can vary
- End Points can be linked to Test Spec Items for early traceability!



Simple top-level scenario for UART



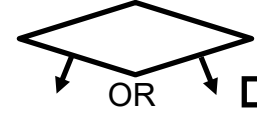
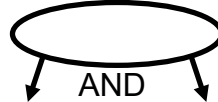
constraint



selected path

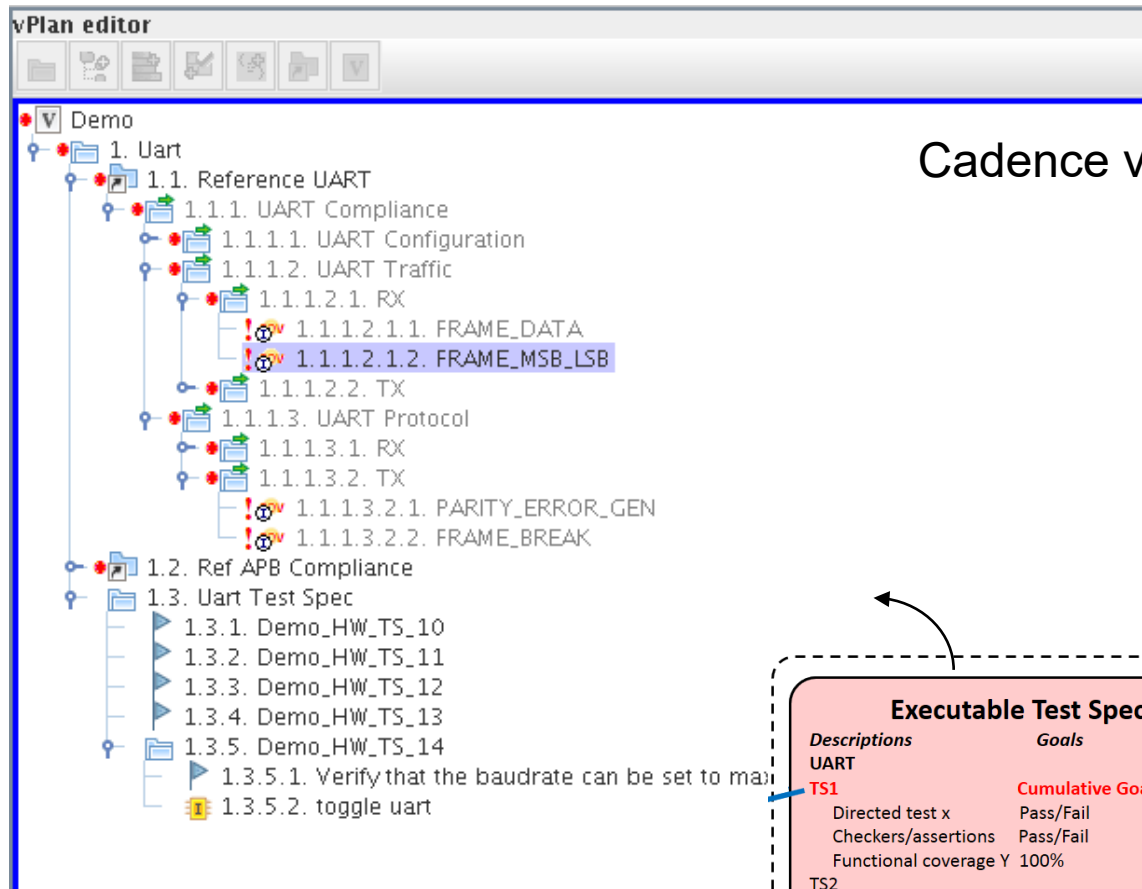
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Test Specification



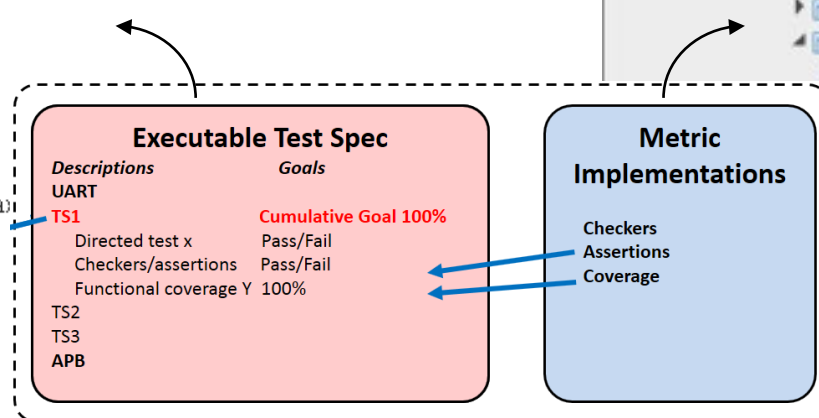
Constraint Random

Results of one scenario and it's IP coverage results



Cadence vManager

Ex	Unit	Name	Overall Average Grade
		(no filter)	(no filter)
	▼	Demo	66.37% *
	▲	1 Uart	66.37% *
	▲	1.1 Ref UART Compliance	47.45%
	▲	1.1.1 UART Compliance	47.45%
	▲	1.1.1.1 UART Configuration	29.86%
	▲	1.1.1.1.1 RX	29.86%
	▶	1.1.1.1.1.1 NUM_STOP_BIT:	50%
	▶	1.1.1.1.1.2 DATA_LENGTH	33.33%
	▶	1.1.1.1.1.3 PARITY_MODE	25%
	▶	1.1.1.1.1.4 PARITY_ERROR	50%
	▶	1.1.1.1.1.5 DATA_LENGTH_2	8.33%
	▶	1.1.1.1.1.6 PARITY_ERROR_2	12.5%
	▶	1.1.1.1.2 TX	29.86%
	▶	1.1.1.2 UART Traffic	62.5%
	▲	1.1.1.3 UART Protocol	50%
	▲	1.1.1.3.1 RX	50%
	▶	1.1.1.3.1.1 PARITY_ERROR_1	50%
	▶	1.1.1.3.1.2 FRAME_BREAK	50%
	▶	FRAME_BREAK	50%
	▶	1.1.1.3.2 TX	50%
		Ref APB Compliance	91.67% *
		2.1 APB Compliance	91.67%
		1.2.1.1 TRANS_ADDR	100%



Conclusions

- Executable Test Specification, is proper place to refine test specifications.
- Scenario modeling increases confidence of completion in top-level verification.
- Reuse from IP to Top-level verification can be achieved by passive Verification Component.
- This methodology concept has been applied successfully.
- The overview of verification quality and coverage has increased.

Acknowledgment

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Questions?