2014 DESIGN AND VERIFICATION DVCON CONFERENCE AND EXHIBITION EUROPE

An Effective Design and Verification Methodology for Digital PLL

Biju Viswanathan, Rajagopal P.C, Ramya Nair S. R, Joseph J Vettickatt, Jobin Cyriac
Network Systems and Technologies (P) Ltd, Kerala, India
biju.viswanathan@nestgroup.net, rajagopal.pc@nestgroup.net , ramya.nair@nestgroup.net , joseph.vettickatt@nestgroup.net , jobin.cyriac@nestgroup.net

Abstract— This Paper depicts an effective simulation methodology to overcome the spice simulation time overhead of digital dominant, low frequency Digital PLL (DPLL). A low power wide range Digital Phase-Locked Loop (DPLL) design for generating precise pixel clock from a noisy and low frequency horizontal synchronization signal (HSYNC) is described here. The basic design challenges faced by pixel clock generator are Noisy low-frequency reference clock and Very high Feed back frequency multiplication ratio. Here, the verification methodology of the DPLL is divided into two stages

1. Digital blocks are designed and verified with stringent test cases using SystemVerilog and analog block models. Analog blocks are designed using normal spice simulation. 2. Co-simulation environment is used for sign-off.

Keywords—DPLL, SystemVerilog, Co-simulation,mixed signal validation

I. INTRODUCTION

A low power wide range Digital Phase-Locked Loop (DPLL) design for generating precise pixel clock from a noisy and low frequency horizontal synchronization signal (HSYNC) is described here. Digital PLL's are used in video front-end systems as pixel clock generator. In such applications, reference signal (HSYNC) used is of low frequency with range of 30Hz to 100 KHz. , and the output pixel clock ranges from 76 MHz to 800 MHz based on different display resolutions. This DPLL design uses an analog oscillator circuit which ensures high linearity and portability to other technologies.

This paper describes the simulation challenges of low frequency analog mixed signal systems and proposes an effective mechanism to reduce the simulation overhead using SystemVerilog and co-simulation environment. This methodology reduces the simulation effort to 1/3rd of the actual spice simulation effort. Also it enables the designer to make the design fool proof.

Here the simulation effort of DPLL circuit is divided into two steps making use of SystemVerilog verification, co-simulation. The DPLL loop consists of almost 80% digital components. It is cumbersome to analyze the entire loop using spice simulation for loop analysis. Even the functionality confirmation of the loop is time consuming as the system operates over a very wide range of division ratios (N). This practical simulation issue is addressed by the modeling of analog systems in the initial stages and by co-simulation in the advanced stage of system design.

Another major design challenge in design of the type of circuit is the validation of digital blocks. Validation of the complex digital filter and controller are done with SystemVerilog methodologies and test benches. This ensures the functionality of digital blocks across all corner cases. 100% code coverage is ensured for the digital blocks.

The Paper describes the system level architecture of the DPLL, its operation and the complexity in simulation of this mixed signal design. It also provides a block level description of each block and explains how they are modeled and validated in the proposed methodology. The block wise validation procedure and top level system integration and testing applying SystemVerilog and co-simulation environment are also explained.

II. DPLL OVERVIEW

The main application of Phase Locked Loop (PLL)s are as frequency synthesizers or clock generators. A PLL acts as a feedback system comparing input phase with output phase and produces an output signal that is phase aligned with the input signal. However when it is used as pixel clock generator in analog interface of digital video display systems, it needs to phase align the output with a noisy and very low frequency horizontal synchronization signal (HSYNC). If proper phase aligning is not obtained, the displayed image will become blurry. Therefore in such applications the PLL must closely track the input clock signal. This paper introduces a Digital PLL (DPLL) design with fast tracking scheme which align the output feedback clock with noisy low frequency input reference signal (HSYNC). The DPLL finds application in Digital video display system such as LCD flat panel monitors, Plasma display panels, Video capture hardware etc. The HPLL is implemented in 65nm CMOS process. Table 1 shows the brief specification of the DPLL.

Table 1. Specification of the DPLL

	Corner Conditions			
Parameter	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage	1.1	1.2	1.26	V
Temperature range	-40		125	°C
HSYNC Frequency	20		300	KHz
CKOUT Frequency	76		650	MHz
Lock Time		45		µS
Power Dissipation		3.5		mW
Process	65			nm

In a digital video display system, the personal computer (PC) graphics card sends analog video RGB signals which will be accompanied by vertical synchronization clock (VSYNC) and horizontal synchronization clock (HSYNC). The DPLL takes the HSYNC as a reference clock to generate a high speed pixel clock. HSYNC is of low frequency with range of 30Hz to 100 KHz. The frequency multiplication ratio of the DPLL depends on the display resolution of the digital video display system and is always larger than 800 and can be up to over 2600. The DPLL provides a wide output frequency of range 76MHz to 650MHz working at a single 1.2V power supply.

Furthermore, here one of the main challenges is that the output pixel clock (CKOUT) is generated from noisy low frequency reference signal so the design needs to ensure that the output pixel clock is phase aligned to the HSYNC

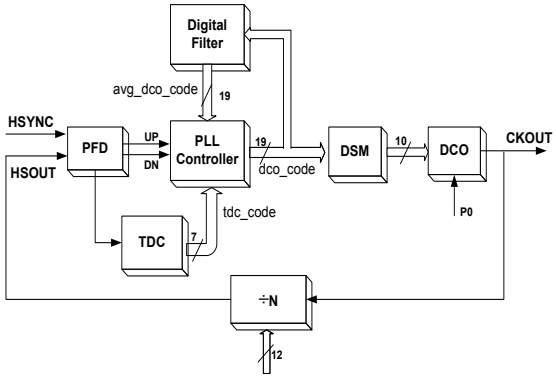

Figure 1. Block diagram DPLL

III. DESIGN OF DPLL SYSTEM MODULES

Figure 1 shows the block diagram of the DPLL. The DPLL is composed of a Phase Frequency Detector, Time-to-Digital Converter (TDC), a first-order delta-sigma modulator(DSM), digitally controlled oscillator (DCO), PLL controller, a digital loop filters (DLF) and a 12 bit programmable frequency divider (Prescalar).

The HSYNC is taken as the reference clock, and the HSOUT is the output pixel clock (CKOUT) divided by the frequency divider. The frequency multiplication ratios (N) for different video display resolutions are specified by the VESA display monitor timing standard. Based on different display standards we can externally program the 12 bit frequency divider.

A. Phase Frequency Detector (PFD)

The phase-frequency Detector is based on PFD used in [2]. The only difference is that, along with the UP and DN signal here additional digital logic is used to generate direction signals LEAD and LAG. After system reset, the PFD detects the phase and frequency error between the HSYNC and the HSOUT and based on that it outputs "UP" and "DN" control signals to the PLL controller. This UP and DN signal represents the time error information between the HSOUT and HSYNC. If HSOUT is leading HSYNC, then DN represents the time error information between them and LAG becomes high indicating the DCO to decrease the speed. Conversely, if HSYNC is leading HSOUT, then UP represent the time error information between them and LEAD becomes high indicating DCO to increase the speed.

PFD is modeled in verilog and can be easily tested for the functionality and logic conditions with verilog test benches. This is done with modelsim and other digital tools.

B. Time to Digital Converter (TDC)

TDC converts the error signal from PFD to digital bits. The TDC block consists of 2 Sub-TDC blocks and a TDC code selection block (Figure 2) for taking into account both positive and negative phase errors [7]. PFD's output signals are used to select the output of the sub-TDCs. Each sub-TDC block consists of a chain of delay generation circuit and T2B (thermometric to binary converter). The delay generation block is implemented using couple of inverters and delay flops where the delay of the couple inverters corresponds to the resolution of the TDC. If the HSYNC leads the HSOUT, the output of the #1 sub-TDC (tdc_code_lead) is selected as the "tdc_code". Oppositely, if the HSYNC lags the HSOUT, the output of the #2 sub-TDC (tdc_code_lag) is selected as the "tdc_code".

The validation of the TDC block is a bit difficult due to the presence of the delay elements. Modeling of the TDC also may not be accurate as the functionality the determined by the delay of cells. Actual standard cell libraries are included in the functionality validation to get the actual characteristics of the delay cells.

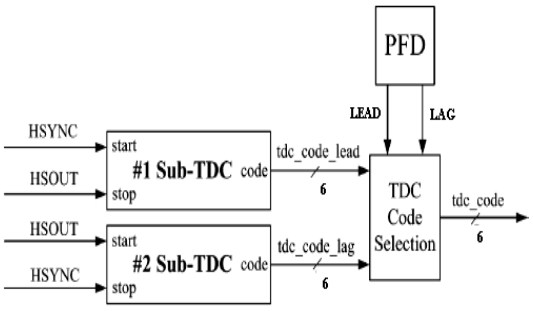

Figure 2.TDC top representation

C. PLL Controller and Digital loop filter

In the DPLL the controller and filter blocks are fully digital in nature [4]. The DPLL controller outputs a 19 bit dco_code to the DSM. The lock-in procedure of the DPLL controller is divided into four states: a coarse code search state, a fine code search state, a fractional code search state and a fast phase tracking state[5][6]. In the coarse code search state and fine code search state, the DSM is turned off, and the PLL controller adjusts the integral part of the DCO control code (dco_code[18:9]) with the PFD's output. Subsequently, the DSM is turned on to improve the equivalent resolution of the DCO. Then, the DPLL controller adjusts the fractional part of the DCO control code (dco_code [8:0]) to minimize the frequency error between the HSYNC and the HSOUT.

After frequency acquisition is complete, the DPLL controller enters the fast phase tracking state, and the phase error between the HSYNC and the HSOUT is quantized by the TDC, then the proposed fast phase tracking scheme is applied to reduce the phase error between the HSYNC and the HSOUT [8]. As a result, after the DPLL is locked, the phase error is minimized. After system is reset, the PFD detects the phase and frequency error between the HSYNC and the HSOUT. Then, it outputs "UP" and "DN" control signals to the PLL controller to indicate that the DCO's output frequency should be sped up or slowed down, respectively. When the PLL controller increases the DCO control code (dco_code), the DCO's output frequency is slowed down. Oppositely, when the PLL controller decreases DCO control code (dco_code), the DCO's output frequency is sped up. A binary search scheme is used in the PLL controller to reduce the lock-in time to search for the target DCO control code (dco_code). Therefore, when the PFD's output is changed from UP to DN or vice versa (shown as A in Figure.3), the search step is divided by 2 until the search step (Internal signal of PLL controller). is reduced to 1(shown as B in Figure. 3).

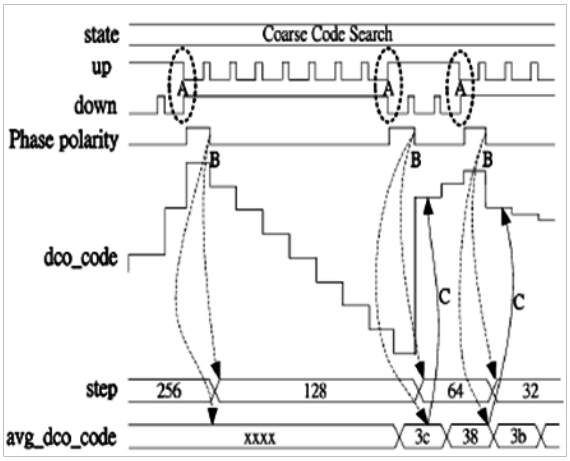

Figure 3. Timing Diagram in Frequency search

The reference clock (HSYNC) is very noisy in the digital video display system. Thus, in the DPLL architecture, a digital loop filter [9] is used to produce a baseline frequency control code (avg_dco_code). When the phase polarity is changed, the DPLL controller along with digital loop filter restores the baseline frequency control code (avg_dco_code) to the DCO control code (shown as C in Figure. 3) to reduce the jitter of the output pixel clock operation.

The flow chart of the proposed digital loop filter is shown in Figure 4. The proposed DLF accepts the DCO control code (dco_code) generated by the PLL controller. Then, it stores eight DCO control codes (C0 to C7) to generate a baseline frequency control code (avg_dco_code). Every time two new DCO control codes (CN1 and CN2) are received by the DLF, the DLF searches for the maximum and minimum values in C0 to C7, CN1 and CN2. Subsequently, the maximum and minimum values are removed and the remaining DCO control codes are then stored in to C0 to C7, thus the output of the filter represents the baseline average code avg_dco_code. Thus DLF helps in reducing the reference clock jitter effects of the noisy HSYNC.

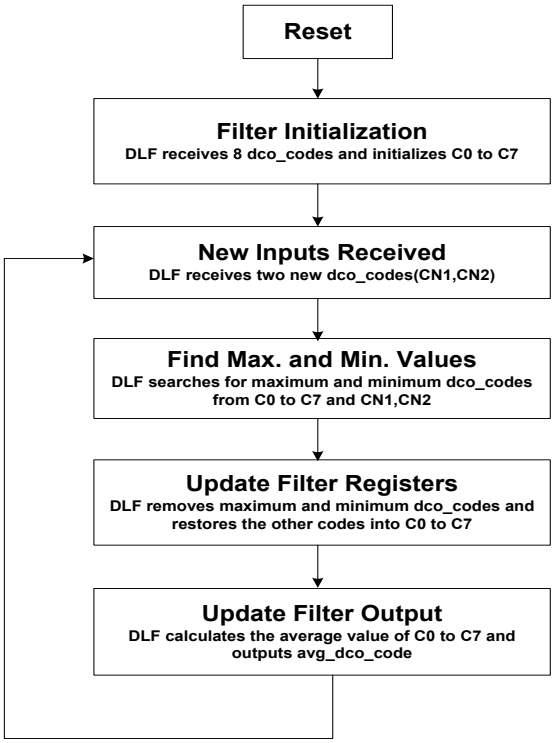

Figure 4. Flow chart of Digital Loop filter

The proposed digital loop filter quickly updates the baseline DCO control code for the PLL controller to track the target frequency. Therefore, the lock-in time of the DPLL is further reduced by the proposed DLF.

The validation of the complex controller and filter block across all test scenarios are very much time consuming with spice simulation. Here we use the SystemVerilog test benches and methodologies for the validation of the same.

D. Delta sigma Modulator (DSM)

After frequency acquisition is complete, the DPLL keeps tracking the phase error between the HSYNC and the HSOUT with TDC and DSM. In the DPLL, the output of the DPLL controller will be 19 bit, here 10 bit MSB of dco_code represents the integral code and 9 bit LSB represents the fractional code. The DSM converts the 19 bit avg_dco_code to 10 bit dco_code. In the frequency acquisition the integral code will be modified based on the output of the PFD by the PLL controller. After the frequency acquisition the time-to-digital converters are applied to quantize the phase error into digital codes. Subsequently, the compensation codes for the digitized phase errors are added to the fractional bits of the DCO control codes. Hence, the phase error is immediately compensated for by the DCO dithering scheme with a delta-sigma modulator (DSM).

E. Digital Control Oscillator (DCO)

The DCO receives the 10 bit control code [D<9:0>] from DSM as shown in Figure 5. The proposed DCO consist of a bias generator circuit, a Ring oscillator section and a Differential to single ended amplifier. The bias generator section consists of a Digital to analog converter (DAC) section which converts the input digital dco_code <9:0> from DSM to analog voltage thereafter generating appropriate bias voltage VBN and VBP by the bias section. Ring oscillator section is implemented using four stages of differential pair same as in [2] and a Differential to single ended amplifier is used to convert the dual small swing differential input to single output having rail-to-rail swing.

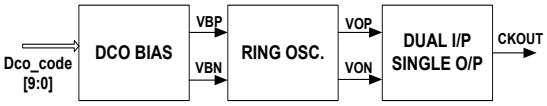

Figure 5. Block Diagram of DCO

Here the DCO is designed in such a way that the frequency range of the DCO can be changed based on external mode pin P0. Mode0 implies low frequency operation and mode1 implies high frequency operation.

This DPLL design uses an analog oscillator to ensure high linearity and frequency accuracy over PVT variations. The oscillator verilog/verilogA models are used in the initial functionality simulations. Models are replaced with actual spice netlist in co-simulation phase.

IV. SIMULATION RESULTS

The DPLL is done in 65 nm CMOS technology. Figure 6 shows the co-simulation simulation waveform of the DPLL. The use of binary search scheme along with fast tracking state of PLL controller minimizes the lock in time and phase error between HSYNC and HSOUT. The 12 bit programmable divider enables us to support different display resolutions such as XGA, SXGA, UXGA and WUXGA.

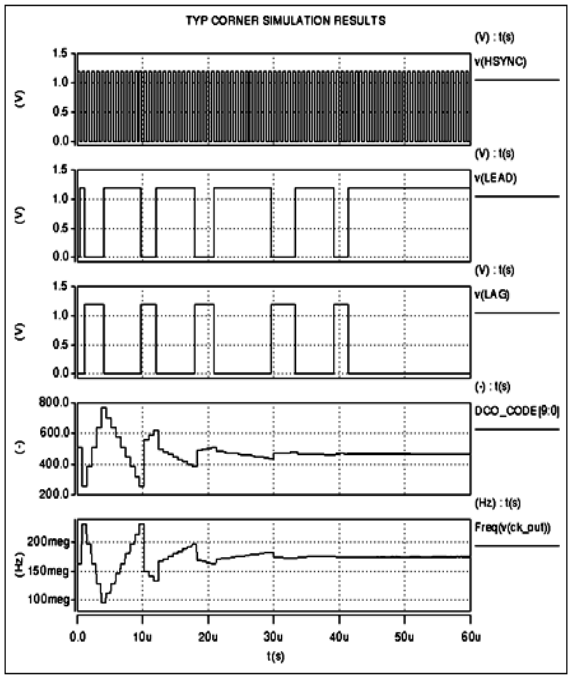

Figure 6. Simulation Waveforms

V. CONCLUSION

In the present work, a fast phase tracking DPLL for video pixel clock applications is implemented in 65nm CMOS technology. In order to overcome the simulation time overhead of the system, an effective mechanism using SytemVerilog and co-simulation environment is employed. This makes the system design and digital logic verification easy and hence reduces the design time considerably. The verification using SystemVerilog test environment ensures the circuit quality and co-simulation makes the system design less time consuming. The suggested mechanism can be applied for similar low frequency operation mixed signal sytems.

VI. REFERENCES

[1] Behzad Razavi, "Design of Analog CMOS Integrated Circuit", McGraw-Hill, 2001.

[2] Biju Viswanathan, Ramya Nair S. R., Vijay Viswam, Joseph J. Vettickatt, Kulanthaivelu R., Lekshmi S. Chandran, "4 GHz 130nm Low Voltage PLL Based on Self Biased Technique", vlsid, pp.330-334, 2010 23rd International Conference on VLSI Design, 2010.

[3] Anitha Babu, Bhavya Daya, Banu Nagasundaram, Nivetha Veluchamy, "All Digital Phase Locked Loop Design and Implementation", IEEE transactions on Magnetics, 2009.

[4] Ching-Che Chung, Member, IEEE, and Chiun-Yao KoTsung-Heng, "A Fast Phase Tracking ADPLL for Video Pixel Clock Generation in 65 nm CMOS Technology", IEEE Journal of Solid-state circuits, vol. 46, no. 10, pp. 2300-2311, 2011

[5] Robert Bogdan Staszewski and Poras T. Balsara, "All-Digital PLL With Ultra Fast Settling", IEEE Trans. on Circuits and Systems, 2007

[6] Ping-Hsuan Hsieh, Jay Maxey, and Chih-Kong Ken Yang, "A Phase-Selecting Digital Phase-Locked Loop With Bandwidth Tracking in 65-nm CMOS Technology", J. Solid-State Circuits, 2010.

[7] Senior Member, IEEE S.-Y. Lin and S.-I. Liu, "A 1.5 GHz all-digital spread-spectrum clock generator," IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 3111–3119, Nov. 2009.

[8] X. Chen, J. Yang, and L.-X. Shi, "A fast locking all-digital Phase Locked loop via feed-forward compensation technique," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 5, pp. 857–868, May 2011.

[9] S.-Y. Yang,W.-Z. Chen, and T.-Y. Lu, "A 7.1mW, 10 GHz all digital frequency synthesizer with dynamically reconfigured digital loop filter in 90 nm CMOS technology," IEEE J. Solid-State Circuits, vol. 45, no.3, pp. 578–586, Mar. 2010.

2014 DESIGN AND VERIFICATION DVCON CONFERENCE AND EXHIBITION EUROPE

Oct 14-15, 2014
Munich, Germany

Copyright Permission Agreement

SIGN AND RETURN by August 1, 2014
(PDF electronic or typed signature accepted)
EMAIL: jinnie.hinderscheit@ecsi.org

Proceedings of the Design & Verification Conference & Exhibition (DVCon) Europe – October 14-15, 2014

Accellera Systems Initiative (Accellera)/DVCon Europe desires to publish the paper, slides, video for the presentation below. Accellera/DVCon Europe desires to receive a limited, non-exclusive, non-transferable, royalty-free license, under Network Systems and technologies (P) Ltd 's copyrights embodied in the Licensed Material to copy and publish these materials on its website at: www.dvcon-europe.org and www.accellera.org

Title of Paper: An Effective Design and Verification Methodology for Digital PLL

Author's Name(s): Jobin Cyriac, Joseph J Vettickatt, Rajagopal P.C, Ramya Nair S. R, Biju Viswanathan

Network Systems and technologies (P) Ltd is the owner of all right, title and interest in and to certain text and figures in the paper, presentation slides and videos.

Company/Author retains all proprietary rights and copyright, such as patent rights, plus the rights to:

1. Reuse all or portions of the above paper in other works for personal use, for company use, for marketing purposes, for electronic distribution and for profit, with the exception that the Company/Author cannot submit or present the paper or presentation slides at another conference.
2. Reproduce, or have reproduced, the above paper provided the copies are not used in a way that implies Accellera/DVCon Europe endorsement of a product or service of an employer.

In exercising its rights under copyright, Accellera/DVCon Europe will make all reasonable efforts to act in the interests of the author(s) and employer(s) as well as in its own interest. In particular, Accellera/DVCon Europe requires that:

1. The consent of the principal author be obtained as a condition in granting permission to others to reproduce all or portions of the above paper for promotion or marketing purposes.
2. The consent of the undersigned employer be obtained as a condition in granting permission to others to reuse all or portions of the paper for promotion or marketing purposes.

In the event the above paper is not published by Accellera/DVCon Europe or is withdrawn by the author(s) before publication by Accellera/DVCon Europe, this agreement becomes null and void.

Authorized Signature

01-07-2014
Date Form Signed

Network Systems and Technologies (P) Ltd
Employer (If Work Was Performed During Service to Employer)

NETWORK SYSTEMS & TECHNOLOGIES (P) LTD. TECHNOPARK TRIVANDRUM PIN - 695 581