An Effective Design and Verification Methodology for Digital PLL

Biju Viswanathan, Rajagopal P.C, Ramya Nair S. R, Joseph J Vettickatt, Jobin Cyriac
Network Systems and Technologies Ltd, Kerala, India

INTRODUCTION

Introducing an effective simulation methodology to overcome the spice simulation time overhead of digital dominant, low frequency Digital PLL (DPLL). Here in this verification methodology for DPLL, the verification process is divided into two stages :

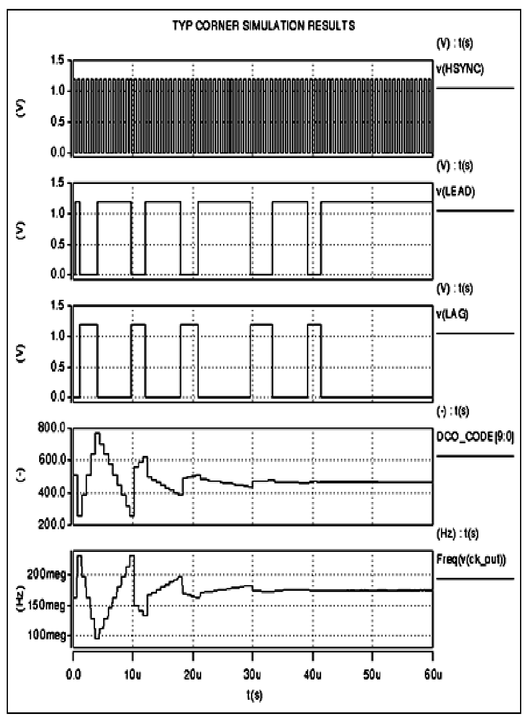
1. Digital blocks are designed and verified with stringent test cases using SystemVerilog and analog models. Analog blocks are verified using normal spice simulation.
2. Co-simulation environment is used for sign-off.

OBJECTIVES

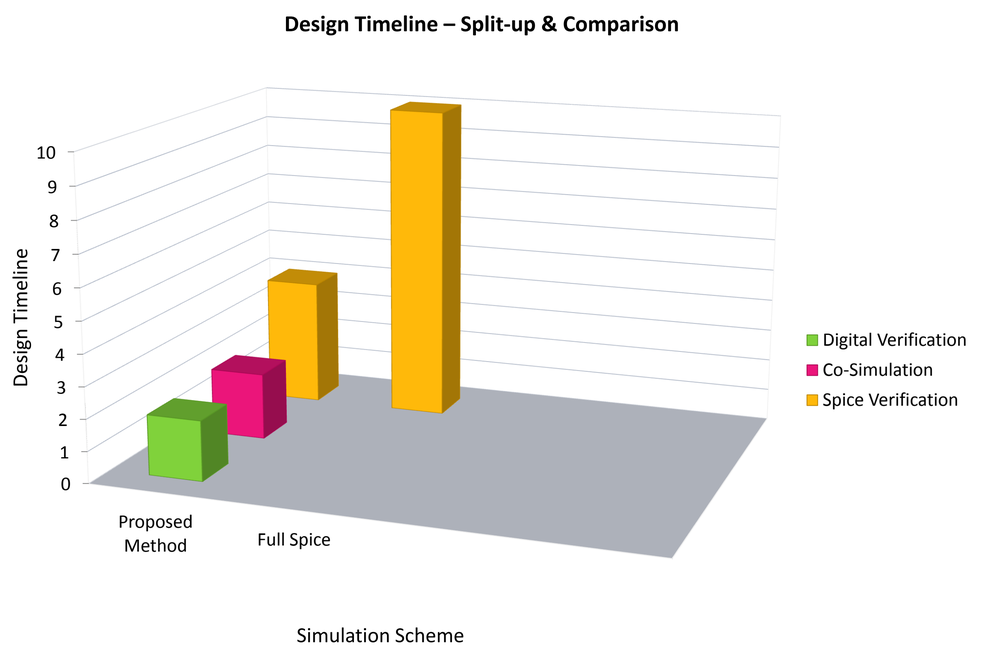
Main objective is to reduce the simulation challenges of low frequency analog mixed signal systems by an effective mechanism using SystemVerilog and co-simulation environment. This methodology reduces the simulation effort to 1/3rd of the actual spice simulation effort. Also it enables the designer to make the design fool proof. The DPLL loop consists of almost 80% digital components. It is cumbersome to analyze the entire loop using spice simulation for loop analysis. Even the functionality confirmation of the loop is time consuming as the system operates over a very wide range of division ratios (N). This practical simulation issue is addressed by the modeling of analog systems in the initial stages and by co-simulation in the advanced stage of system design.

OBSERVATION

- Reduces the simulation timeline significantly
- Can be adopted to a wide class of design which has analog & Digital blocks involved
- Coverage driven constraint random verification
- Modeling capabilities of SystemVerilog is adopted.



OBSERVATION



CONCLUSIONS

In order to overcome the simulation time overhead of the low frequency DPLL systems, an effective mechanism using SystemVerilog and co-simulation environment is employed. This makes the system design and digital logic verification easy and hence reduces the design time considerably. The verification using SystemVerilog test environment ensures the circuit quality and co-simulation makes the system design less time consuming. The suggested mechanism can be applied for similar low frequency operation mixed signal systems.

REFERENCES

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NeST Software
ENGINEERING ENDURANCE
NeST Towers, Plot No.73 & 74,
Technopark Campus, Trivandrum
Tel: +91 471 2527441 Fax: +91 471 2700442
vlsi.info@nestgroup.net





biju.viswanathan@nestgroup.net;rajagopal.pc@nestgroup.net;ramya.nair@nestgroup.net;joseph.vettickatt@nestgroup.net;jobin.cyriac@nestgroup.net