AMS Verification in a UVM Environment

Dr. Silvia Strähle

accellera SYSTEMS INITIATIVE

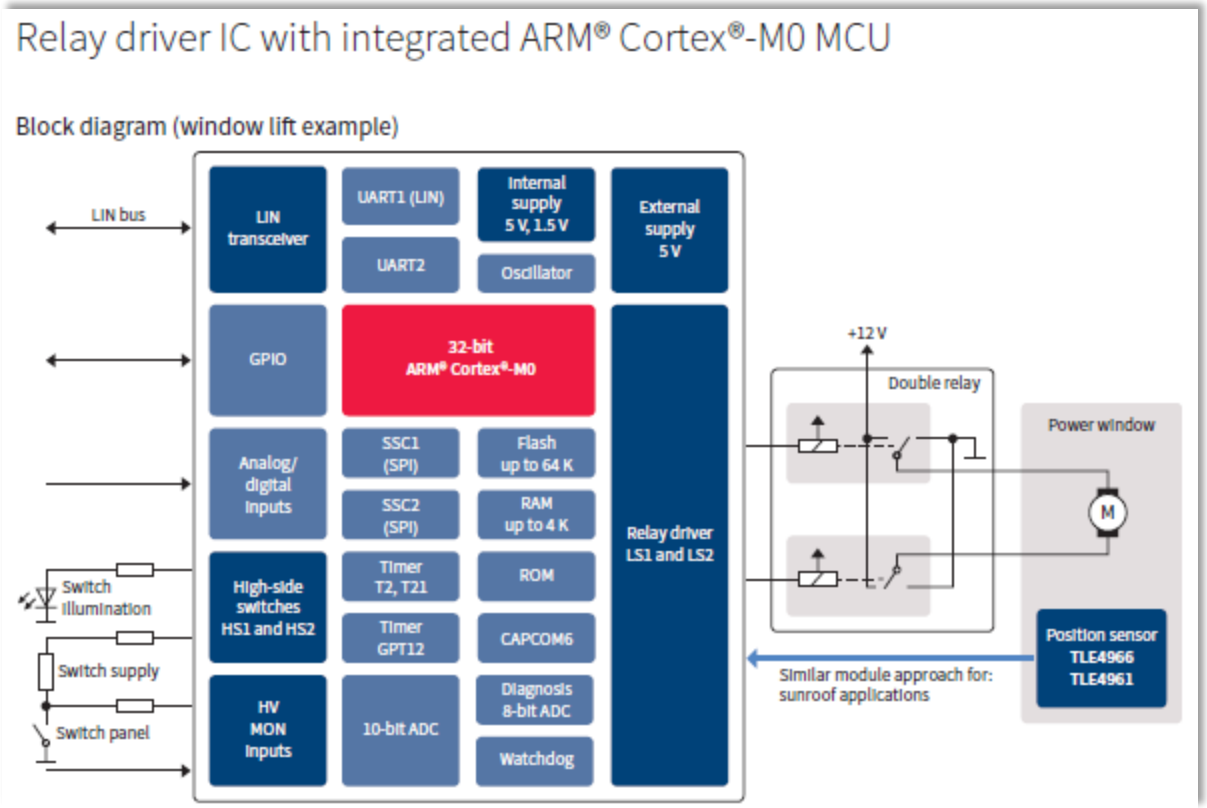
2016 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

Outline

- Introduction
- Pre-Silicon Verification Strategy
- Universal Verification Methodology (UVM) Setup
- UVM Extension for AMS Simulation
- UVM AMS Tests
- Summary

Introduction

Infineon Automotive Embedded Power IC's



Source: http://www.infineon.com/cms/de/product/power/motor-control-and-gate-driver-ics/automotive-embedded-power-ics-system-on-chip/relay-driver-ic-with-integrated-arm-cortex-m0/channel.html?channel=5546d4614815da88014859b49c9317b7

How to ensure that Embedded Power IC fulfills

Specification

?

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Pre-Silicon Verification Strategy

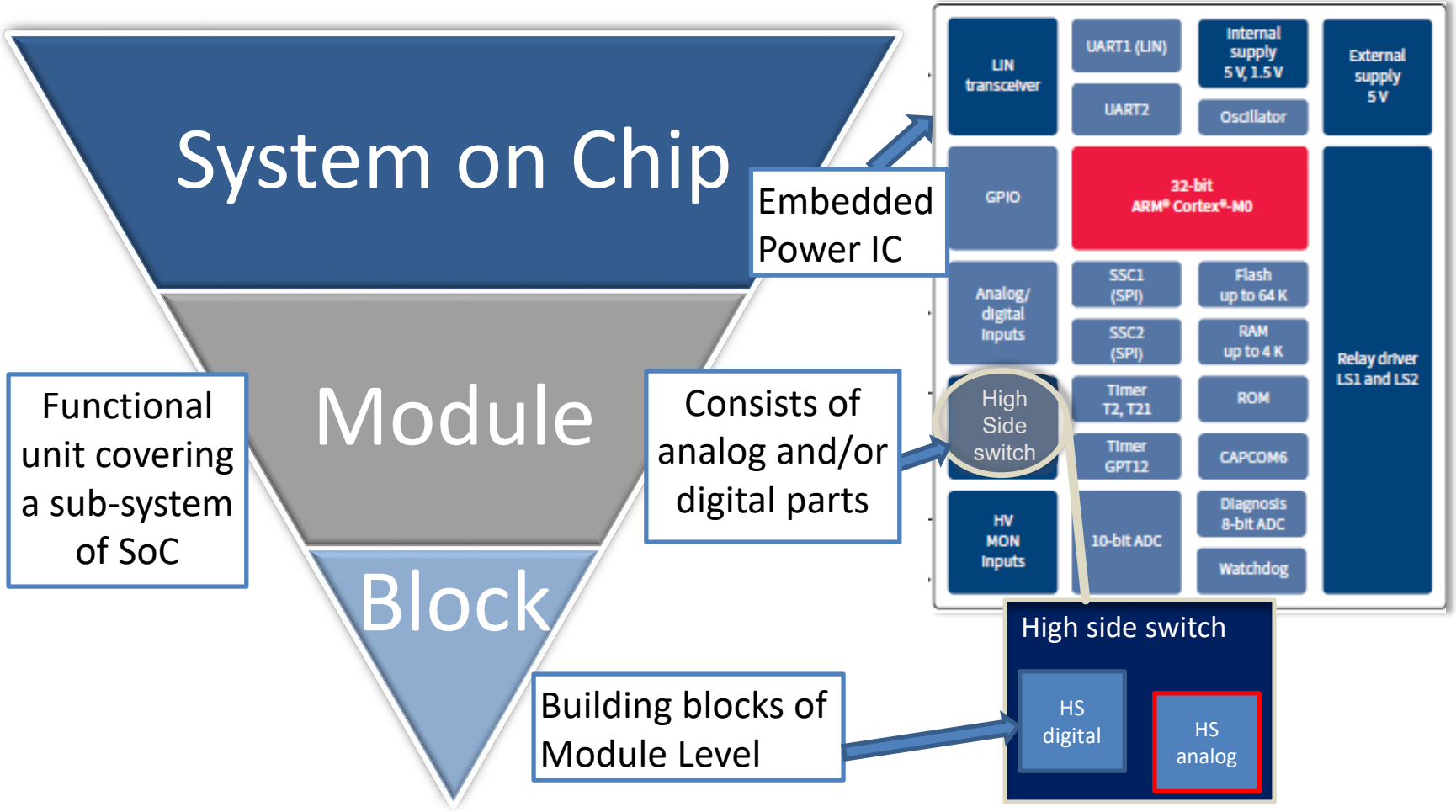
- Requirements Driven Verification
  - Customer Requirements
  - Product Requirements
  - Design Specific Requirements

  } Overall Requirements
- Each Requirement needs to be verified at least on one Verification Level
- Verification Rules
  - Verify on lowest level possible
  - Reuse of Verification IP

  } Motivation to extend UVM to UVM AMS

Pre-Silicon Verification Levels

Source: http://www.infineon.com/cms/de/product/power/motor-control-and-gate-driver-ics/automotive-embedded-power-ics-system-on-chip/relay-driver-ic-with-integrated-arm-cortex-m0/channel.html?channel=5546d4614815da88014859b49c9317b7



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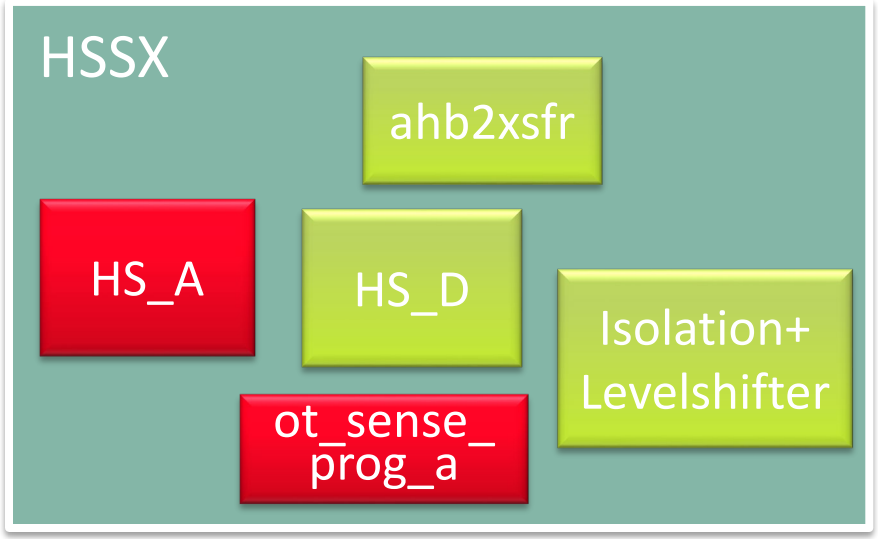
Module High Side Switch

- Analog blocks
  - High Side analog core
  - Temperature sensor



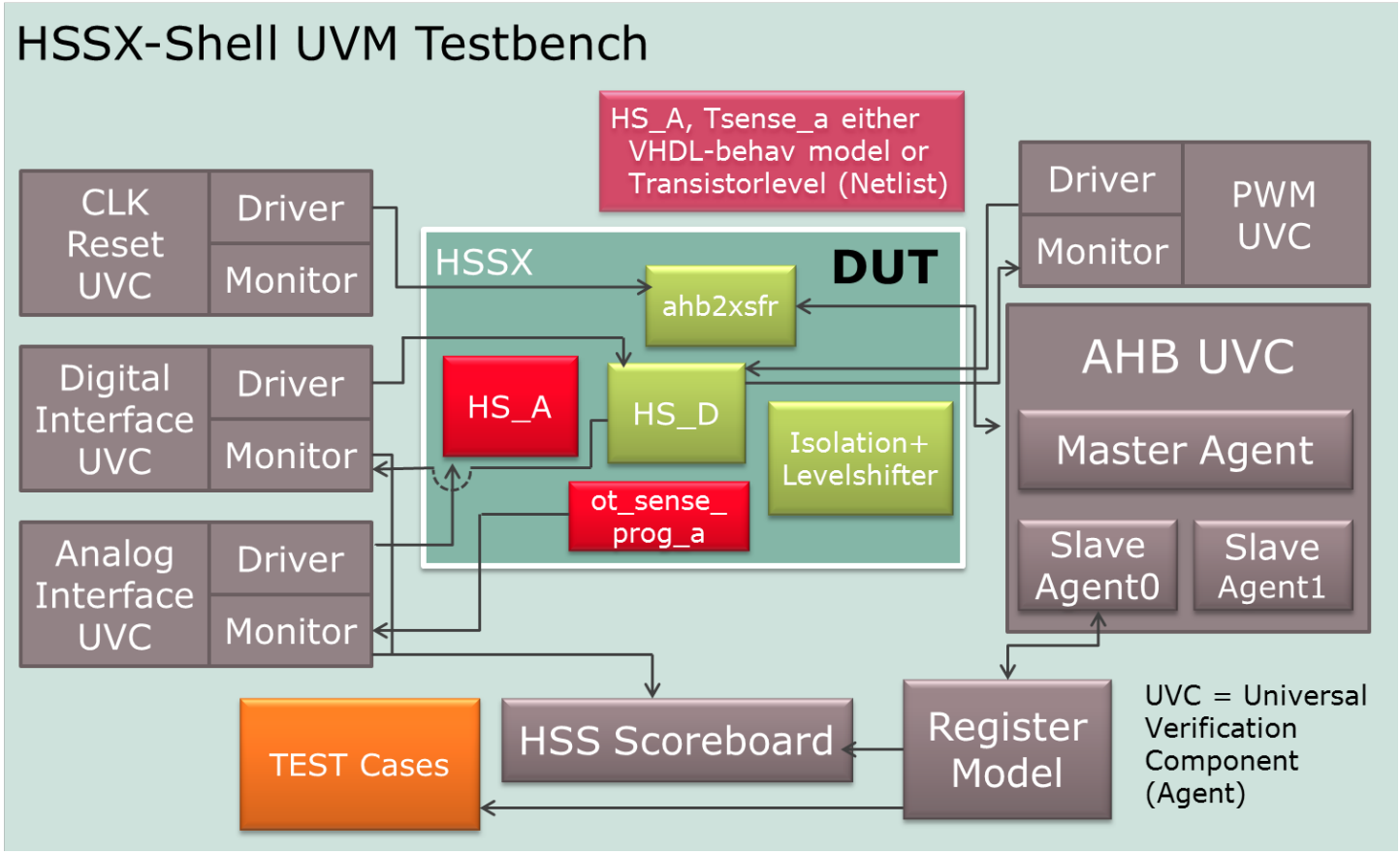
- Digital blocks
  - High Side digital core
  - Registers
  - Isolation and Levelshifter cells
  - AHB = Advanced High-performance bus (ahb2xsfr)

Features of High Side Switch

- The High Side Switch can drive external loads e.g. LED
- Selectable slew rate control
- Overcurrent detection for 3 different current threshold
- Over-temperature detection
- Digital configurable filter stages
- SFR Register to store values
- Test features

UVM Environment

Verification Components



AHB = Advanced High-performance bus

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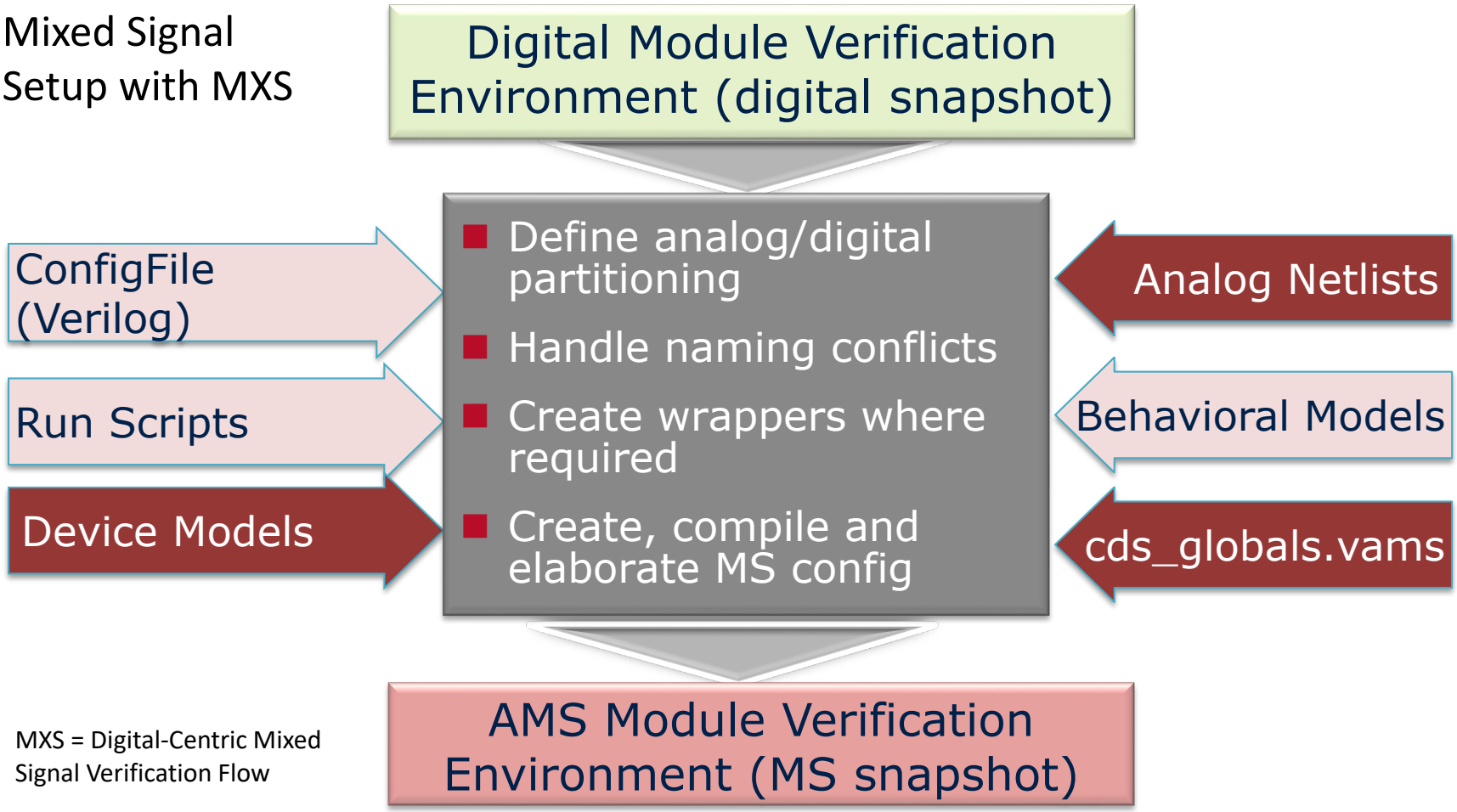
UVM Extension to AMS

Mixed Signal Setup with MXS



MXS = Digital-Centric Mixed Signal Verification Flow

Configure AMS View

Digital Configuration
hs_common_tb_top #testbench top level

```
inst_hss    #DUT
  i_hss_ahb_shell   #AHB Bus
  i_hss_d_shell     # Digital Design
  i_hss_a_shell     # Analog Design + ISO Cells
    i_hs_a_top    # Verilog Wrapper
      i_hs_vhd    # VHDL config for VHDL behav model
```

Mixed Signal Configuration
hs_common_tb_top #testbench top level

```
inst_hss    #DUT
  i_hss_ahb_shell   #AHB Bus
  i_hss_d_shell     # Digital Design
  i_hss_a_shell     # Analog Design + ISO Cells
    i_hs_a_top    # VerilogConfig: i_hs_a_top is a wrapper
      i_hs_ams    # verilog ams netlist of hs analog block
        `include hs_tb_ms.inc.vams  # access to analog
```

Include File:
Define external loads:
e.g. Resistor, Capacitor

Include file
hs_a_tb_ms.inc.vams

```
`include "disciplines.vams"
`include "userDisciplines.vams"

parameter extern_load_res = `EXTERN_LOAD_RES;

//######## External circuitry for  High Side analog  part  ######################
 capacitor #(.c(6.8n)) C_hs    (hs_av_o, inh_lSup_GND_A);
 resistor #(.r(extern_load_res)) R_load1   (hs_a_inst.hs_av_o, hs_a_inst.inh_lSup_GND_A);
//######## end  ###################################
```

Variable for param extern_load_res

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UVM AMS Test

The AMS Tests cover critical analog behavior which is not modelled in detail in behavior models

- Testcases
  - Slewrate Control for 3 different slewrates
  - Overcurrent detection for different thresholds
  - Overtemperature detection for different temperature thresholds

AMS Extension – slew rate test

```
`ifdef MIXED_SIGNAL
// check if high side enabled and set to on
 if (vif.hs_en === 1'b1) && (vif.hs_on === 1'b1)) begin
     hs_av_o_out_r = $cds_get_analog_value(hs_av_o_signal);

// Get value if hs_av_o is in the range of 20% output voltage
     if ((hs_av_o_out_r > hs_20_1) && (hs_av_o_out_r < hs_20_2)) begin
        hs_av_o_out_r20 = hs_av_o_out_r;
        hs_av_time_r20  = $realtime;
      `uvm_info(get_type_name(), $sformatf("hs_av_o_rise 20: Voltage is
                              %9.7f V at time %t \n",  hs_av_o_out_r20, hs_av_time_r20), UVM_NONE);
     end
// Get value if hs_av_o is in the range of 80% of the output voltage

// Calculate slew rate
 delta_voltage_r = (hs_av_o_out_r80 - hs_av_o_out_r20);
 delta_time_r = (hs_av_time_r80 - hs_av_time_r20)*1e-3
 tmp_slew_rate_r = ((delta_voltage_r) / (delta_time_r));

// check if slew rate is within defined limits for respective slew rate chosen
if (vif.hs_srctl_sel===2'b00) begin
   if((tmp_slew_rate_r > normal_slew_rate_min) && (tmp_slew_rate_r < normal_slew_rate_max))  begin
      check_slew_rate = 1'b1;
   end
 `endif   ## Mixed_SIGNAL
```

Only activated in AMS case

Scoreboard

Measure analog Voltage

Check which Slew Rate selected

Check spec range

AMS Extension – Overcurrent test

```
`ifdef MIXED_SIGNAL
// check overcurrent
if($cds_analog_exists(hs_av_o_signal) && (vif.hs_en === 1'b1) && (vif.hs_on === 1'b1)) begin
      hs_av_o_i = $cds_get_analog_value(hs_av_o_signal,"flow");

       case (vif.hs_oc_sel)
              2'b00: begin
                   if  (-hs_av_o_i*1e3 > hs_iocth0) begin
                   check_oc = 1'b1 ;
                   hs_iocth_tmp = hs_iocth0;
                   end
             end
             2'b01: begin
                 if  (-hs_av_o_i*1e3 > hs_iocth1) begin
                 check_oc = 1'b1 ;
                 hs_iocth_tmp = hs_iocth1; end
              end
        endcase
     if(vif.hs_oc_is !== 1'b1) begin
    `uvm_error(get_type_name(), $psprintf("hs_av_o Overcurrent %9.7f is out of selected threshold %3.1f hs_oc %d hs1_oc_tfilt_sel
%2d", hs_av_o_i*-1e3, hs_iocth_tmp, vif.hs_oc_is, vif.hs1_oc_tfilt_sel ))
    end
 'endif   ## Mixed_SIGNAL
```

Only activated in AMS case

Measure analog current

Check which Overcurrent threshold selected

Check if overcurrent limit exceeded

Scoreboard

AMS Extension – Overtemperature test

Temperature value is passed into the setup file:
"simulator options temp=TEMPVAL tnom=27"

TEMPVAL set to 160°C to get OT event

Scoreboard

```
task ifx_hss_analog_monitor::check_overtemperature();
`ifdef MIXED_SIGNAL
//check overtemperature
```

check if analog signals exist; measure Overtemperature output

```
if($cds_analog_exists(ad_ot_signal) && $cds_analog_exists(hs_av_o_signal) begin
    ad_ot_out = $cds_get_analog_value(ad_ot_o_signal);
```

check if Overtemperature is detected ad_ot_out > 0.8V

```
    if (ad_ot_out > 0.8) begin
    #500;
        hs_av_o_out_ot = $cds_get_analog_value(hs_av_o_signal);
        if (hs_av_o_out_ot < 0.3) begin
      check_ot_shutdown = 1'b1;
        end
    if((check_ot_shutdown) !== 1'b1) begin
      `uvm_error(get_type_name(), $psprintf("thermal shut down failed")
    end
  end
```

check that high side is shutdown

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Summary

- Achievements
  - ✓ Reuse of UVM testbench from “digital verification”
  - ✓ AMS extensions in UVM improves accuracy in module level verification
  - ✓ Increased confidence on the accuracy of the results

- Establish UVM – AMS
  - Further extend our UVM environment toward AMS
  - Improve setup and regression on AMS

Outlook

- Establish UVM – AMS
  - EDA vendors should be encouraged to make AMS Setup straightforward in UVM
  - Extend SystemVerilog language toward analog measures
  - Develop IP Libraries with AMS UVC

Questions

Finalize slide set with questions slide