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AMS Verification in a UVM Environment

Dr. Silvia Strähle, Infineon Technologies, Neubiberg, Germany (silvia.straehle@infineon.com)

***Abstract* — A verification environment based on Universal Verification Methodology (UVM) is set-up to verify the requirement defined in specification of a Mixed-Signal module. Universal Verification Methodology is chosen to ensure coverage. But also the reuse of verification IP for other modules and on System on Chip Level verification is an important aspect. Most of the requirements are verified in a configuration where the analog design of the module is represented by a behavior VHDL model. To verify specific requirements like over-temperature and current detection or feedback loops between analog and digital design, behavior models are not accurate enough. To cover those requirements the behavior model is replaced by the respective transistor-level netlist. As a consequence an Analog-Mixed-Signal simulator (AMS) is required. In this paper it is shown how the UVM Environment is extended to verify analog quantities like voltage and currents or influence of temperature.**

Keywords* — *AMS, Pre-Silicon Verification, UVM, Mixed-Signal

I. Application

Infineon Technologies develops System-on-Chip Products for Automotive Applications. For example products to drive electrical motors for window lift, electrical fans or pumps in cars. All required functions are integrated on a chip. ARM core, NVM, Flash, Watchdog, ADC's, Voltage Regulators, High Side Switches, Linear-Bus or Gate-driver are integrated on a single chip. More than one thousand of requirements need to be verified to ensure that the chip is fully functional.

II. Motivation

To ensure that the defined requirements and features of the products are correctly implemented a Requirements-Driven Verification Flow is setup. First it is distinguished between Pre-silicon and Post-silicon verification [1]. The Pre-silicon verification is based on simulation, emulation and formal verification. Pre-silicon verification is applied before any masks written or silicon is produced in the fab. Post-silicon verification or validation is based on measurements. In this paper the focus lies on Pre-silicon verification based on simulation.

In Pre-silicon verification we distinguished further levels:

- System on Chip Level
- Module Level
- Block Level

System on Chip Level (SoC) is defined as the level where all functions are integrated on a single chip. This means that ARM core, Memories, Flash, Watchdog, analog digital converters, voltage regulators, linear bus, high side switch and other blocks are integrated on one design. **Module Level** is defined as functional unit like High Side Switch combining analog and digital design including registers and design for test (DFT) features. **Block Level** is the building block of a Module.

Each requirement leads to one or more verification tasks being defined in the verification plan. It is also considered at which level (Post-, Pre-Silicon, SoC, Module or Block Level) the verification takes place.

The following rules are defined to decide at which level a verification task will take place:

- Each verification task needs to be covered by at least one level
- Verify the respective task at the level where it could be done most effective; in most cases it is the lowest level possible.
- Reuse of verification IP

In this paper the verification of a Mixed Signal High Side module is taken as an example. The module consists of an analog part, a digital part including isolation, levelshifters, and registers. Most parts of the verification tasks related to the High Side Switch can be verified on **Module Level**. The electrical characteristics of the analog part are verified on **Block Level**. Functions triggered from **System Level** like wakeup from a power down mode are verified on **System on Chip Level**.

The UVM approach is chosen to achieve respective coverage. Regression can be setup since Electronic Design Automation (EDA) vendors have tools in place to setup and run UVM regression. Reuse of the module verification IP on the System-on-Chip level verification is a further advantage.

UVM regression is based on a digital simulator. Therefore the analog part of the High Side Switch is described as VHDL behavior model. Unfortunately analog behavior could not be modelled very accurate in VHDL, especially if external circuitry, as capacitors, resistors or inductors, is required for the analog block as output load. To overcome the drawback the idea is to replace the analog behavior model with its respective transistorlevel netlist.

The "classical" UVM Environment is extended to run an AMS Simulator. But also drivers and monitors need to be extended. To access analog quantities like voltage or currents respective simulator function calls are used. With this approach the reuse of the UVM-Testbench towards AMS simulation is also obtained which is one of our verification rules.

III. UVM ENVIRONMENT

The UVM Environment introduced in this paper is setup to verify a High Side Switch Module. The design under test (DUT) which is the High Side Switch Module is partitioned into 5 main blocks (Figure 1).

Two analog blocks:

- High Side analog core
- Temperature sensor

and 3 digital blocks

- Digital core of the High Side Switch
- Registers
- Isolation and levelshifters.

The Device under test (Module Top-Level) is RTL and called "Digital on Top". In pure digital verification analog blocks are represented by VHDL behavior models. In the AMS simulation the behavior models are replaced by the respective transistorlevel netlist.

In the bullet list below several features of the High Side Switch are listed:

- The High Side Switch can drive external loads e.g. LED
- Selectable Slewrate Control
- Overcurrent detection for 3 different current threshold
- Overtemperature detection
- Digital configurable filterstages
- SFR Register to store values
- Design for Test Features

To verify the features and requirements listed above, different Universal Verification Components (UVC's) are developed and used in the UVM Environment.

- AHB (Advanced High-performance bus) UVC
- Clock and Reset UVC
- Digital Interface UVC
- Analog Interface UVC
- PWM UVC

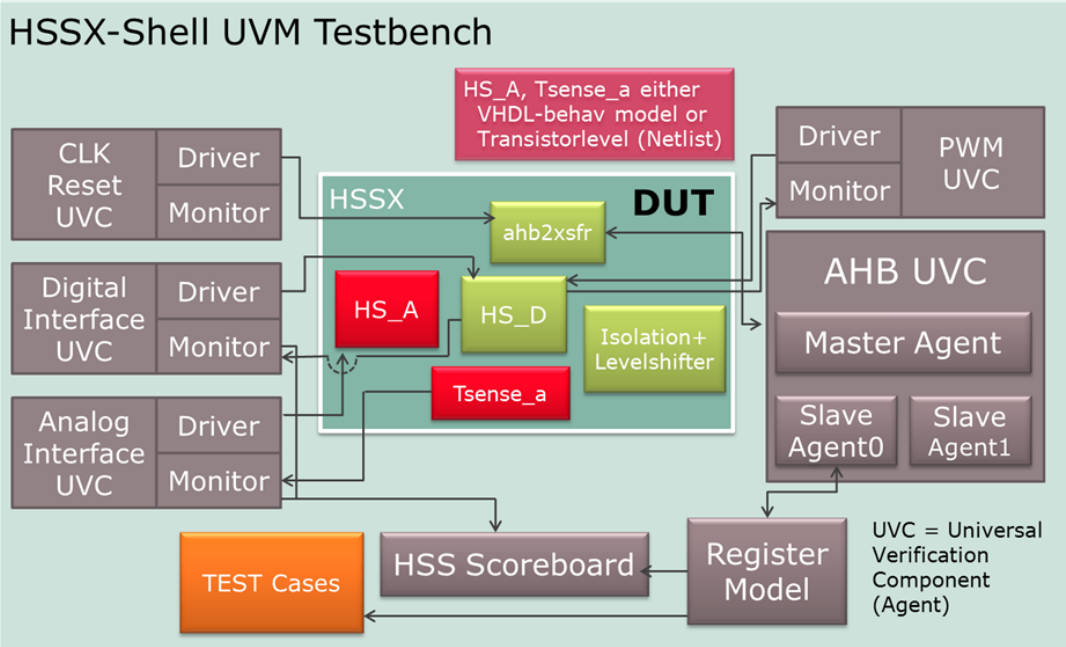

Figure 1 UVM Environment for Module Level (High Side Switch)

The AHB UVC is a Verification IP which is used to access SFR Registers. The Clock and Reset Interface UVC provides respective System Clock and Reset. The Digital Interface UVC drives the High Side digital block. To cover analog behavior an Analog Interface UVC is built to drive and monitor the analog blocks. In the Scoreboard the respected results are checked.

Test cases are setup to verify specified features and requirements. Below a small extraction of the tests is listed. Some of them cover digital functions but of course examples are taken with typical features affecting the analog part.

- Register_Test - includes reset, write and read access
- Slew Rate Test - Set different slew rate via register and verify the slew rate
- OT Detection Test -Overtemperature detection and shutdown of the High Side Switch
- OC Detection Test - Overcurrent detection and shutdown of the High Side Switch

The features overcurrent and overtemperature detection as well as slew rate measurements of the output signal are analog properties. An accurate modelling in the VHDL behavior model is not really possible. For these test cases the UVM environment is extended towards AMS simulation and the VHDL behavior model is replaced by the transistorlevel netlist.

IV. UVM Environment Extension to Analog-Mixed-Signal Simulator

To verify the accurate analog behavior of a Mixed-Signal Design the transistorlevel netlist for the analog block is mandatory. As depicted in Figure1 the analog blocks are marked in red. The VHDL behavior models are replaced with the transistor level netlist to simulate the accurate analog design.

The AMS Verification Flow depicted in Figure 2 is developed specifically for digital on top DUT's by the Infineon DES Department, responsible for our Design Flow.

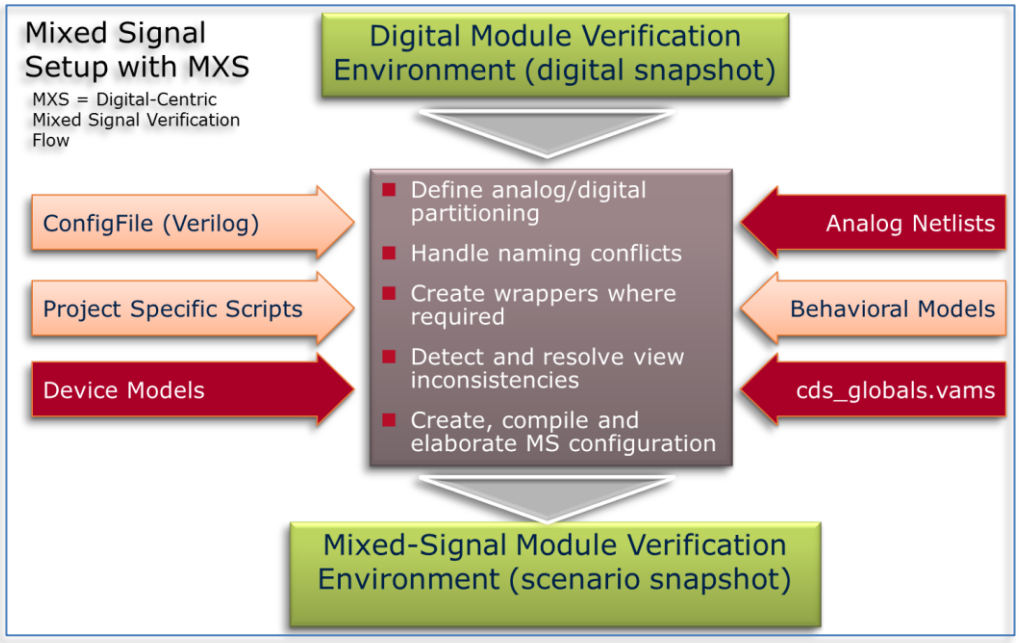

Figure 2. Setup to replace VHDL behavior model with a transistorlevel netlist + other files for Mixed-Signal setup

Before starting the verification with an AMS simulator a UVM setup, running with a digital simulator, is mandatory. The starting point is the elaborated digital snapshot as depicted in Figure 2.

The replacement of the VHDL behavior model with respective transistorlevel netlist is done by changing the configuration. The transistorlevel netlist is bound instead of the behavior VHDL model. After a recompile and elaboration step a "scenario snapshot" is generated. Transistorlevel netlists are provided in Verilog AMS language. Verilog AMS fits easier to the VHDL and SystemVerilog language than spice like netlists.

In Figure 3 the difference of configuration for digital and AMS Simulation is illustrated. On the left hand side of Figure 3 the design hierarchy for pure digital is listed. The testbench named hs_common_tb_top is the top level. The next deeper hierarchy level is the DUT (inst_hss). The DUT includes the AHB Bus (i_hss_ahb_shell), digital High Side (i_hss_d_shell) and analog High Side (i_hss_a_shell) part. The VHDL behavior model is located in the analog part. Between VHDL and SystemVerilog language boundary a Verilog Wrapper is introduced.

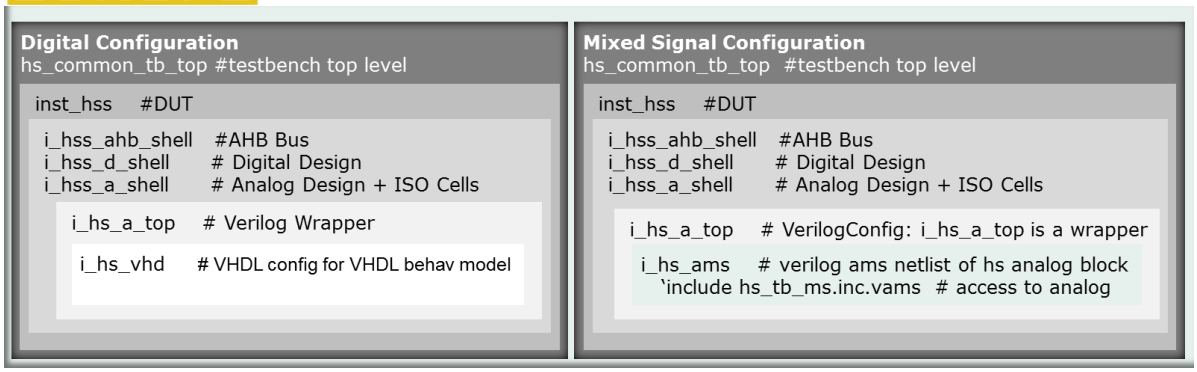

Figure 3. Configuration for digital and AMS Simulation

The AMS design hierarchy is listed on the right hand side of Figure 3. The upper hierarchies like testbench and next hierarchy levels stay the same and can be reused. Only the analog part needs to be replaced. The Verilog wrapper is replaced by the VerilogVams wrapper (i_hs_a_top). In the VerilogVams wrapper the Verilog AMS transistorlevel netlist is instantiated. In addition an include file (hs_tb_ms.inc.vams) is loaded. In the include file external loads are defined and connected. For the High Side Switch a capacitance and resistor is added to represent the external load. The High Side Switch has currents as inputs. In the level of i_hs_a_top the currents are of datatype real for digital setup and of datype wreal in AMS Setup. In the include file the currents are defined as quantity electrical. A transition from wreal to electrical is implemented as well.

The simulator options of the analog simulator are defined in amsControl.scs file. The temperature value is defined as a variable which can be set for the AMS simulation. Changing of the temperature value is needed for the overcurrent testcase.

V. Results from UVM AMS Verification

Testcases being verified are already listed in chapter III. Register default settings, reset, read and write access, are verified with the digital setup including the behavior VHDL model. In UVM AMS, where the transistorlevel netlist is used, the focus lies on testcases with analog functions like slew rate, overcurrent and overtemperature, where accurate analog values of voltages and currents are of importance. In case of overtemperature a change in analog simulator control file is required. While transistorlevel netlist is used an external load is required. The external load is represented by a capacitor and resistor connected between output signal hs_av_o and ground.

Most of the UVC's can be reused for AMS Verification. The UVC's to write and check register status can be used the same way in AMS simulation. Changes are needed in the analog Interface UVC and Scoreboard.

A. Slew rate Test

In testcases where slew rates and overcurrent detection are checked an access to the analog quantities "voltage" and "current" is implemented. Mixed signal simulators provide functions ($get_analog_voltage) to measure voltage and current.

This function is implemented in the scoreboard to measure voltage or current when a certain event is triggered (Figure 4). The function is only valid when compilation and simulation is done with the AMS option therefore the directive 'ifdef MIXED_SIGNAL … 'ENDIF is necessary.

In the slew rate testcase each of the 3 different slew rates are set in the UVM Slew rate sequencer via respective register. In addition the High Side Switch is enabled and switched on and off. The voltage on the output hs_av_o is measured in case High Side is enabled and on. The value of the voltage and time is stored in a variable when 20% and 80% of output signal is reached. From stored values in respective variables the slew rate can be calculated. Then it is compared to the expected value of the slew rate, set in the register. If it is out of range a UVM error is triggered and a message is written out.

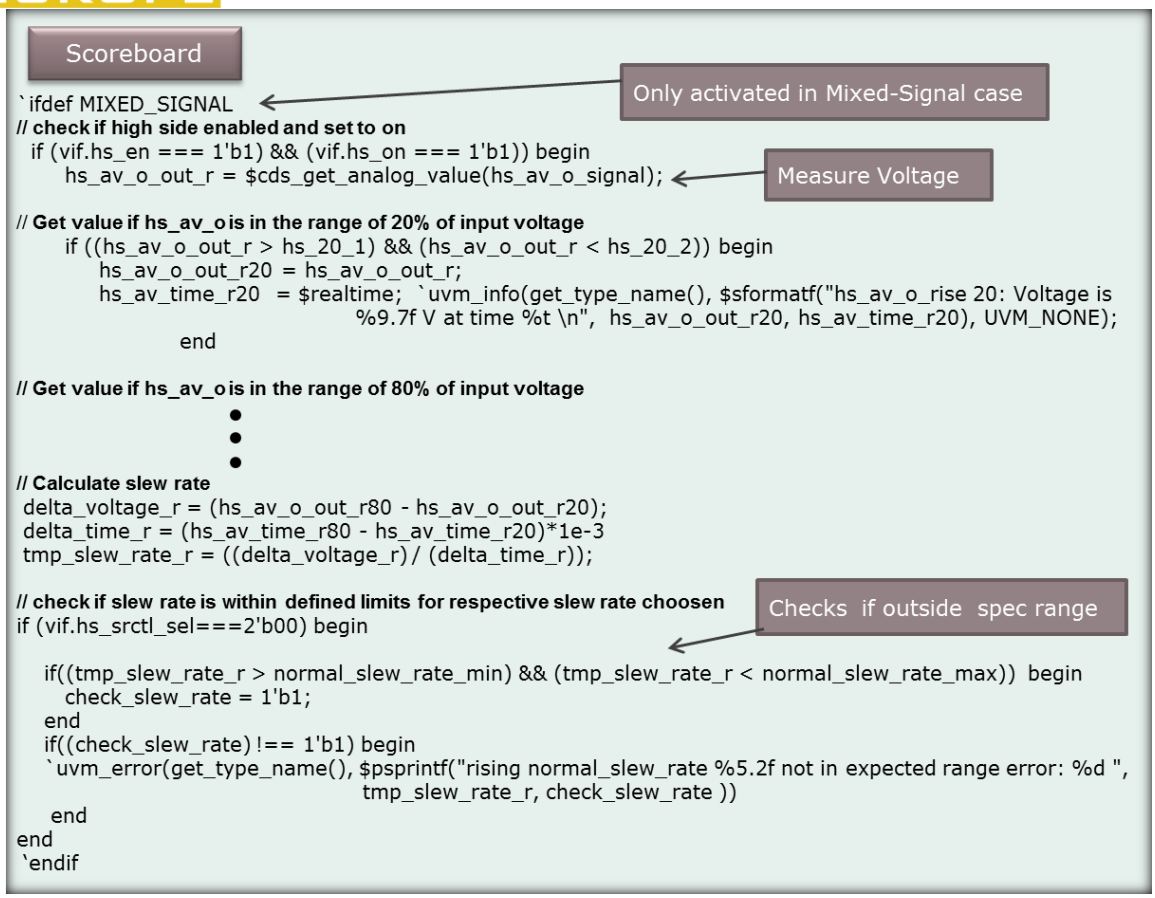

Figure 4. Implementation in the Scoreboard to measure analog voltage and slew rate calculation

B. Overtemperature Test

A further test is overtemperature detection. As depicted in Figure 1 a temperature sensor is part of High Side Switch module. This temperature sensor detects if the temperature extends a certain threshold and the signal ot_detect rises to '1'. If overcurrent condition is detected the High Side Switch is turned off after a defined filter time and respective status flag is set to '1'.

In analog simulators the temperature is a simulator option named "temp". By default this value is set to 27°C. To overwrite the value for "temp" a variable "TEMPVAL" is defined. When starting the overtemperature detection test we pass for instance 180°C to the "TEMPVAL" variable which is defined in the amsControl.scs file (see also chapter IV). We are aware that with this approach it is not possible to simulate thermodynamic heating effects, but high temperature can be set and overtemperature detected. It is checked that the overtemperature flag is rised and that the High Side Switch is turned off. Although the High Side Switch is turned off the overtemperature signal ot_detect stays at '1' since temperature stays at 200°C which is a limitation of this setup.

C. Overcurrent detection Test

It is possible to detect four different overcurrent thresholds (25mA, 50mA, 100mA, and 150mA) and turn off the High Side Switch module after a certain filter time, if respective threshold is exceeded. The thresholds are selected by setting respective control register. The first challenge is to generate respective overcurrent conditions. To do so the external load of the High Side Switch is varied to generate short circuit overcurrent. To enforce the different overcurrent values the resistor connected between output signal hs_av_o and ground is changed. As already described in chapter IV the external load is part of the include file hs_tb_ms.inc.vams (Figure 5). The resistor is defined as parameter "extern_load_res" with a variable "EXTERN_LOAD_RES".

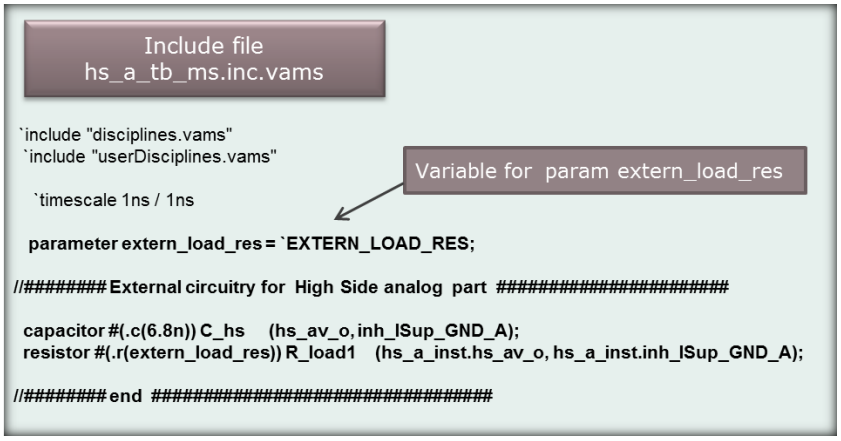

Figure 5. Include file for analog part of the High Side Switch,
where external load circuit is defined

The variable "EXTERN_LOAD_RES" is parsed while starting the simulator. Depending on the resistor value a respective overcurrent is generated.

In the Scoreboard a check is implemented to detect the overcurrent. An overcurrent shorter than 8us is allowed since it does not damage the High Side Switch. The output current of the High Side "hs_av_o" is measured in case the hs_av_o_signal exists, and in case High Side is enabled and on (see Figure 6). Next it is compared to the selected overcurrent threshold hs_oc_sel="00" which is 25mA.

If it exceeds the respective overcurrent limit (25mA) also after filter time "oc_fil_time", which is 8us, then the "hs_oc_is" signal is still "1" a UVM error is triggered and a message is written out. The same sequence is implemented for the other overcurrent thresholds.

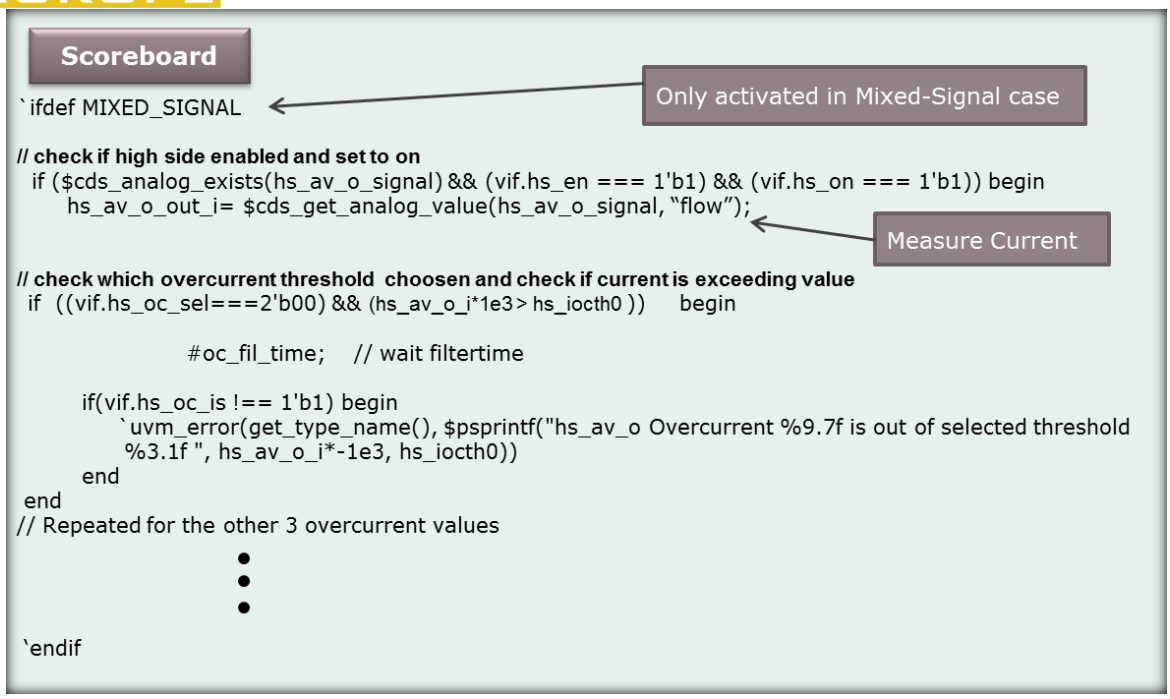

Figure 6. Scoreboard implementation to detect overcurrent for the different thresholds

VI. SUMMARY AND OUTLOOK

In this paper the different level of verification are introduced. Running verification on Module level reduces complexity compared to verification on System on Chip level and is an effective way. The extension of the UVM testbench towards AMS simulation is shown. Regarding reuse the extension towards AMS of the UVM environment is a substantial advance. Analog specific behaviors which are difficult to model in VHDL behavior models are verified under realistic conditions.

The EDA vendors should be encouraged to provide further analog features in the Mixed Signal environment. It would be also helpful to have a defined way to do the configuration for Mixed Signal. The UVM community should be encouraged provide IP libraries to measure and calculate analog quantities to reduce the effort further.

ACKNOWLEDGEMENT

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REFERENCES

[1] Subhasish Mitra, Sanjit A. Seshia, and Nicola Nicolici, "Post-Silicon Validation Opportunities, Challenges and Recent Advances", Proceedings of the 47th Design Automation Conference Pages 12-17.