Advantages of using UVM/System Verilog IEEE standards to Verify Complex Probabilistic Constellation Shaping Design for a Coherent DSP ASIC.

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INTRODUCTION

High-performance Coherent DSPs are powered by complex algorithms, one of which is a Probabilistic Constellation Shaping and Decoding algorithm. Data Distribution Layer. A very high-level optical transmission data path is shown in Figure 1. It shows how the functional blocks are divided into different categories.

- PCS feature highlights:
  - Subcarrier level bandwidth distribution.
  - Configuration supported at chip/module level.
  - Symbol level Encoding and Decoding/interleave Decoding algorithm.
  - Parallel processing using several Encoder and Decoder. Together, and through lower clocks, thus parallel processing.
  - Importance of latency to increase the subcarrier level traffic.
  - Interference and deinterleaving functions and the symbol level communication with Encoder and Decoder blocks to form the boundaries.

TRADITIONAL VERIFICATION METHODOLOGY AND DRAWBACKS

DSP models are verified and written in MATLAB and can be converted to C-models that can be used for verification. Using C-models to verify a critical path is very difficult to debug at the next level of bandwidth comparison to UVM algorithms. The testbench is improved.

- They were not very effective when considering a process requirement. Especially with multiple instances of algorithmic blocks with block working on a different configuration/Encoder and Decoder or slice instances. (Figure 1 and Figure 5). The test is overwhelmed with managing configurations of multiple submodules and the instance hierarchy to program the C-models compared to the desired configuration.

- System Verification model with DPI import is highly preferable when communicating with upper or lower-level environment components compared to TLM ports which provide full functionality modeling layer protocol.

One can make this argument: having an end-to-end C model instead of using SV and UVM based methodology will fail all the issues highlighted above, but that has limitations.

- Configuration: Interconnect design with a constant random verification is not possible using only C model.

- An end-to-end C-model approach is inefficient for self-checking tests. They provide limited debugging opportunities.

- The effort and work put in at module level are not scalable and reusable without much effort at the higher level which has timelines or resources implications.

In Figure 3, we present the Configuration model of a Coherent DSP ASIC. It is a high-level view of the chip that includes all the major components with their interface buses and signals. This diagram shows the physical layout of the chip, including the processor, memory, and various I/O interfaces. Each component is represented as a box with a label detailing its function. The connections between these components are shown as lines, indicating the data signals or control signals that pass between them. The layout is highly simplified to focus on the overall architectural design rather than the fine-grained details. Overall, the diagram provides a comprehensive overview of the chip's design, highlighting its modular structure and the interconnections between its various parts.