2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Advanced Digital-Centric Mixed-Signal Methodology

Methodology for Analog and Mixed-Signal Model Integration and Progression inside a Mature Digital UVM Testbench

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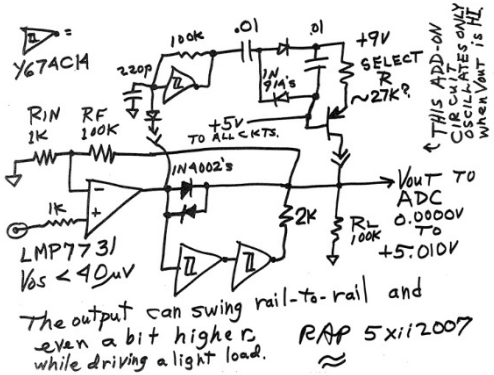
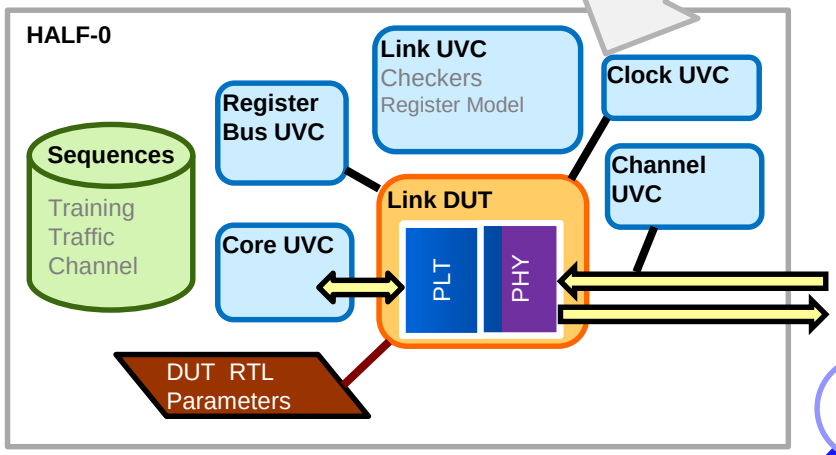
What is Digital-Centric Mixed Signal?

Bringing mixed signal verification to the powerful functional verification world

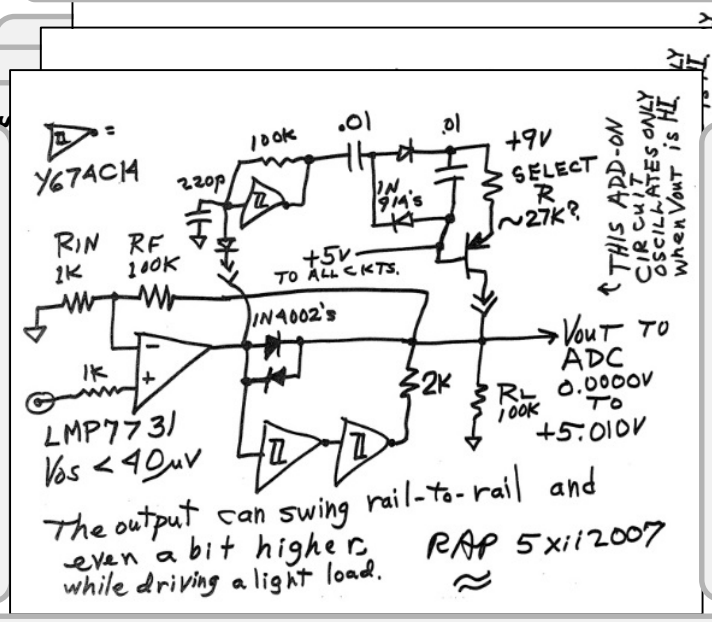




- Existing full featured testbench
- Coverage Driven Verification
- Random stimulus
- Automated checking
- UVM architecture
- Full suite of existing tests
- Automated 24x7 regressions

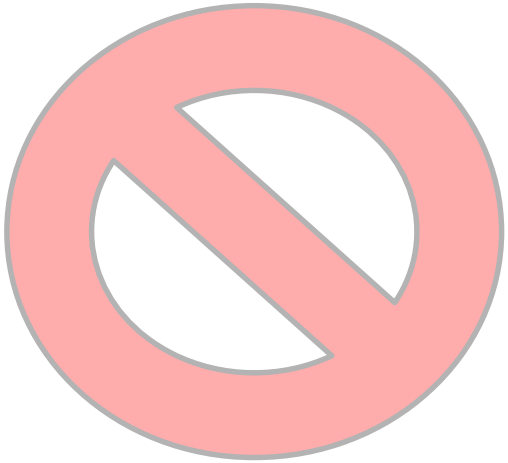
Analog Circuit Verification

Many small subcircuit simulation environments



Simple digital controls provides stimulus

Manual checking



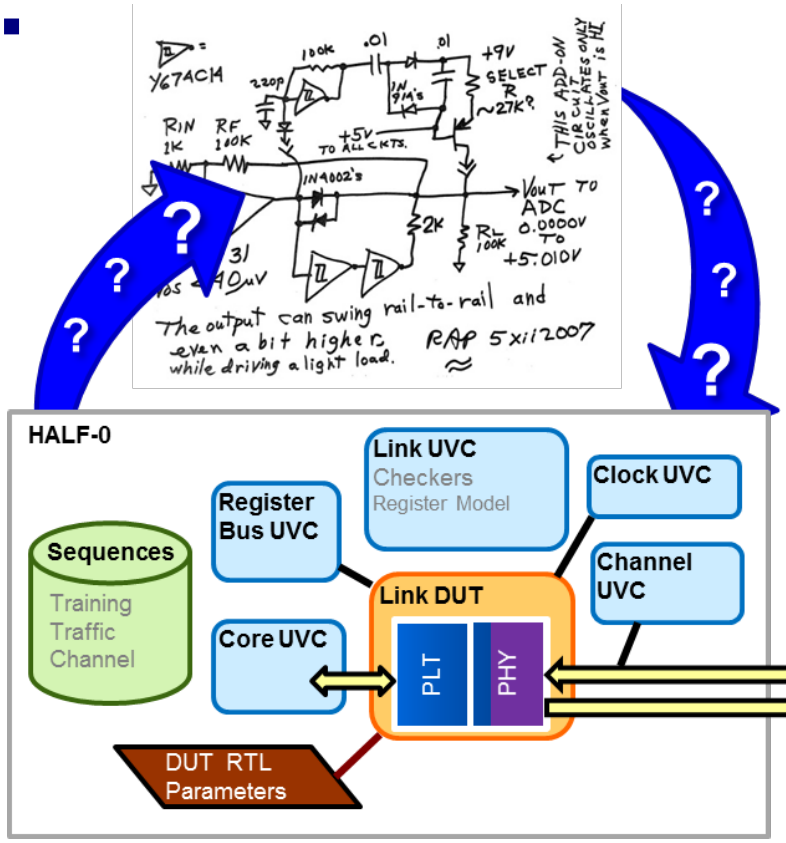
Still requires full gate models for system sims

High investment costs

Our Decision…

Circuit development needs

- Complex algorithms involving more digital logic interaction
- Historical analog / digital bugs
- Unknowns of new technology node



Where do we invest the effort?

- ~~Bring UVM to the analog world~~
- **Bring analog to the discrete testbench**

Our Motivation

Low investment cost / high ROI

- Greater value (high return) using existing infrastructure
- No changes (low investment) needed to digital testbench

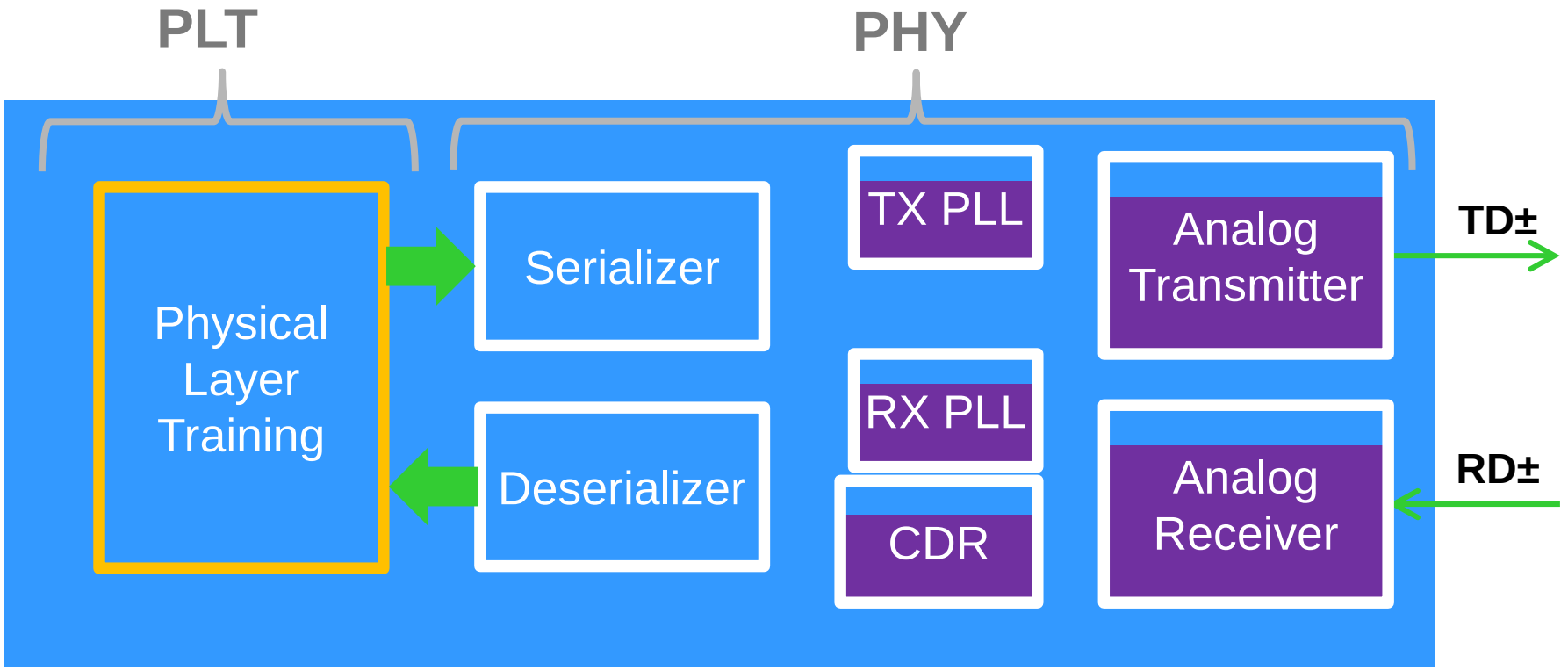
Full power of existing testbench

- Full suite of tests
- Advanced DV techniques in place

Tunable to the exact desired circuits

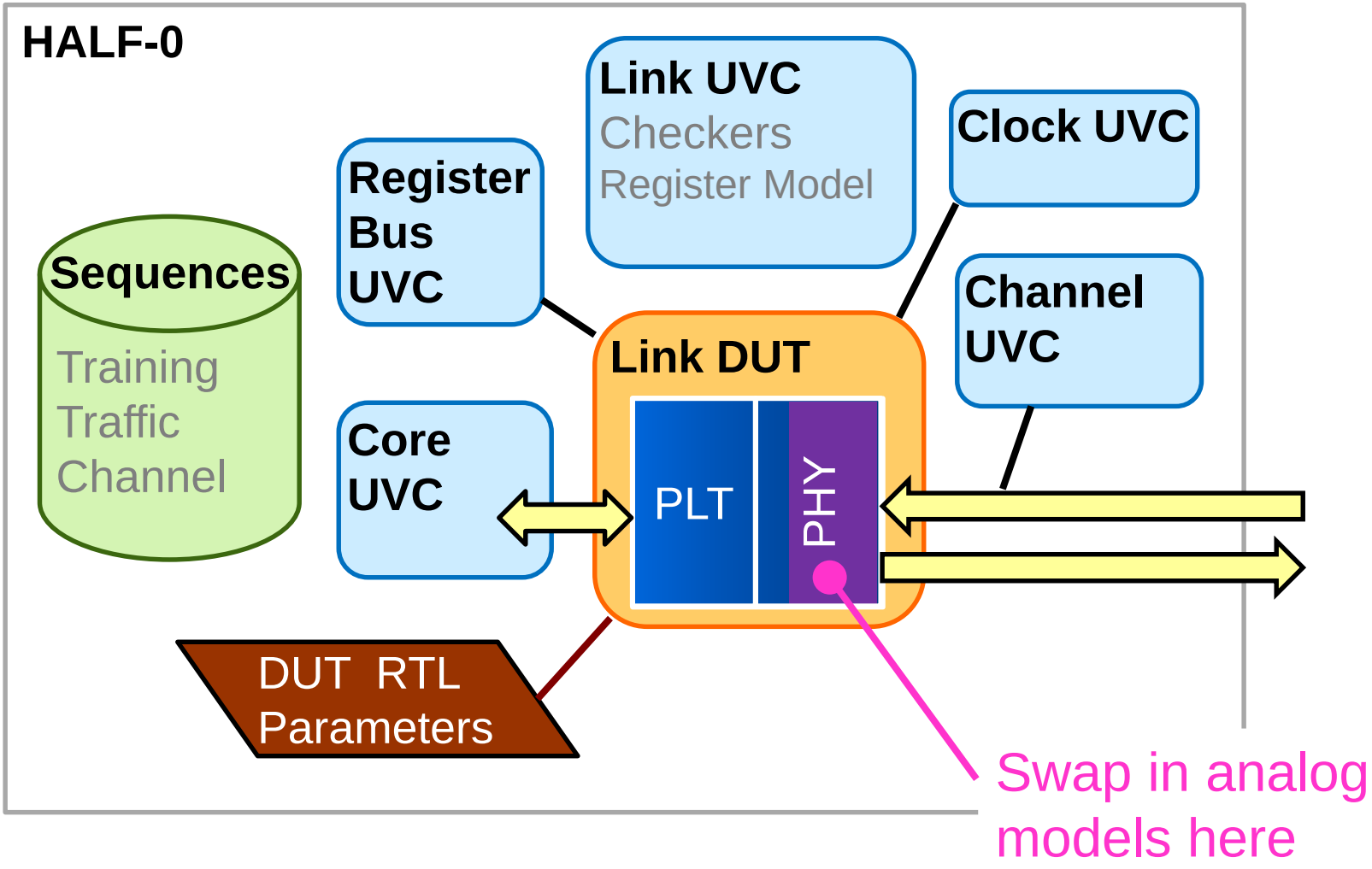
- Focus on the larger algorithm around the circuits

Application - SerDes Link



Analog Design | Discrete Design | RTL Design

Target - PLT UVM Testbench



Models

V – Verification Engineer

A – Analog Engineer

Type	Author	Purpose
High Level Discrete	**V**	• Enable digital testbenches • Bulk high level functional verification
Low Level Discrete	**A**	• Required for all low level cells • Enables gate models in digital testbench • Digital connectivity
Abstracted Models	**A**	• Balance model accuracy with testing objectives (RNM, VerilogA, VerilogAMS) • Example: equalization (de-emphasis) on analog front ends
Analog	**A**	• Full analog circuit provides highest accuracy • Process/skew aware • Targeted only for specific subcircuits.

Getting started

Build flow → Mature AMS tool flows → Cadence irun supports AMS

Model swapping → Verilog Config Block (beh/RNM/VerilogA) → AMS config card (SPICE)

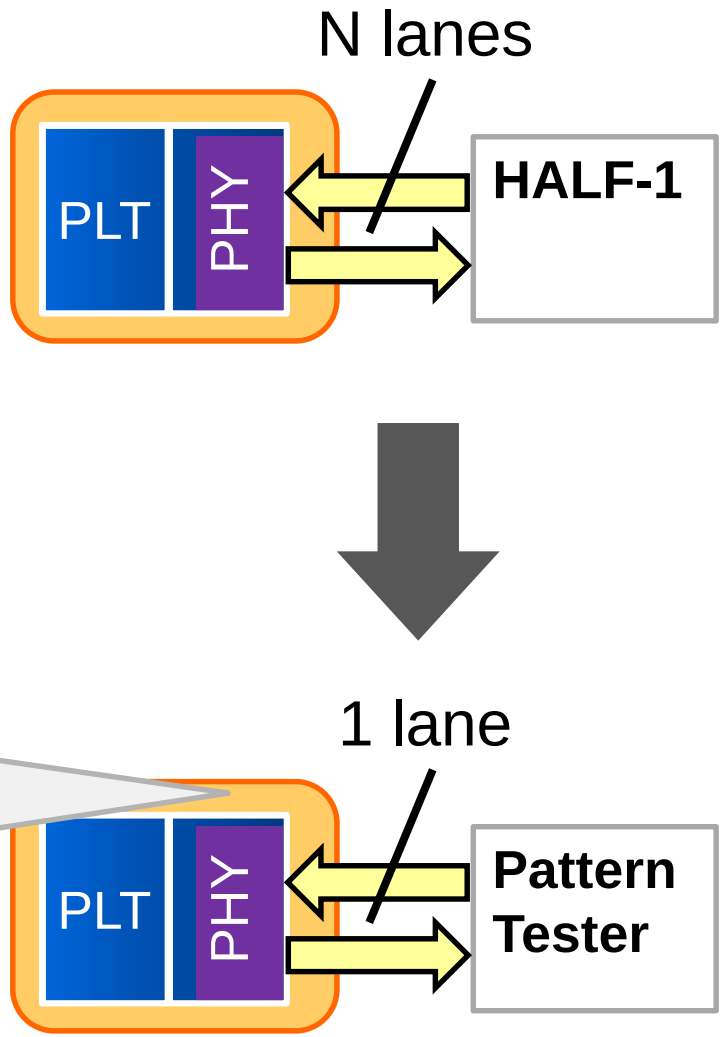
Challenges

- Maturity of mixed-signal tools low (Verilog 2009/SV)
- Full control of analog settings from random TB

Addressing Performance

Speed Improvements

- Shorten reset period
- Parameterization limits amount of analog models
- Adjust to testing focus
- Traditional approaches
  - Backdoor CSRs
  - Tune analog solver parameters
  - Alternate models (RNMs, etc.)



8x faster simulation time

UVM Testbench is ready! Where are my Models?

- The PLT and PHY designed in parallel.

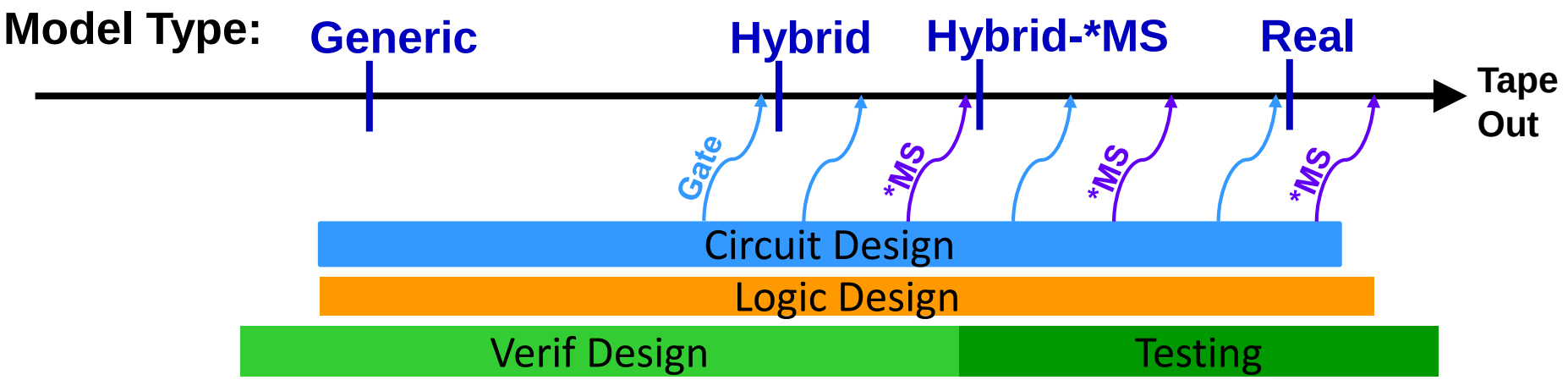
- PHY circuits designed bottoms up meaning no complete design until late into the project.

Solution:

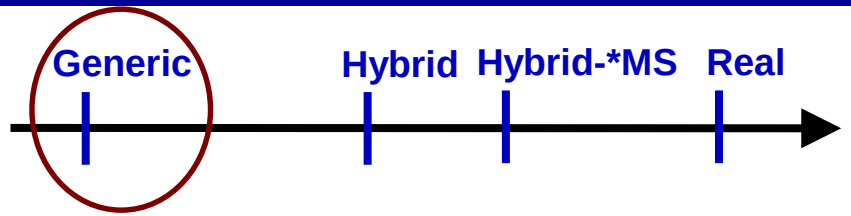
Model Progression Plan

Model Progression Plan

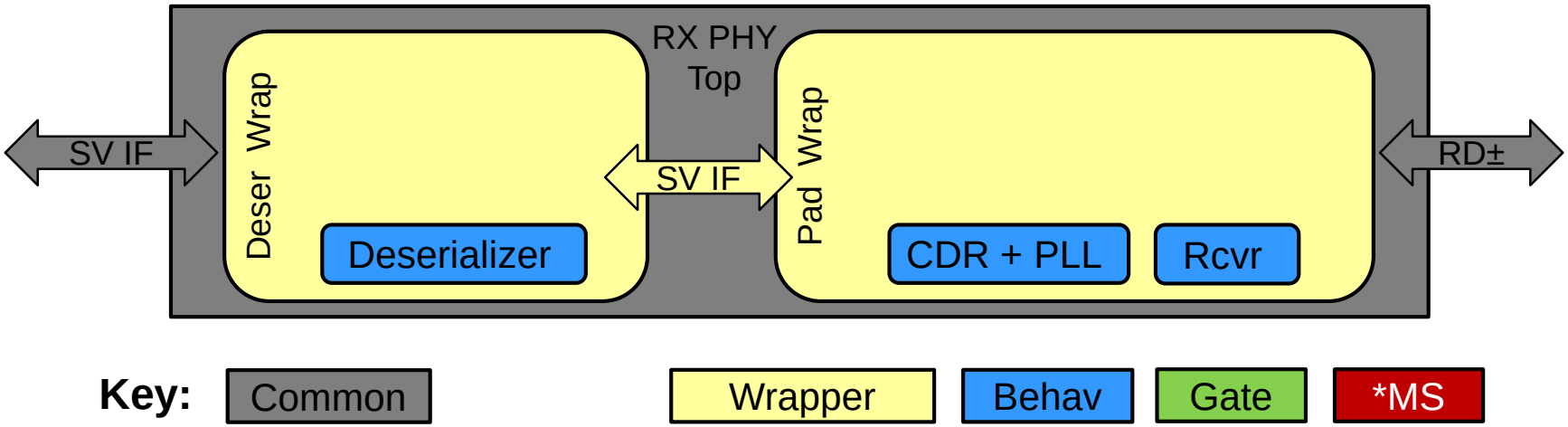
- Project long framework for upgrading behavioral models with completed schematic designs (gate models) over time.
- Pieces of the gate model can then be further upgraded with *MS or Analog models.
- The order of model delivery into this framework.



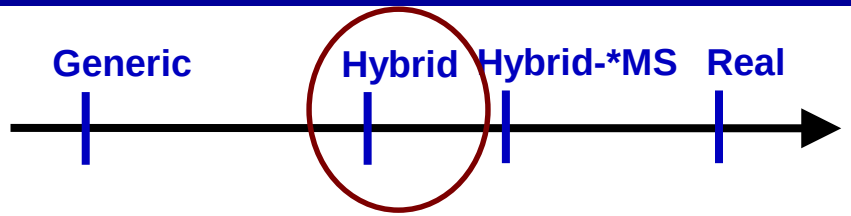
Generic



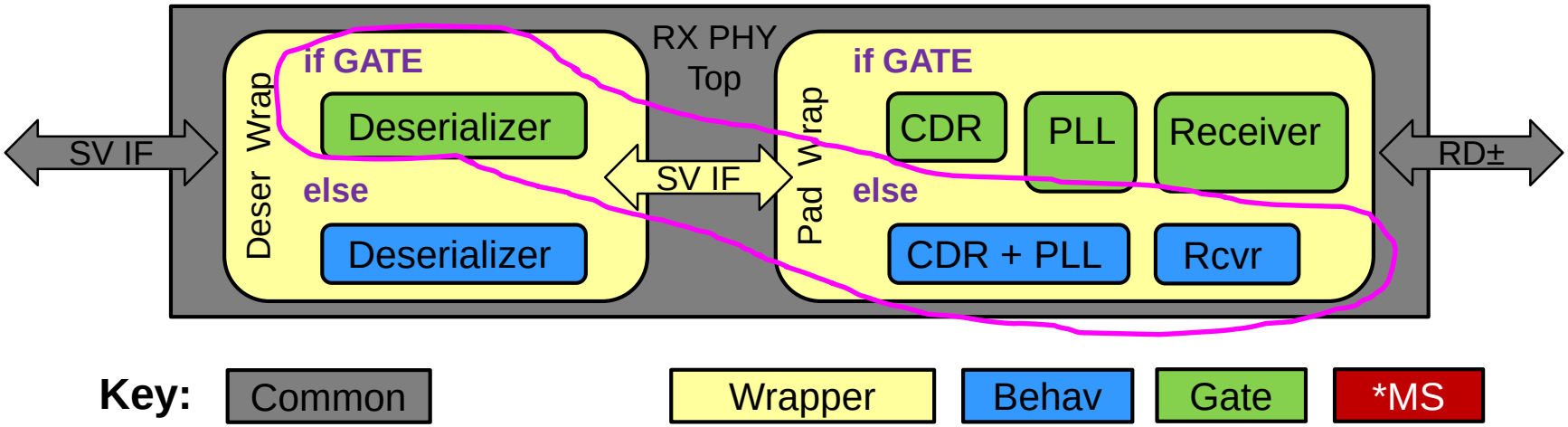
- Worked with analog microarchitect to define the long term high level hierarchy of the overall design.
- Generic behavioral models for major subblocks.
- Enables UVM digital testbench before physical design begins.
- Wrappers and SystemVerilog interfaces hide internal upgrades to come.



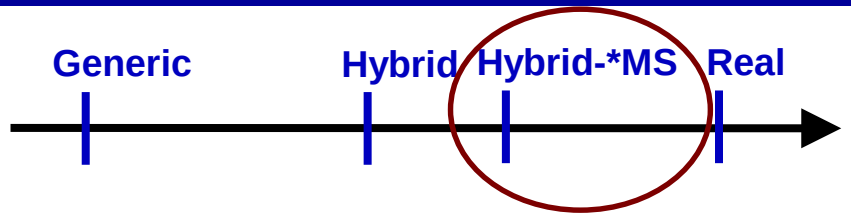
Hybrid



- Mixture of behavioral and gate models.
- Wrappers use Verilog parameter or define to swap between model type.
- Extra logic needed to bring generic behavioral up to par with real gate design.
- Behavioral + gate combos dictated by model delivery order.



Hybrid-*MS



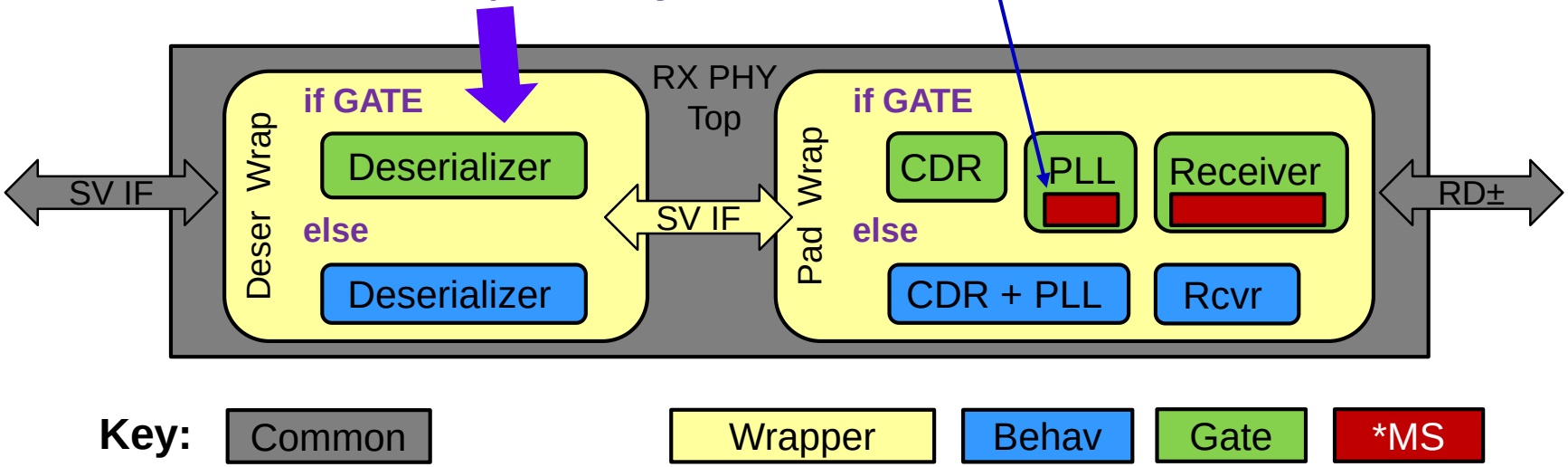
- With gate model in place, MS models can now be used.

```
config cfg_phy_vco_vams;
   design worklib.top;
   instance top.half0.phy.rx_pad.pll.vco use worklib.mikes_vco:rnm;
endconfig
```

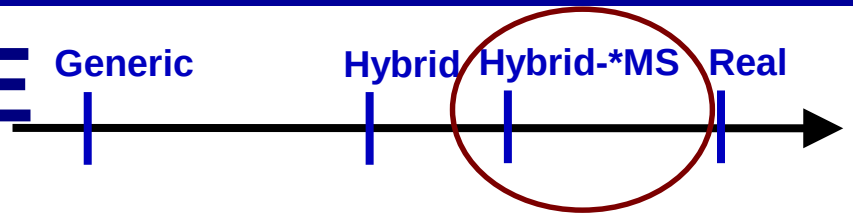
Models 1:1 with schematic for easy swapping

Additional Wrapper Benefits:

- Keep non-logic discipline contained
- Convert to *MS friendly Verilog constructs

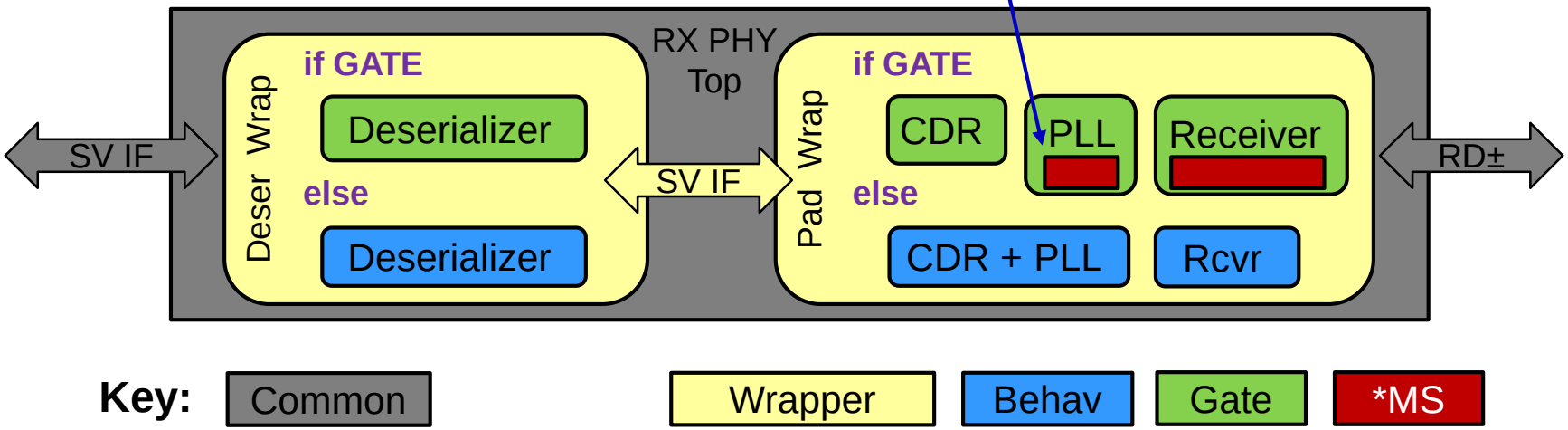


Hybrid+SPICE

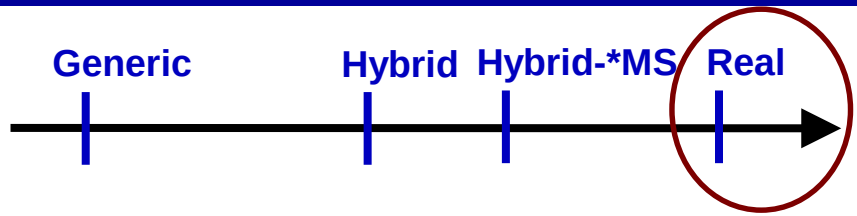


- SPICE models can be added as well.

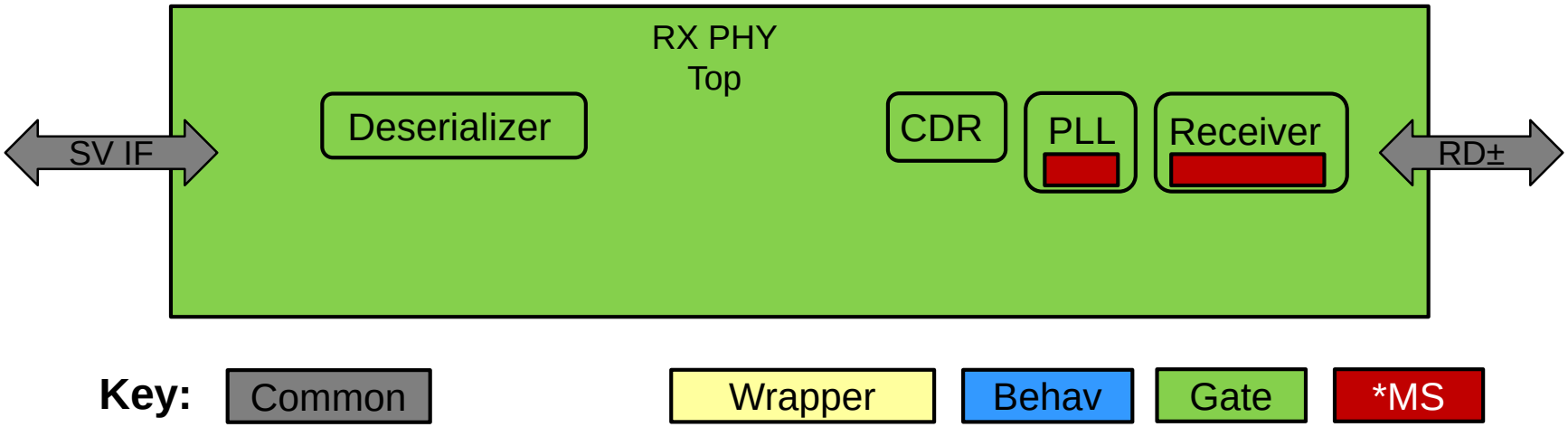
```
include "vco.scs"
amsd {
   // match ports between schematic and module using port names
   portmap subckt=vco autobus=yes reffile="vco.v" porttype=name
   config inst="top.half0.phy.rxpad.pll.vco" use=spice
}
```



Real



- Entire model is complete gate level extract from schematics.
- Mixed signal models can be swapped in again for final testing.



Roles

Verification Engineers

- Create and maintain testbenches
- All infrastructure tooling
- Create high-level behavioral models
- Debug and triage

Analog Engineers

- Develop low-level analog circuits
- Develop gate model hierarchy
- Create and verify Mixed Signal models

Results

Small Investment

- Low cost to add complete mixed signal capability to mature UVM testbench

Real Benefits

- Added models reaped benefits of more complete stimulus and checking

Model Progression Plan Worked

- Enabled testbench well ahead of schematics
- Swapping gate/*MS models later was easy

Cross Discipline Understanding

- Grew team's cross discipline knowledge and teamwork

Sim Performance

Simulation Time (minutes)		
Model Type	**Serializer 16 Subcircuits**	**Serializer All Circuits**
Discrete Behavioral	1	1
Real Number Model	2.5	n/a
Verilog-A	5	n/a
Fast-SPICE*	14	501 (8 hours)
SPICE*	40	4740 (79 hours)

* Huge variability depending on accuracy and waveform settings (range: 1 hour to weeks)

Future Plans

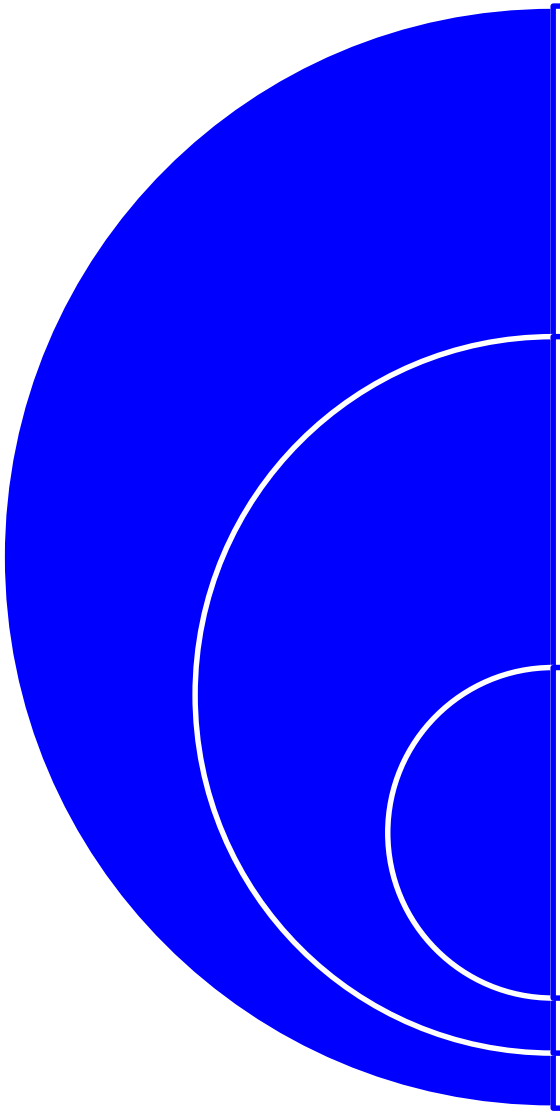
More Real-Number Models

- Enable full length link training simulation.
- Target PLT+PHY holistic items like automatic equalization.

Save and restore capabilities

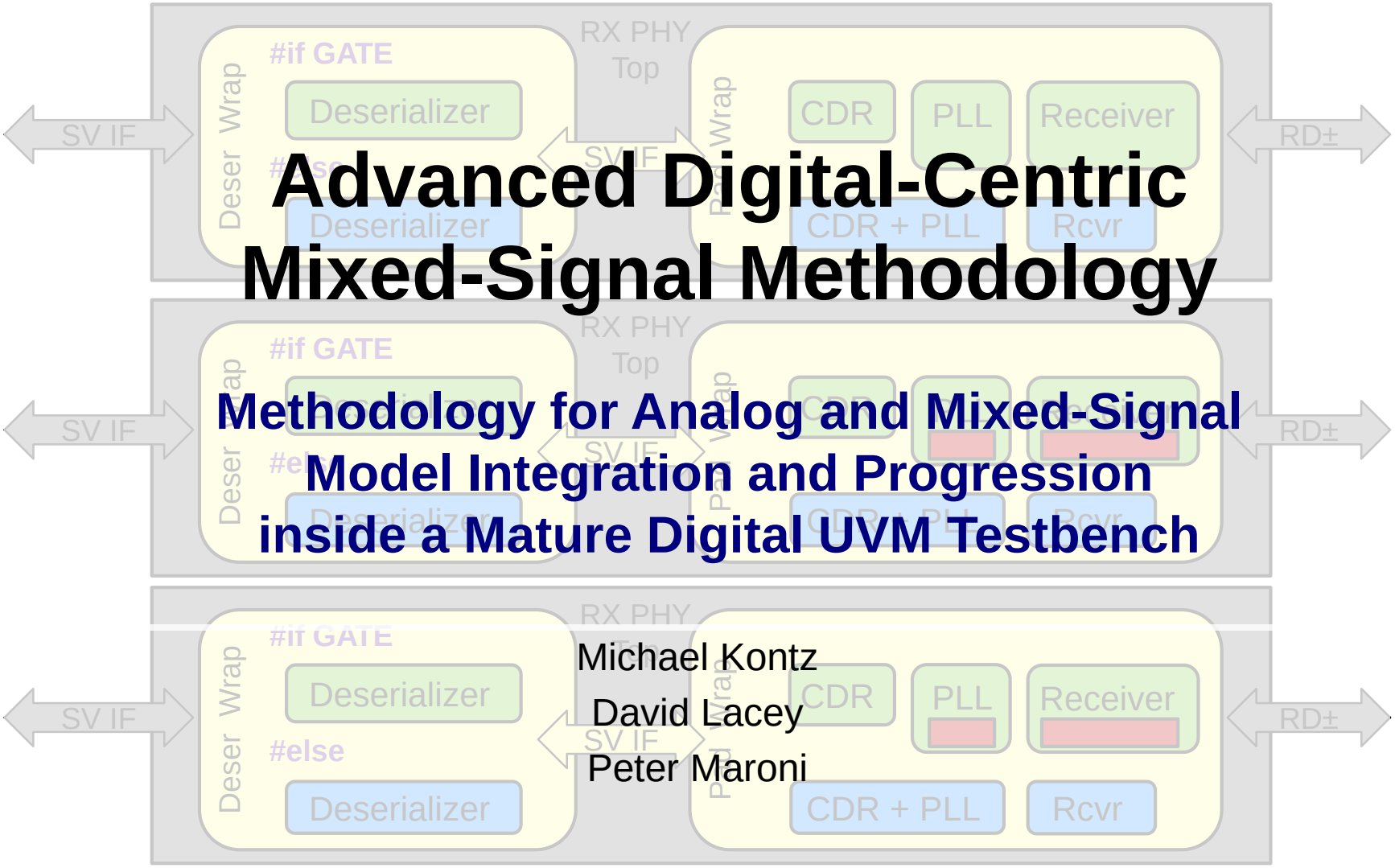
- Restore mixed signal sim after lengthy reset and calibration with different stimulus.

Conclusions



Complete flexibility with minimal investment	• Languages and tools are ready • Only incremental effort required – high ROI
Mixed environment not equal capability to digital	• Mixed signal tools are still maturing • Shield MS models from advanced RTL constructs
Model Progression plan achieves earlier verification	• Schematic designs and *MS models added to UVM testbench as soon as they're available • Plan == Teamwork

Questions



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