Achieving Faster Reset Verification Closure with Intelligent Reset Domain Crossings Detection

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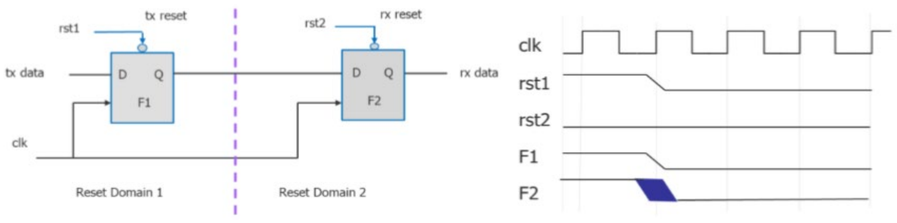
Introduction

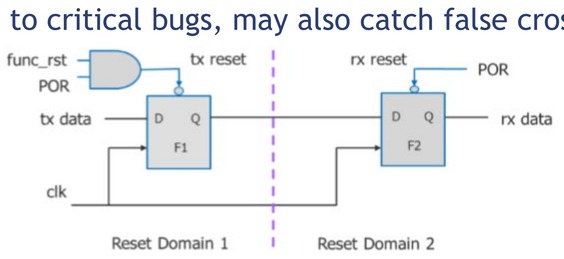
➢ Complex reset architecture of multiple reset sources splits SoC chip into several reset domains

➢ Data signal metastability captured on a Reset Domain Crossing (RDC) path can cause chip to fail



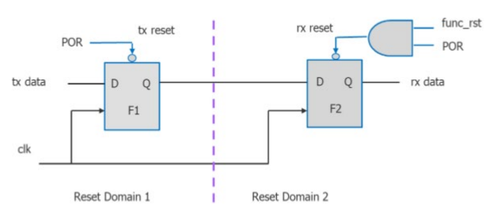
➢Dependency of reset domain of a sequential on concurrent assertion/de-assertion of several reset sources complicates RDC analysis

➢ RDC verification of SoC, in addition to critical bugs, may also catch false crossings having overlapping reset domains



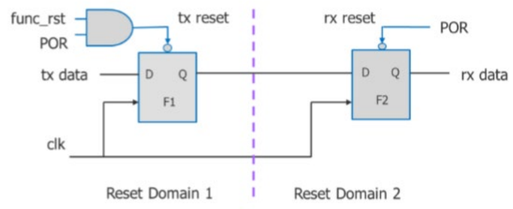
Complexity Of Reset Domain Verification Analysis

➢ Rise in functional modes leads to rise in combinational resets resulting in complex reset architecture
➢ Two categories of crossings having multiple dependent reset assertions, reported as bugs by traditional methodologies:



S. no.	POR	func_rst	Result
1	1 → 0	1→ 0	No RDC issue
2	1 → 0	1	No RDC issue
3	1	1 → 0	No Reset Assertion
4	1	1	No Reset Assertion

1. All resets in source domain impact destination domain



S. no.	func_rst	POR	Result
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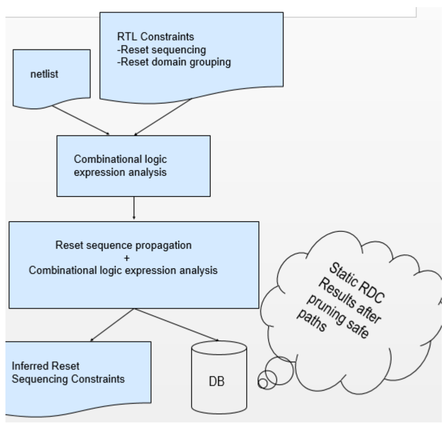
4	1 → 0	1	RDC issue

2. Some resets in source domain do not impact destination domain

Reset Detection Optimization Methodology

➢ The proposed method utilizes a combination of structural reset analysis, expression analysis, and functional analysis to prune noisy and inefficient RDC paths in the design during static verification.



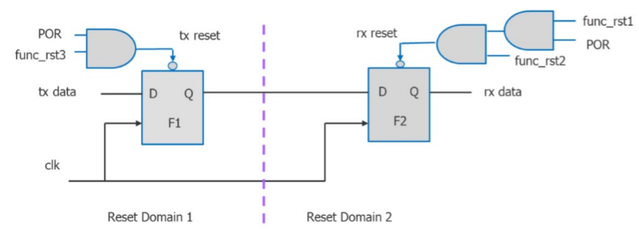
➢ **Stage 1:** Comprehensive expression analysis of the resets at source and destination to identify and prune safe candidates
➢ **Stage 2:** Propagation of user defined reset sequencing across combinational resets in addition to reset expression analysis to identify and prune safe candidates out of second category crossings

Analysis of Reset detection Optimization Methodology

➢ **Quality of results and minimal noise**
- Proposed methodology always resulted in reduction in noise by at least one fourth

➢ **Ease of debug**
- Filtered crossings and ordered crossings available for user separately to debug and verify
- Debug aids available for reset structure analysis and tracing inferred reset sequencing in the form of report file

➢ **Accuracy**
- Multi-level complex reset structures handled accurately



➢ **Reduction in verification time**
- False crossings pruned in the initial stage of analysis giving cleaner, genuine RDC paths for designer to verify.

CASE STUDY

➢ The proposed methodology was benchmarked on a highly complex real SoC with more than 1.8 million registers, and 5 RAMs

➢ Out of Identified 287 reset domains including asynchronous and synchronous resets, 90k RDC crossings detected during RDC analysis.

➢ Comparison of RDC results on the SoC with and without proposed methodology, with reset grouping and reset ordering applicable:

Reset Domain Crossings	Number of crossings
RDCs having source and destination registers in different asynchronous reset domains ***without*** proposed methodology	34562
RDCs having source and destination registers in different asynchronous reset domains ***with*** proposed methodology	22811
Ordered RDC paths (based on sequencing information) **without** proposed methodology	23126
Ordered RDC paths (based on sequencing information) **with** proposed methodology	27650

➢ Around ~34% crossings pruned as false paths, ~20% increase in ordered crossings.

CONCLUSIONS

➢ Proposed automatic technique improves quality of results for static RDC analysis, and reduces closure time required for real RDC issues
➢ Improved tool performance
➢ Methodology ensures no critical path is missed and false crossings are pruned
➢ Advanced techniques utilize reset ordering information as well to simplify the reset architecture and enhances the tool capabilities

REFERENCES

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[2] Chris Kwok, Priya Viswanathan, Ping Yeung, “Addressing the Challenges of Reset Verification in SoC Designs”, DVCon US, 2015
[3] Akanksha Gupta, Ashish Hari, Anwesha Choudhary, “Systematic Methodology to Solve Reset Challenges in Automotive SoCs”, DVCON Europe 2019

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