ACE'ing the Verification of SOCs with Cache Coherent Heterogeneous Multiprocessors Targeted for Optimized Power Consumption

Authors

Mehul Kumar | Broadcom Corp.

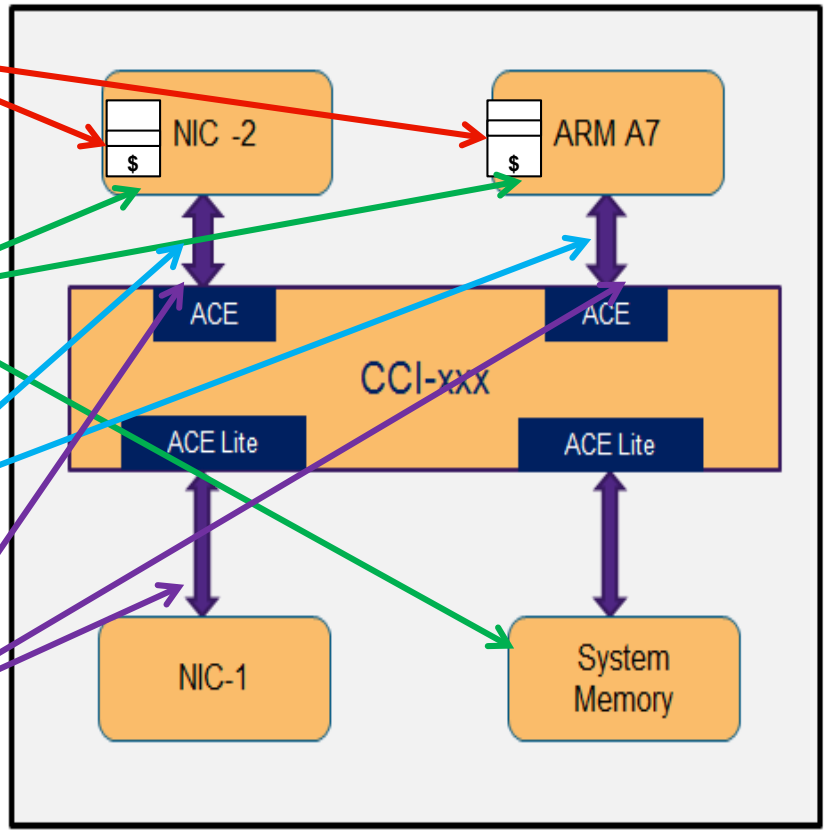
Shawn Honess | Synopsys Inc

Amir Nilipour | Synopsys Inc.

Tushar Mattu | Synopsys Inc.

System Coherency Verification

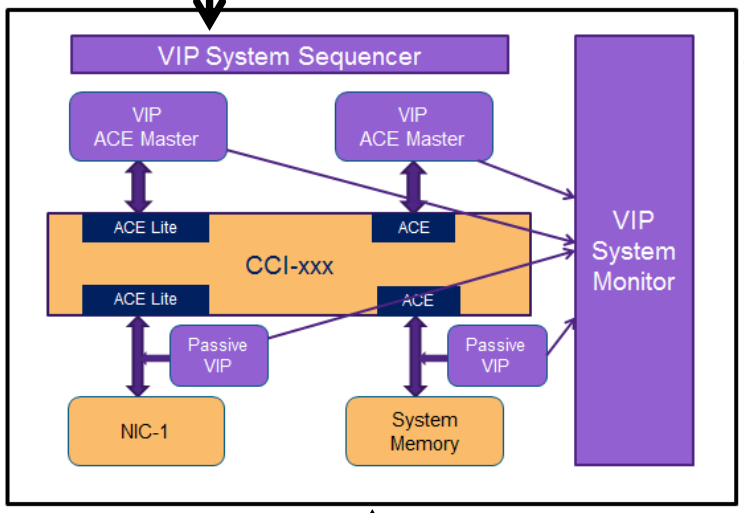
- Maintain coherency across caches
- Coherency across master cache and memory
- Issuing Snoop transactions
- Data Integrity between snoop and coherent transactions
- Sequencing transactions



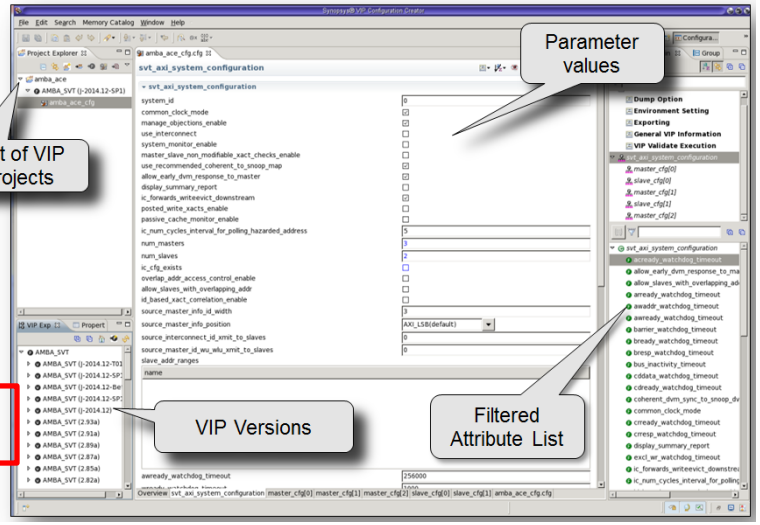
Verification Environment

READONCE
MAKEUNIQUE
READCLEAN

VIP Test Suite

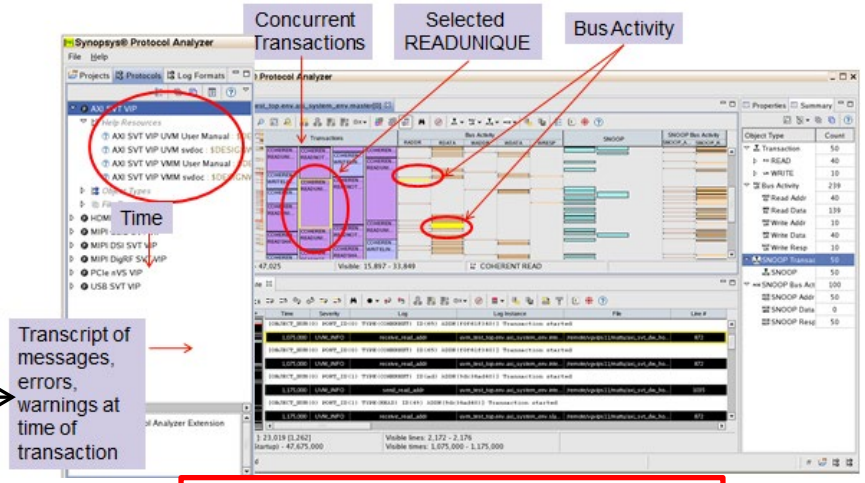


Testbench



VIP Configuration creator

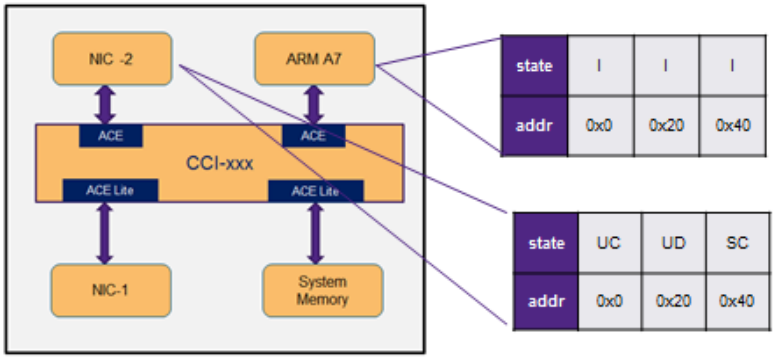
DEBUG



Verdi Protocol Analyser

Coherent Stimulus

Stimulus Permutations



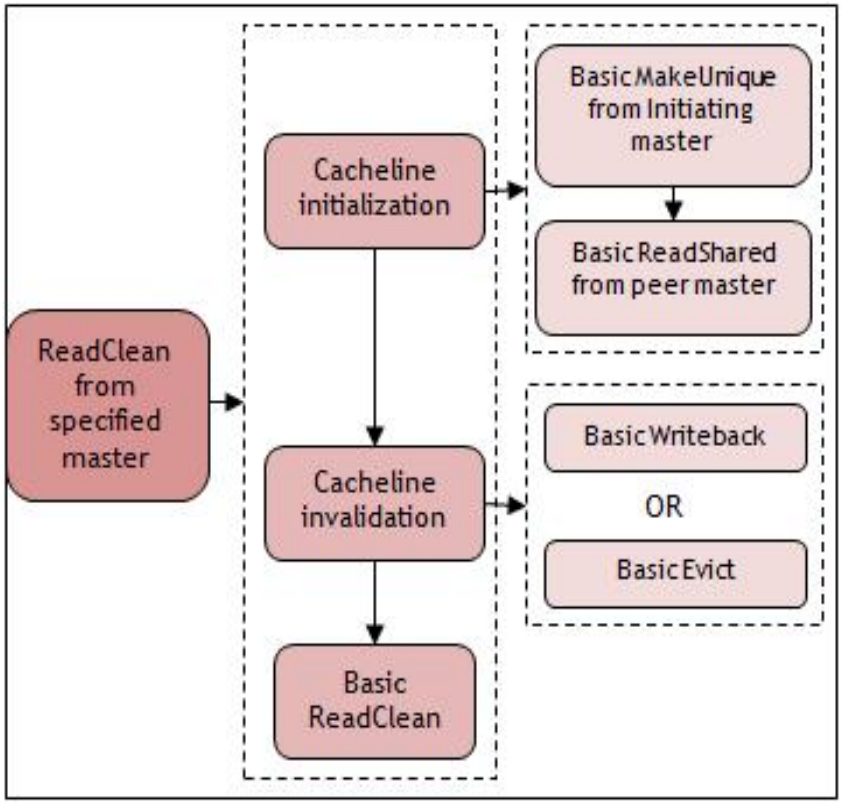
Peer caches initialized to valid cache line states to enable different responses and cache state transitions

Several combinations of start/end state of cache and responses to be tested

Table C4-5 Expected ReadClean cache line state change

Transaction	Start state	RRESP[3:2] IsShared/PassDirty	Expected end state	Legal end state With Snoop Filter	Legal end state No Snoop Filter
ReadClean	I	00	UC	UC, SC	I, UC, SC
		10	SC	SC	I, SC

Sample Sequence Flow



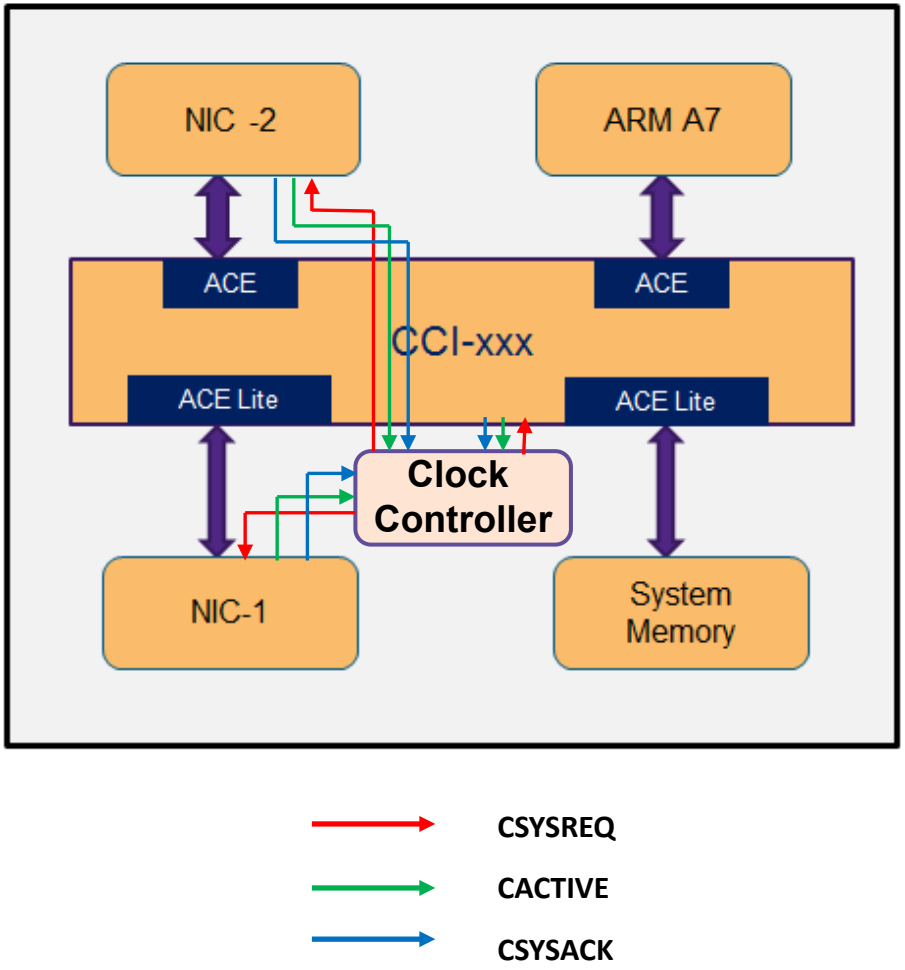
Low Power (LP) Interface : C-Channel

Low Power Interface used to reduce power consumption of a system

LP signaling and handshake between peripherals & clock controller

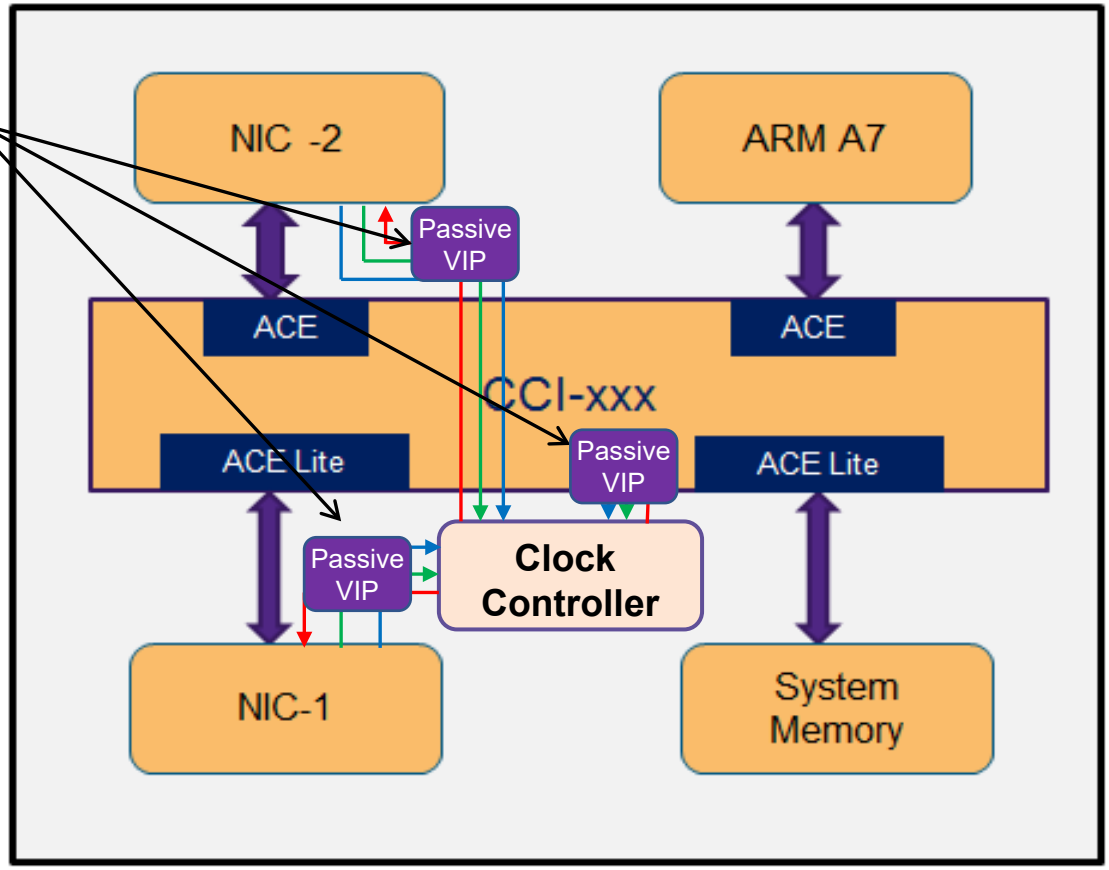
Dynamically disable/enable clocks to peripherals and system components

Peripheral can request its clock to be enabled or disabled

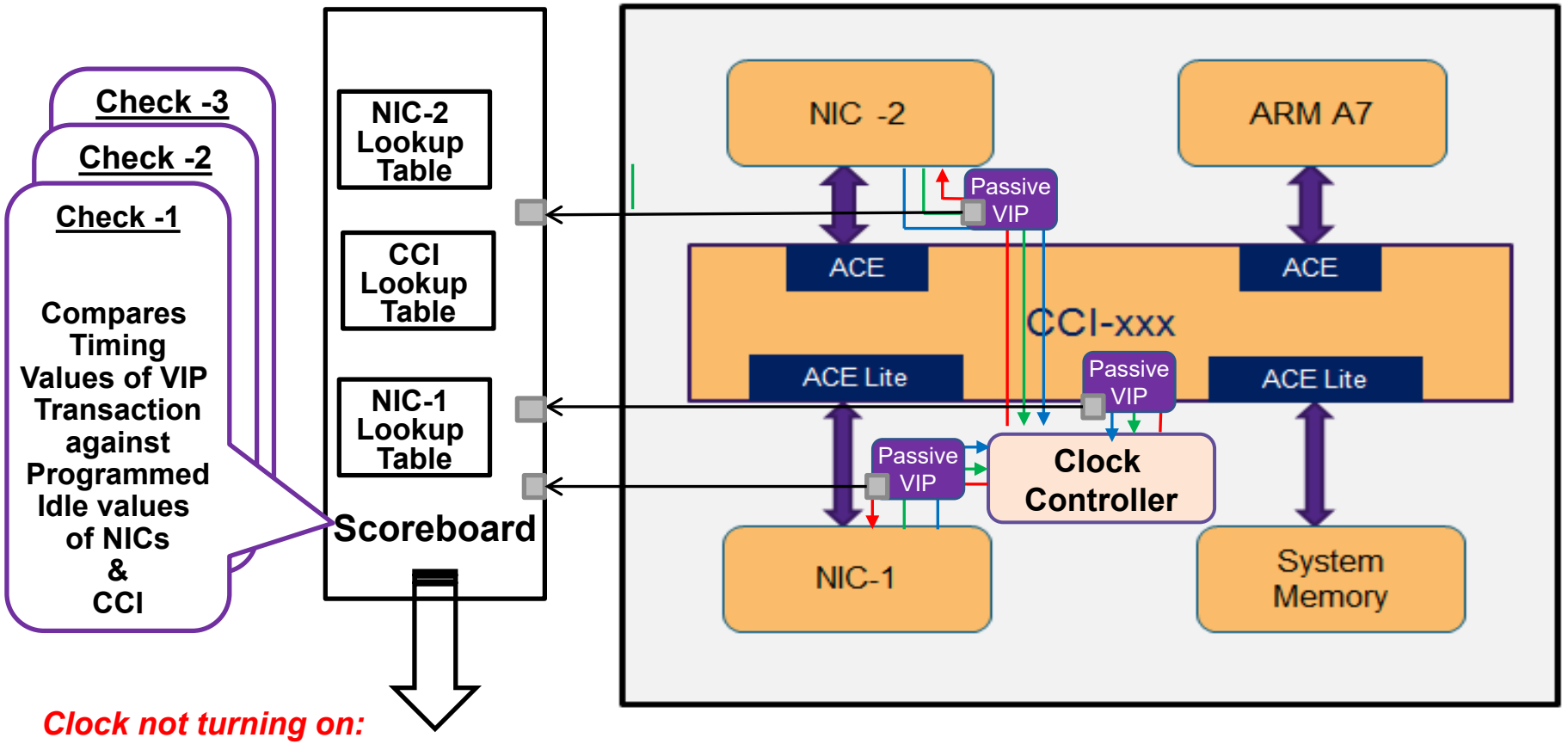


VIP for Low Power(LP) Interface

- AXI VIP Low Power Agent
- Protocol Checking as per Specification
- VIP Transaction provides timing information of LP entry, exit
- VIP provides analysis port and events



Low Power Entry & Exit Scoreboarding



Clock not turning on:
UVM_ERROR @ 118555.1ns: [scoreboard] csysack_cd_clk_sysm not changing as expected

Clock not turning off after required N clock cycle expiry:
UVM_ERROR @ 119473.2ns: [scoreboard] cactive_cd_clk_sysm csysreq_cd_clk_sysm not changing as expected after Timer timeout

Conclusion

- Complex dynamic clock gating scheme was validated at backplane level.
- The design issues are caught early in the RTL design cycle using the methodology proposed.
- VIP Verification features enabled team to spent more time in writing design specific tests, checks and coverage.
- The verification performed with combination of Synopsys VIP system checking and end-end Scoreboard lowered risk