ACE’ing the Verification of SOCs with Cache Coherent Heterogeneous Multiprocessors Targeted for Optimized Power Consumption

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System Coherency Verification

- Maintain coherency across caches
- Coherency across master cache and memory
- Issuing Snoop transactions
- Data Integrity between snoop and coherent transactions
- Sequencing transactions
Verification Environment

VIP Test Suite

READONCE
MAKEUNIQUE
READCLEAN

VIP System Sequencer

VIP ACE Master

ACE Lite

Passive VIP

NIC-1

System Memory

VIP System Monitor

Testbench

VIP Configuration creator

Parameter values

List of VIP projects

VIP Versions

Filtered Attribute List

Concurrent Transactions

Selected READONCE

BusActivity

Transcript of messages, errors, warnings at time of transaction

DEBUG

Verdi Protocol Analyser
Coherent Stimulus

Stimulus Permutations

Peer caches initialized to valid cache line states to enable different responses and cache state transitions.

Several combinations of start/end state of cache and responses to be tested.

Sample Sequence Flow

Table C4-5: Expected ReadClean cache line state change

<table>
<thead>
<tr>
<th>Transaction</th>
<th>Start state</th>
<th>RRESP[0:2]</th>
<th>Expected end state</th>
<th>Legal end state</th>
</tr>
</thead>
<tbody>
<tr>
<td>ReadClean</td>
<td>I</td>
<td>00</td>
<td>UC</td>
<td>UC, SC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>SC</td>
<td>SC</td>
</tr>
</tbody>
</table>

Basic MakeUnique from Initiating master

Basic ReadShared from peer master

ReadClean from specified master

Cacheline invalidation

Basic ReadClean

Basic Writeback

Basic Evict

OR
Low Power Interface used to reduce power consumption of a system

LP signaling and handshake between peripherals & clock controller

Dynamically disable/enable clocks to peripherals and system components

Peripheral can request its clock to be enabled or disabled

![Block diagram of Low Power Interface: C-Chanel](image)
VIP for Low Power (LP) Interface

- AXI VIP Low Power Agent
- Protocol Checking as per Specification
- VIP Transaction provides timing information of LP entry, exit
- VIP provides analysis port and events

VIP Transaction provides timing information of LP entry, exit

VIP provides analysis port and events
Low Power Entry & Exit Scoreboarding

Clock not turning on:
\texttt{UVM\_ERROR @ 118555.1ns: [scoreboard] csysack\_cd\_clk\_sysm not changing as expected}

Clock not turning off after required \( N \) clock cycle expiry:
\texttt{UVM\_ERROR @ 119473.2ns: [scoreboard] cactive\_cd\_clk\_sysm csysreq\_cd\_clk\_sysm not changing as expected after Timer timeout}
Conclusion

• Complex dynamic clock gating scheme was validated at backplane level.

• The design issues are caught early in the RTL design cycle using the methodology proposed.

• VIP Verification features enabled team to spent more time in writing design specific tests, checks and coverage.

• The verification performed with combination of Synopsys VIP system checking and end-end Scoreboard lowered risk