Accellera Systems Initiative SystemC Standards Update

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Presentation Overview

- Accellera Overview
 - Membership list
 - How to join a WG
 - Global SystemC events
- Number of IEEE-1666 standard downloads
- Accellera SystemC Working Group updates
 - Language & Transaction-Level Modeling
 - Configuration, Control & Inspection
 - Synthesis
 - Analog/Mixed-Signal
 - Verification





All Members Can Join SystemC WGs!

Corporate Members



























Associate Members























































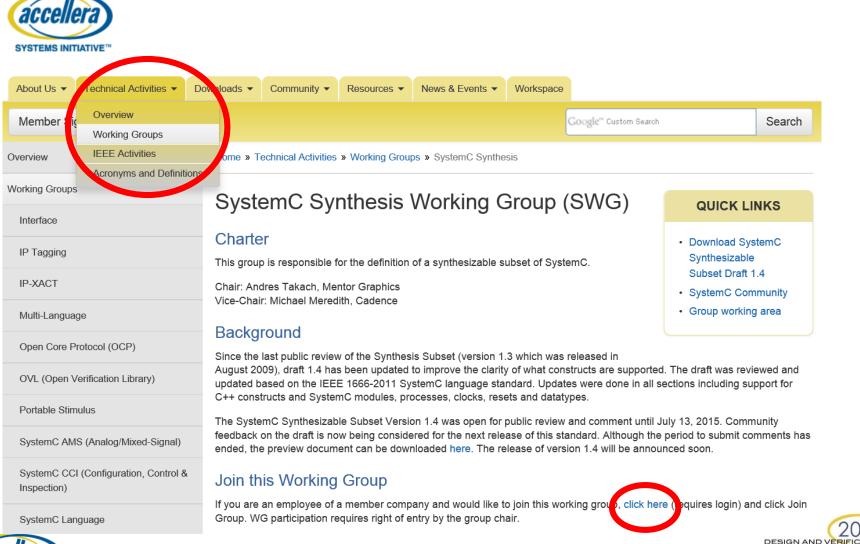




DESIGN AND VERIFICATION



Join A Working Group And Contribute!





SystemC Community

- Online at http://accellera.org/community/systemc
- Community forums, upload area for contributions, SystemC news



Home » Community » SystemC

SystemC

SystemC addresses the need for a system design and verification language that spans hardware and software. It is a language built in



standard C++ by extending the language with a set of class libraries created for design and verification. Users worldwide are applying SystemC to system-level modeling, abstract analog/mixed-signal modeling, architectural exploration, performance modeling, software development, functional verification, and high-level synthesis.

COMMUNITY LINKS

- Download SystemC
- Forums
- Uploads
- Working Groups
 - Language
 - AMS
 - TLM
 - o CCI
 - Synthesis
 - Verification





Global SystemC Presence 2015+

- DVCon US March in Silicon Valley
- DAC June in San Francisco
- SystemC Japan June in Shin-Yokohama
- DVCon India September in Bangalore
- DVCon Europe November in Munich
- Accellera Day Taiwan December, location TBA

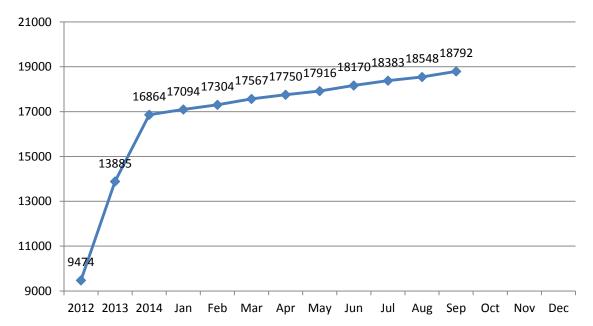




IEEE 1666 SystemC Downloads



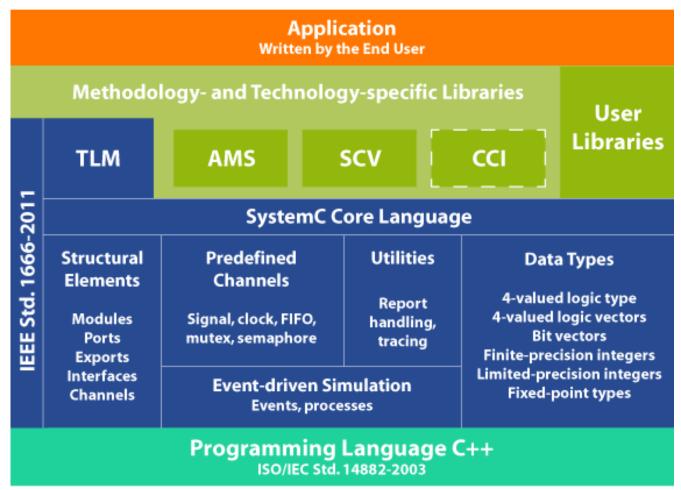
Cummulative Downloads - 2012-15



http://standards.ieee.org/getieee/1666/download/1666-2011.pdf



SystemC Overview







SystemC Language Working Group

• Charter: Responsible for the definition and development of the SystemC core language, the foundation on which all other SystemC libraries and functionality are built.

Current status

- SystemC/TLM 2.3.1 released in April 2014
- Currently collecting, addressing, refining proposals and errata towards IEEE 1666-201x
- Adding extensions to the core language
 (e.g. as needed by other SystemC-related WGs)

Plans for 2015/2016

 Continue work on necessary standards extensions for parallelization of SystemC simulations (contributors wanted!)





SystemC TLM Working Group

 Charter: The Transaction-level Modeling Working Group (TLMWG) is responsible for the definition and development of methodology and add-on libraries for transaction-level modeling in SystemC.

Current status

Accellera TLM-2.0 became part of IEEE 1666-2011,
 PoC implementation 2.0.3 bundled with SystemC 2.3.1

Plans for 2015/2016

- Work on TLM interfaces, extensions, and guidelines to improve modeling of protocols beyond memory-mapped I/O
- "TLM signals"; serial, bi-directional communication, …





SystemC Synthesis WG

 Charter: To define the SystemC synthesis subset to allow synthesis of digital hardware from high-level specifications.

Current status

- Public review of SystemC Synthesizable Subset 1.4 completed in July 2015
- Processing feedback from review
- http://workspace.accellera.org/apps/org/workgroup/swg

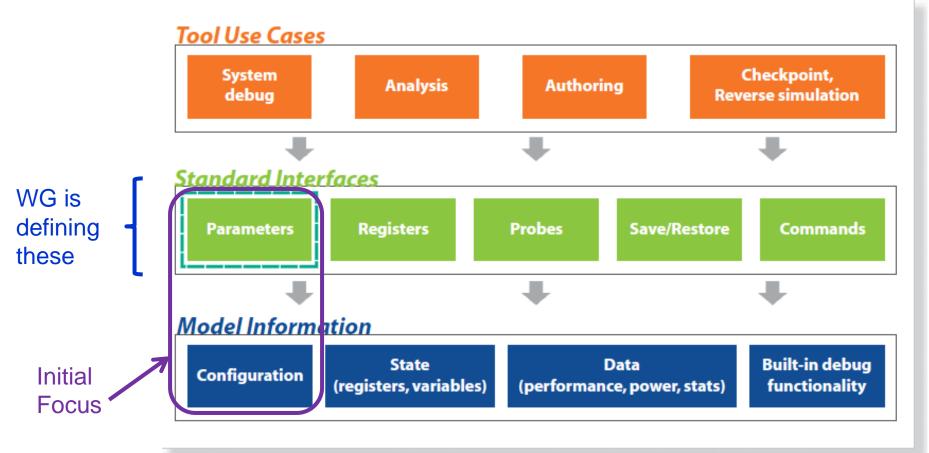
Plans for 2015/2016

- Release of standard targeted for Q4 2015
- Start work on new topics for the second version of the standard





Configuration, Control & Inspection WG



Goal: Standardizing interfaces between models and tools



CCI WG Status

- Configuration standard status
 - Requirements specification, available on Accellera web site
 - Proof-of-Concept Implementation, educational examples
 - Key improvements identified
 - Technical previews available:
 ISCUG '13: http://www.iscug.in/iscug2013_agenda_tutorials
 DVCON '13:
 - http://events.dvcon.org/events/proceedings.aspx?id=144-2-T
- Working to prepare a 2016 draft standard public review
 - Make identified improvements
 - Complete the Library Reference Manual (LRM)





SystemC Analog/Mixed-Signal WG

 Charter: The SystemC AMS Working Group is responsible for the standardization of the SystemC AMS extensions, defining and developing the language, methodology and class libraries for analog, mixed-signal and RF modeling in SystemC

Current status

- IEEE P1666.1 SystemC AMS Working Group completed draft for ballot in IEEE-SA (October 2015)
- New features under development (e.g. piece-wise-linear modeling, tracing customization, analog solver parameters)

Plans 2015/2016

- Approval of IEEE 1666.1-2016 by IEEE-SA
- Publish User's Guide update based on SystemC AMS 2.0





SystemC Verification WG

• Charter: The Verification Working Group (VWG) is responsible for defining verification extensions to the SystemC language standard, and to enrich the SystemC reference implementation by offering an add-on libraries (SystemC Verification (SCV) library, etc.) to ease the deployment of a verification methodology based on SystemC.

Current Status

Released version 2.0 of SystemC Verification library (SCV) in April 2014

Plans for 2015/2016

- Integrate the UVM verification methodology in SystemC
- Standardization of coverage APIs (coverage groups, bins, etc.)
- Further explorations of needs regarding SystemC/TLM





UVM in SystemC

- Native UVM implementation in SystemC
- Language Reference Manual finished
- Open source proof-of-concept implementation in public beta later this year
 - Already available to working group members
 - Please join us if you are interested!
- See Fraunhofer's tutorial (coming up next here!)
 "UVM Goes Universal Introducing UVM in SystemC"





Advancing Standards Together

- Share your experiences
 - Visit <u>www.accellera.org</u> and register to post on community forums at <u>forums.accellera.org</u>
- Show your support
 - Record your adoption of standards
- Become an Accellera member
 - Join working groups
- Join SystemC Birds-of-a-Feather Meeting today!
 - − 18:30 − 19:30, room forum 8
 - Current and future needs for SystemC/TLM,
 SystemC and C++14, ... and your favorite topics!





Questions



