

Accellera Systems Initiative SystemC Standards Update

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Presentation Overview

- Accellera Overview
 - Membership list
 - How to join a WG
 - Global SystemC events
- Number of IEEE-1666 standard downloads
- Accellera SystemC Working Group updates
 - Language & Transaction-Level Modeling
 - Configuration, Control & Inspection
 - Synthesis
 - Analog/Mixed-Signal
 - Verification

All Members Can Join SystemC WGs!

Corporate Members

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ARM

cadence

ERICSSON

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semiconductor

intel

Mentor
Graphics

NXP

QUALCOMM

SONICS

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life.augmented

SYNOPSYS

TEXAS
INSTRUMENTS

Associate Members



AGNISYS
ACCELERATING DESIGN VERIFICATION

ALDEC
THE DESIGN VERIFICATION COMPANY

ALTERA

ANALOG
DEVICES

SPYGLASS
FROM ATRENTA



berkeley design
automation, inc.

BOEING

BROADCOM

dialog
SEMICONDUCTOR

DOULOS

Fraunhofer
IIS

IBM

Imagination

magi/em

NEC

NVIDIA

OFFIS
INSTITUTE FOR
INFORMATION TECHNOLOGY

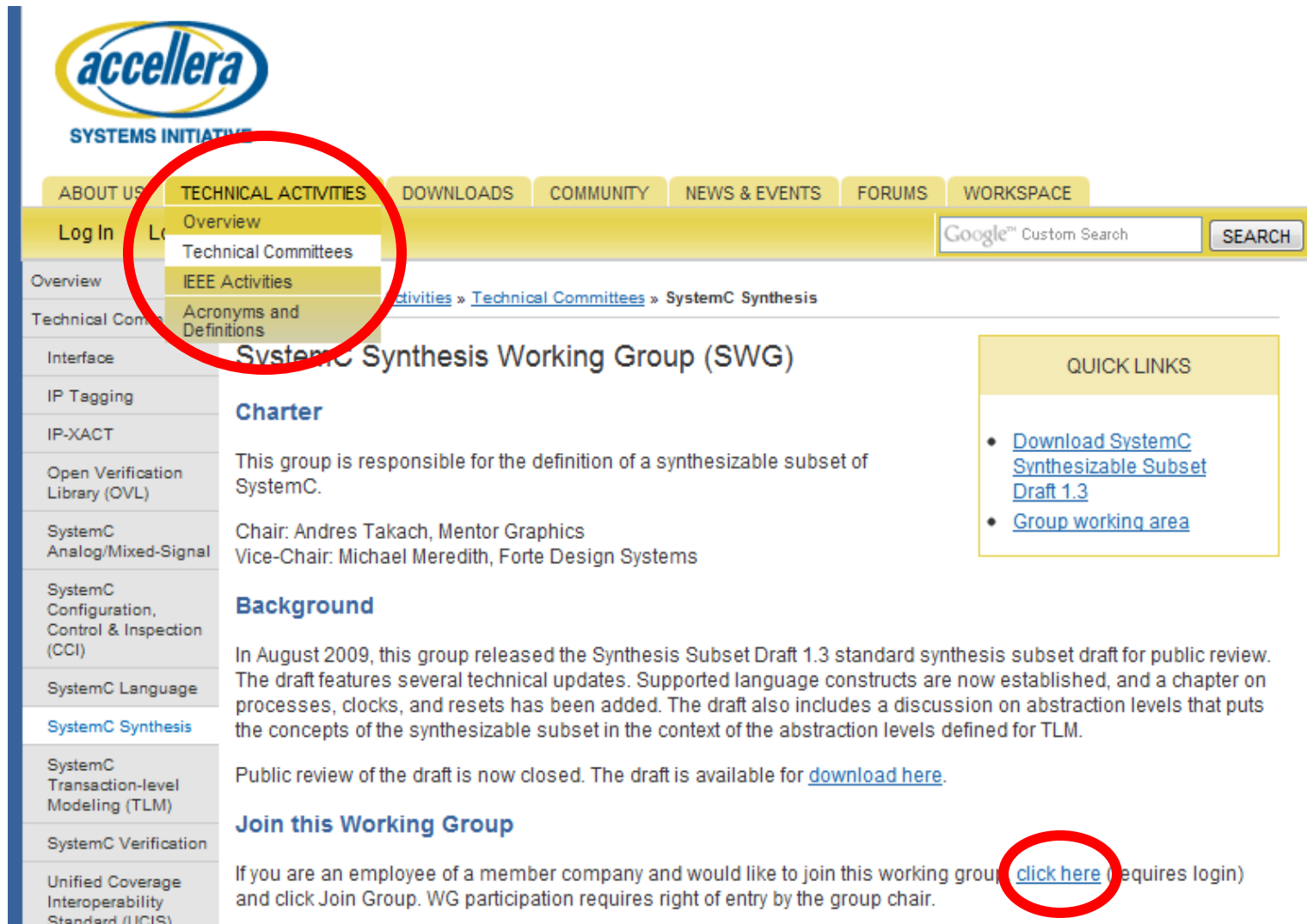
PARADIGM
WORKS

Semifore
The address map experts

UPMC
SORBONNE UNIVERSITÉS

XILINX

Join A Working Group And Contribute!



accellera
SYSTEMS INITIATIVE

ABOUT US | **TECHNICAL ACTIVITIES** | DOWNLOADS | COMMUNITY | NEWS & EVENTS | FORUMS | WORKSPACE

Log In | **Overview** | Technical Committees | IEEE Activities | Acronyms and Definitions

Overview | Technical Committees | Interface | IP Tagging | IP-XACT | Open Verification Library (OVL) | SystemC Analog/Mixed-Signal | SystemC Configuration, Control & Inspection (CCI) | SystemC Language | **SystemC Synthesis** | SystemC Transaction-level Modeling (TLM) | SystemC Verification | Unified Coverage Interoperability Standard (UCIS)

Activities » Technical Committees » SystemC Synthesis

SystemC Synthesis Working Group (SWG)

Charter

This group is responsible for the definition of a synthesizable subset of SystemC.

Chair: Andres Takach, Mentor Graphics
Vice-Chair: Michael Meredith, Forte Design Systems

Background

In August 2009, this group released the Synthesis Subset Draft 1.3 standard synthesis subset draft for public review. The draft features several technical updates. Supported language constructs are now established, and a chapter on processes, clocks, and resets has been added. The draft also includes a discussion on abstraction levels that puts the concepts of the synthesizable subset in the context of the abstraction levels defined for TLM.

Public review of the draft is now closed. The draft is available for [download here](#).

Join this Working Group

If you are an employee of a member company and would like to join this working group, [click here](#) (requires login) and click Join Group. WG participation requires right of entry by the group chair.

QUICK LINKS

- [Download SystemC Synthesizable Subset Draft 1.3](#)
- [Group working area](#)

SystemC Community

- Online at <http://accelera.org/community/systemc>
- Community forums, upload area for contributions, SystemC news

The screenshot shows the SystemC Community website. On the left is a navigation menu with links: Overview, SystemC, About SystemC, SystemC TLM, SystemC AMS, SystemC CCI, and UVM. The main content area has a breadcrumb trail: Home » Community » SystemC. Below this is the 'SystemC' title and a paragraph describing the language: 'SystemC addresses the need for a system design and verification language that spans hardware and software. It is a language built in standard C++ by extending the language with a set of class libraries created for design and verification. Users worldwide are applying SystemC to system-level modeling, abstract analog/mixed-signal modeling, architectural exploration, performance modeling, software development, functional verification, and high-level synthesis.' To the right of the text is the SystemC logo. Further right is a 'COMMUNITY LINKS' box containing a list of links: Download SystemC, Forums, Uploads, Working Groups (with sub-links for Language, AMS, TLM, CCI, Synthesis, and Verification).

Overview

SystemC

About SystemC

SystemC TLM

SystemC AMS


SystemC CCI

UVM

Home » Community » SystemC

SystemC

SystemC addresses the need for a system design and verification language that spans hardware and software. It is a language built in standard C++ by extending the language with a set of class libraries created for design and verification. Users worldwide are applying SystemC to system-level modeling, abstract analog/mixed-signal modeling, architectural exploration, performance modeling, software development, functional verification, and high-level synthesis.



COMMUNITY LINKS

- Download SystemC
- Forums
- Uploads
- Working Groups
 - Language
 - AMS
 - TLM
 - CCI
 - Synthesis
 - Verification

Global SystemC Presence 2014+

- DVCon USA March in Silicon Valley
- DAC June in San Francisco
- **DVCon India** September in Bangalore
- **DVCon Europe** October in Munich
- SystemC Japan June 19, 2015
- Accellera Day Taiwan 1st half of 2015



IEEE 1666 SystemC Downloads

IEEE STANDARDS ASSOCIATION



IEEE Standard for Standard SystemC® Language Reference Manual

IEEE Computer Society

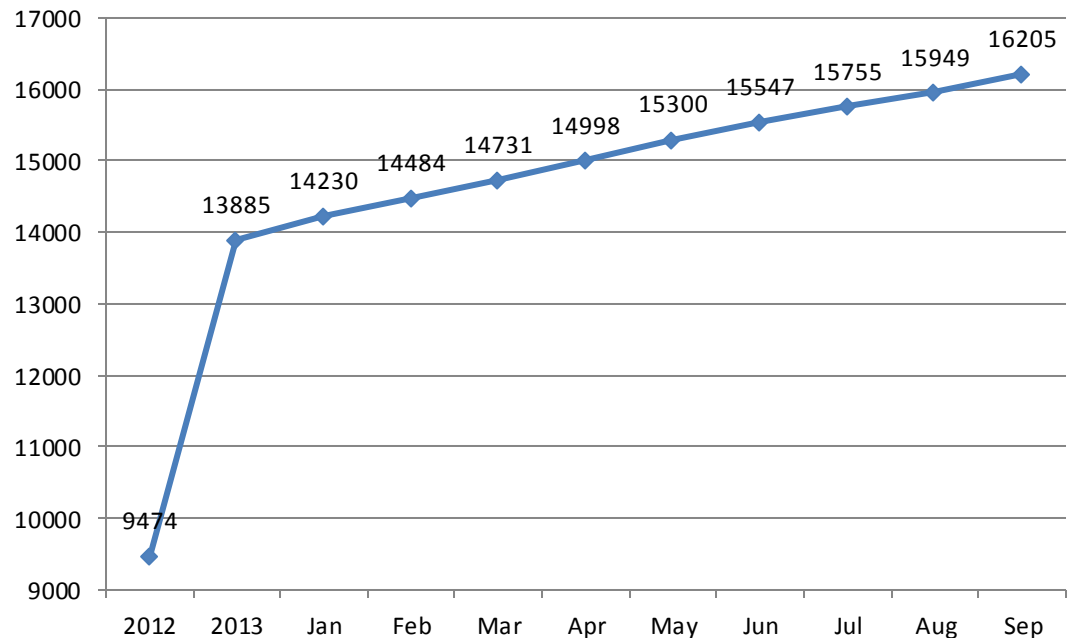
Sponsored by the
Design Automation Standards Committee

IEEE
3 Park Avenue
New York, NY 10016-5997
USA

9 January 2012

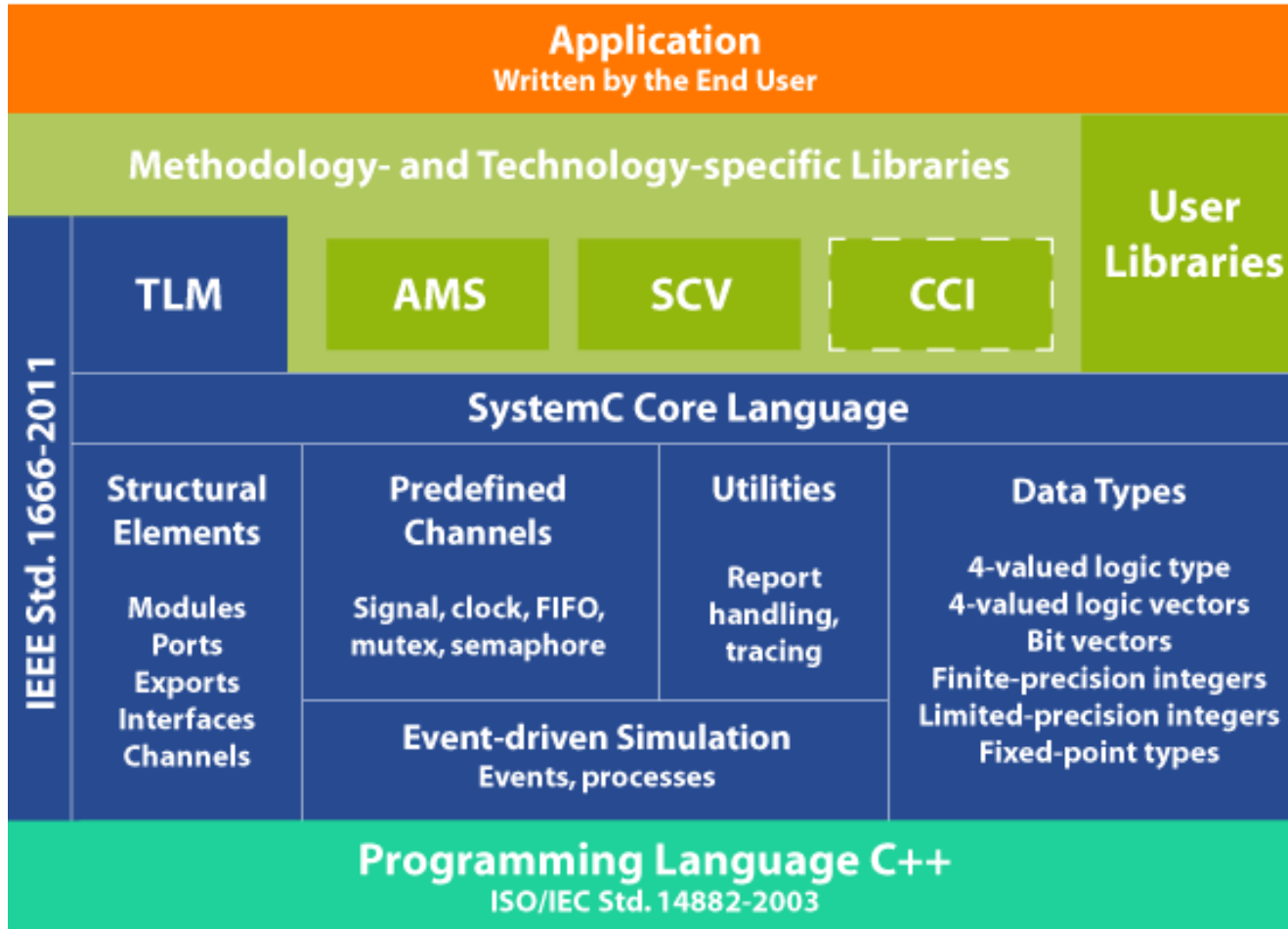
IEEE Std 1666™-2011
(Revision of
IEEE Std 1666-2005)

Cummulative Downloads - 2012-14



<http://standards.ieee.org/getieee/1666/download/1666-2011.pdf>

SystemC Overview



--- CCI standardization effort is underway

SystemC Language & TLM WG

- **Charter:** Responsible for the definition and development of the SystemC core language, the foundation on which all other SystemC libraries and functionality are built.
- **Current status**
 - Maintenance release version 2.3.1 of the proof-of-concept simulator in April 2014 (bug fixes, experimental features)
- **Plans for 2014/2015**
 - Discuss new concepts affecting simulation performance
 - Collect, address, refine proposals and errata towards IEEE 1666-201x

SystemC 2.3.1 Maintenance Release

- Release of 2.3.1 in April 2014
 - Bug fixes for known issues wrt. IEEE 1666-2011
 - Some feature additions beyond IEEE 1666-2011 (may require explicit configuration during library build)
 - Code cleanups, deprecation of non-standard features
 - Support for 64-bit builds on Windows

2.3.1

Closed on 7 Feb ⓘ Last updated about 5 hours ago

Maintenance release

100% complete 0 open 71 closed

[Edit](#) [Mark as open](#) [Delete](#)

Roadmap for IEEE 1666-201x

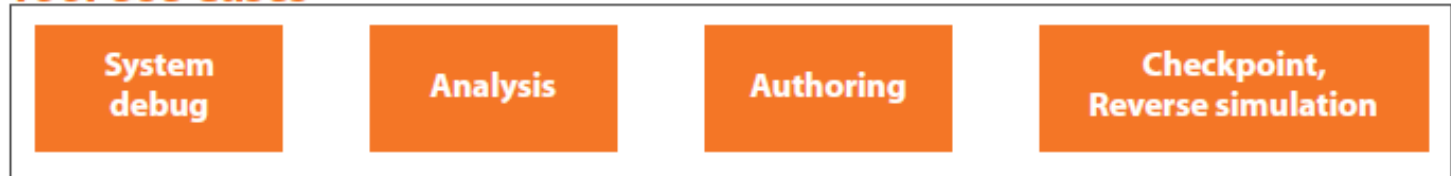
- Next IEEE 1666 update later this decade
 - Several errata and proposals already addressed in 2.3.1
 - Formal standardization will be moved to IEEE when sufficient input is available
- LWG/TLMWG are currently collecting proposals
 - Report your favorite missing feature/extension/annoyance
 - Non-Accellera members can use the community forums
- Parallelization of SystemC could be significant driver
 - More contributors needed!

SystemC Synthesis WG

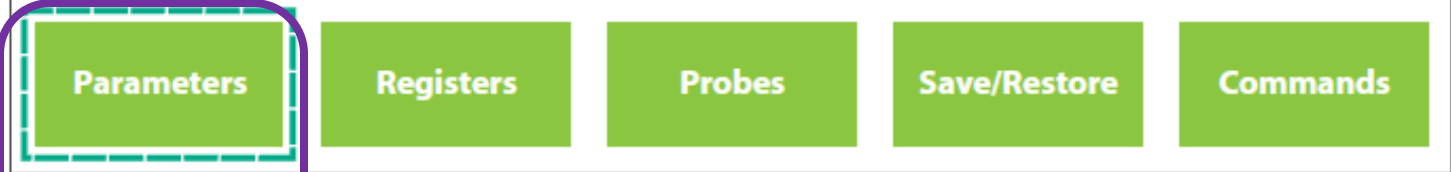
- Charter: To define the SystemC synthesis subset to allow synthesis of digital hardware from high-level specifications.
- Current status
 - Release of standard targeted for Q2 2015
 - www.accellera.org/apps/org/workgroup/swg
- **Plans for 2014/2015**
 - Release draft of standard for public review in 2014
 - Process feedback from review in Q1 2015
 - Start work on new topics for the second version of the standard

Configuration, Control & Inspection WG

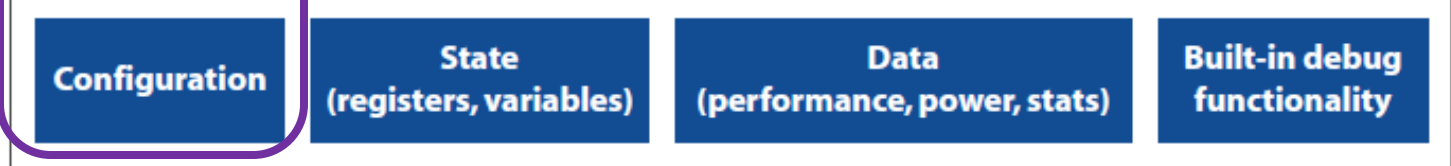
Tool Use Cases



Standard Interfaces



Model Information



WG is defining these

Initial Focus

Goal: Standardizing interfaces between models and tools

CCI WG Status

- WG reconvening in October 2014
- Configuration draft standard status
 - Requirements specification, available on Accellera web site
 - Initial LRM, 37 pages
 - POC Implementation
 - Educational examples
 - Key improvements identified
 - Technical previews available:
 - ISCUG '13: http://www.iscug.in/iscug2013_agenda_tutorials
 - DVCON '13: <http://events.dvcon.org/events/proceedings.aspx?id=144-2-T>
- Focus now on finalizing draft standard for public review
 - Schedule available once the pool of contributing resources is better understood

SystemC Analog/Mixed-Signal WG

- **Charter:** The SystemC AMS Working Group is responsible for the standardization of the SystemC AMS extensions, defining and developing the language, methodology and class libraries for analog, mixed-signal and RF modeling in SystemC
- **Current status**
 - Released the SystemCAMS 2.0 standard in March 2013
- **Plans 2014/2015**
 - Publish User's Guide update based on SystemCAMS 2.0
 - IEEE P1666.1 SystemCAMS Working Group started –
Accellera contributed SystemCAMS standard to IEEE-SA

SystemC Verification WG

- **Charter:** The Verification Working Group (VWG) is responsible for defining verification extensions to the SystemC language standard, and to enrich the SystemC reference implementation by offering an add-on libraries (SystemC Verification (SCV) library, etc.) to ease the deployment of a verification methodology based on SystemC.
- **Current Status**
 - Released version 2.0 of SystemC Verification library (SCV) in April 2014
- **Plans for 2014/2015**
 - Integrate the UVM verification methodology in SystemC
 - Standardization of coverage APIs (coverage groups, bins, etc.)
 - Further explorations of needs regarding SystemC/TLM

UVM SystemC

- New standard under discussion in VWG
- Materializes the UVM methodology natively in SystemC
- Language Reference Manual under review/discussion right now
 - Please join us if you are interested!
- Open source proof-of-concept implementation to be donated later this year
- See Fraunhofer's tutorial (coming up next here!)

Advancing Standards Together

- Share your experiences
 - Visit www.accellera.org and register to post on community forums at forums.accellera.org
- Show your support
 - Record your adoption of standards
- Become an Accellera member
 - Join working groups