

A Systematic Take on Addressing Dynamic CDC Verification Challenges

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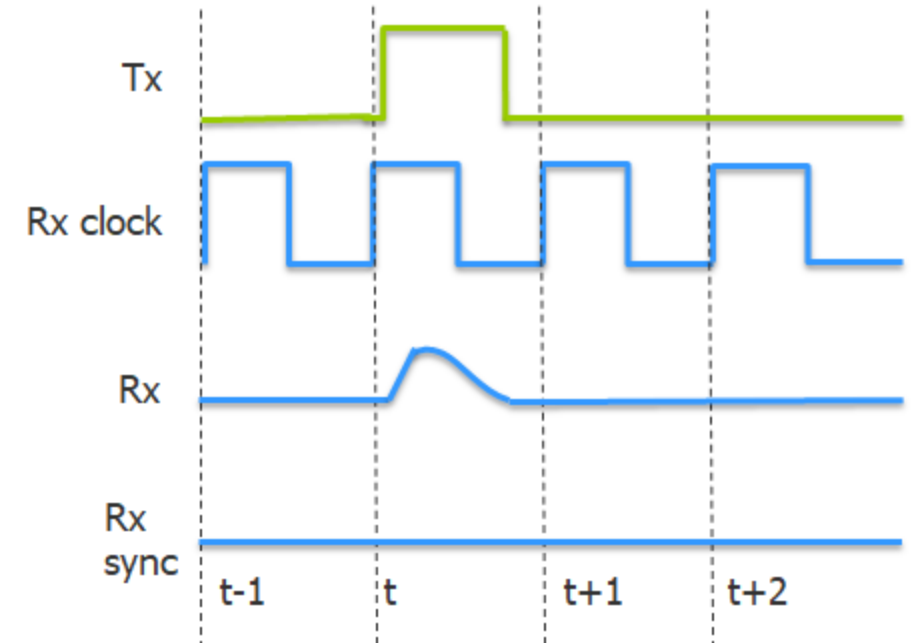
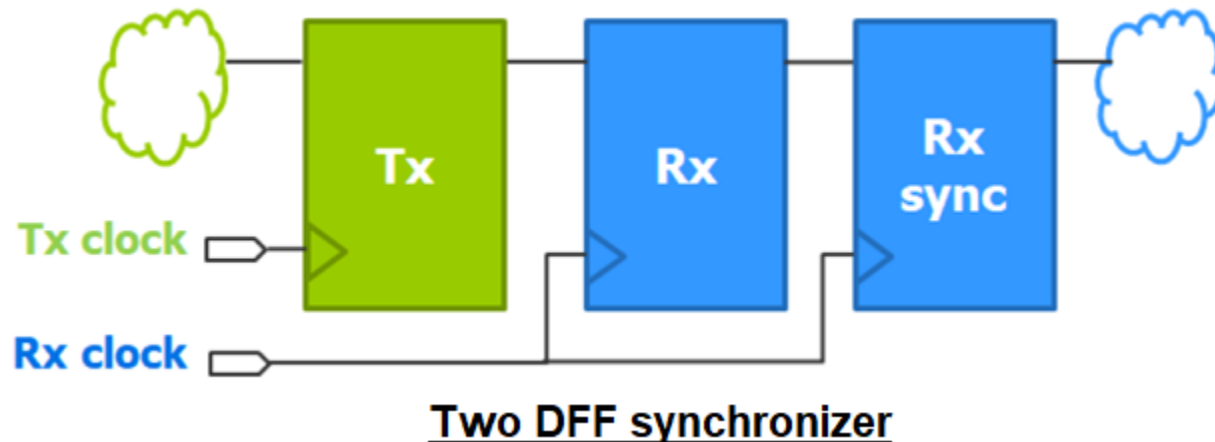
Introduction

- CDC issues: 2nd most common reason for silicon re-spins
 - Incorrect logic propagation across CDC paths
 - Results in functional failure of design
 - Synchronizers mitigate problem but **protocols** should be followed
- Dynamic CDC Protocol Verification essential
 - Synchronizer unreliable if protocols are violated
 - Crucial to validate synchronizer protocols for reliability

Synchronizer Protocol Violation

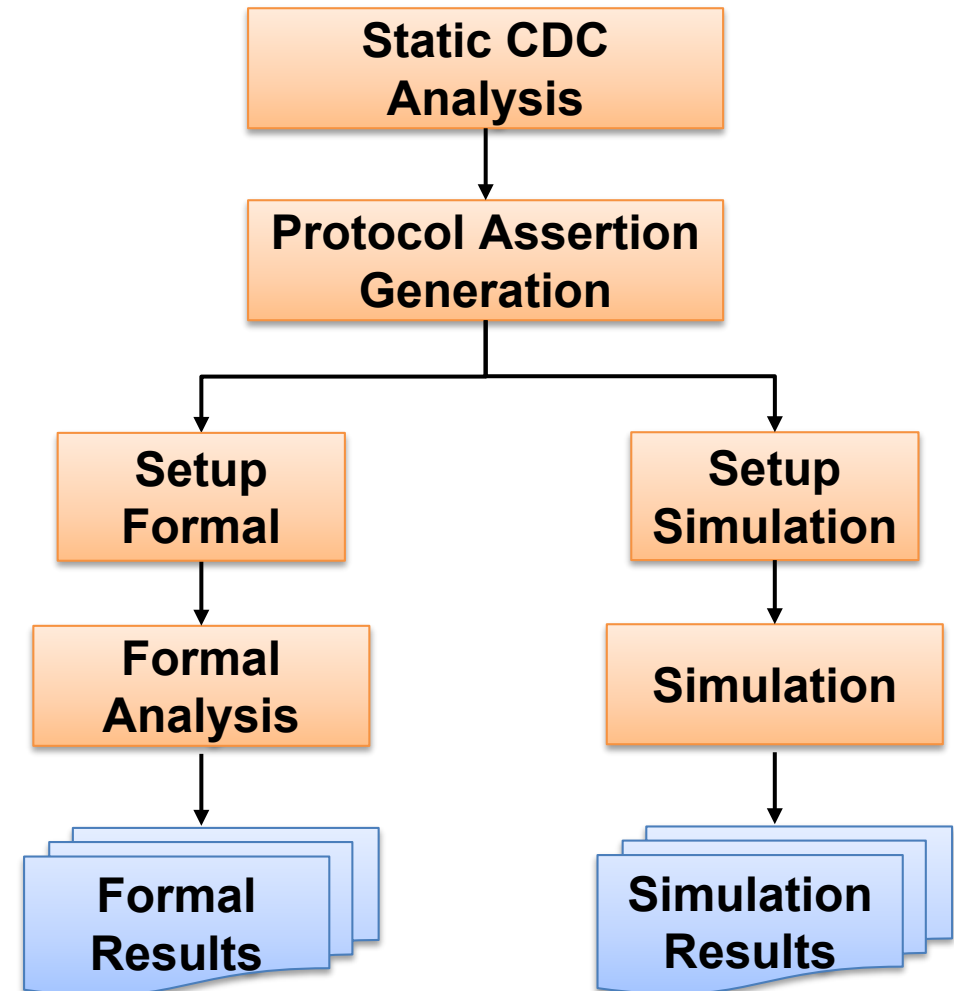
- Reliability of synchronizer depends on some assumptions or **protocols**
- Example: Two DFF synchronizer protocol violation
 - Data loss as input of two DFF synchronizer stable for less than two clock cycles
 - Data stability protocol violation (NUM_CYCLES = 2)

```
property data_stable_prop(data, clock, reset, areset, NUM_CYCLES);
    @(posedge clock) disable iff(areset)
    ##1 !reset && $changed(data) |=> $stable(data)[*(NUM_CYCLES-1)];
endproperty
```



Existing Verification Methodology

- Perform static CDC analysis
- Generate assertions for protocols of synchronizers
- Validate assertions in formal
 - Setup design for formal
 - Perform formal analysis
- Validate assertions in simulation
 - Setup design for simulation
 - Simulate design

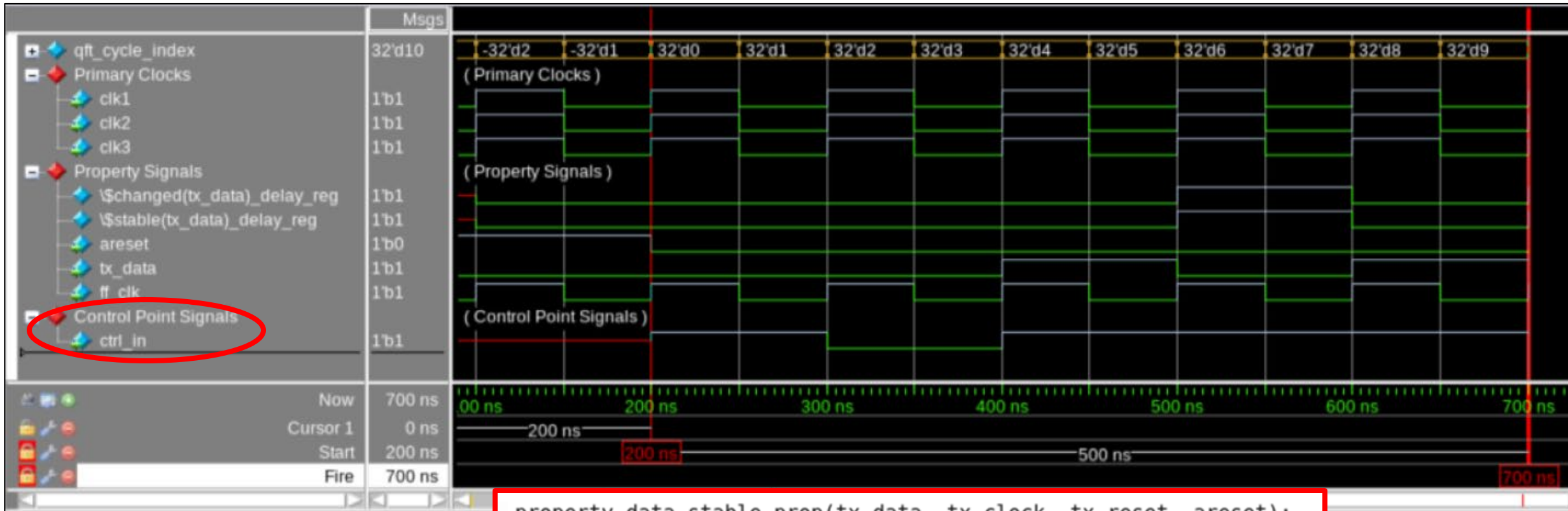


Challenges with Existing Methodology

- Setup design for Formal, Simulation
 - Effort, time for translating CDC design setup to both environments
- Debug effort to review firings in Formal, Simulation
 - Technical expertise of both environments
 - False firings if errors during translating design setup
- Correlating assertions results in Formal, Simulation to CDC
 - Coverage, review of CDCs is cumbersome for complex crossings
- No re-utilization of benefits, efforts of Formal, Simulation
 - Simulation: More intuitive to understand but coverage issues
 - Formal: Offers exhaustive proofs but infrastructural, capacity issues
 - Formal proven assertions revalidated in Simulation

Setup, Debug Challenge (1)

- Example: False two DFF synchronizer protocol firing in Formal
 - Data stability check firing due to change in value of 'ctrl_in' signal

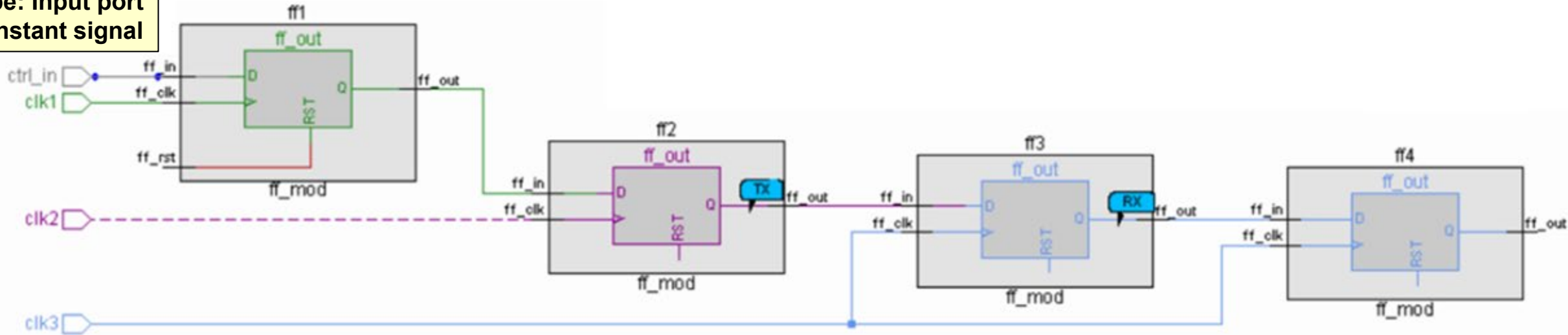


```
property data_stable_prop(tx_data, tx_clock, tx_reset, areset);
    @(posedge tx_clock) disable iff(areset)
    ##1 !tx_reset && $changed(tx_data) |=> $stable(tx_data)[*(1)];
endproperty
```

Setup, Debug Challenge (2)

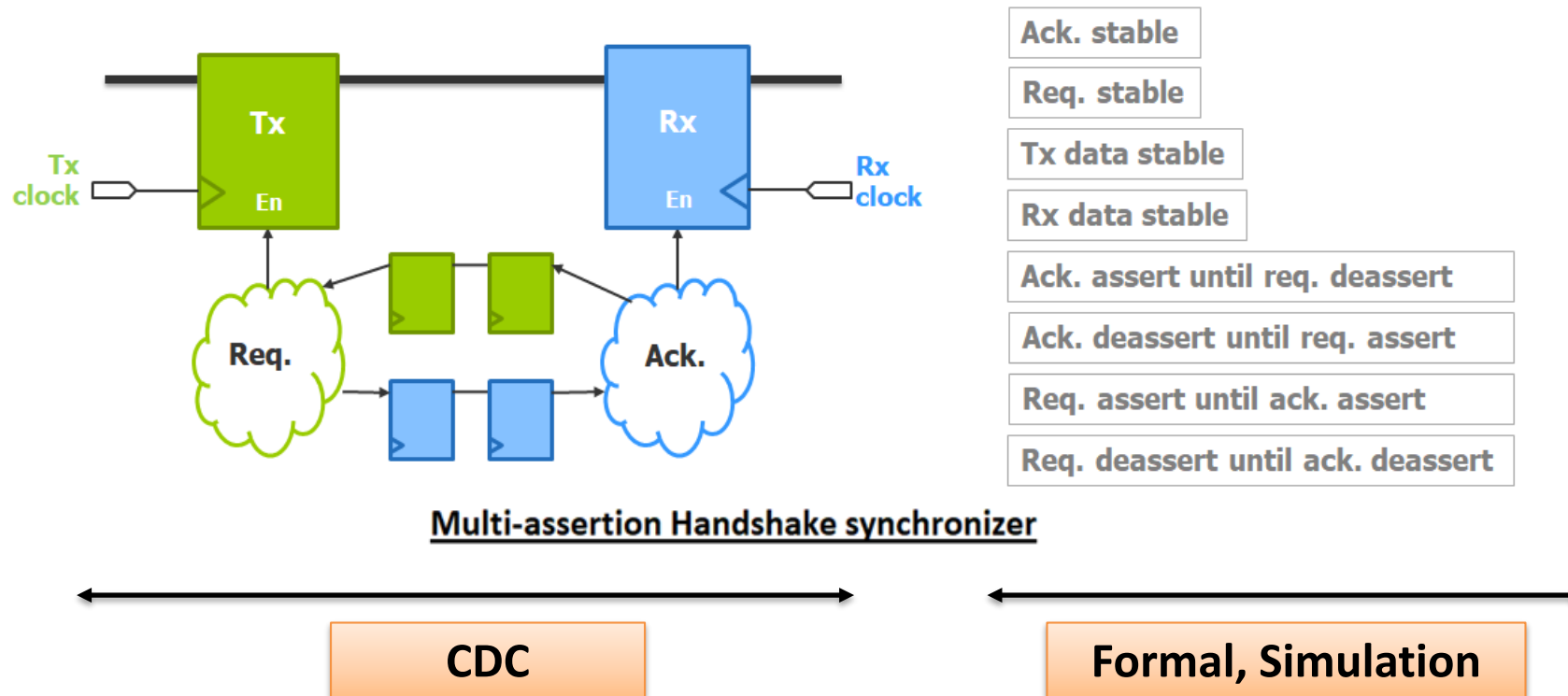
- False firing due to incomplete setup for Formal
 - Constant specified on input signal 'ctrl_in' during static CDC
 - Setup issue: Constant value missing from formal setup
 - Debug effort required for false firing caused due to incomplete setup

Signal: ctrl_in
 Type: Input port
 Constant signal



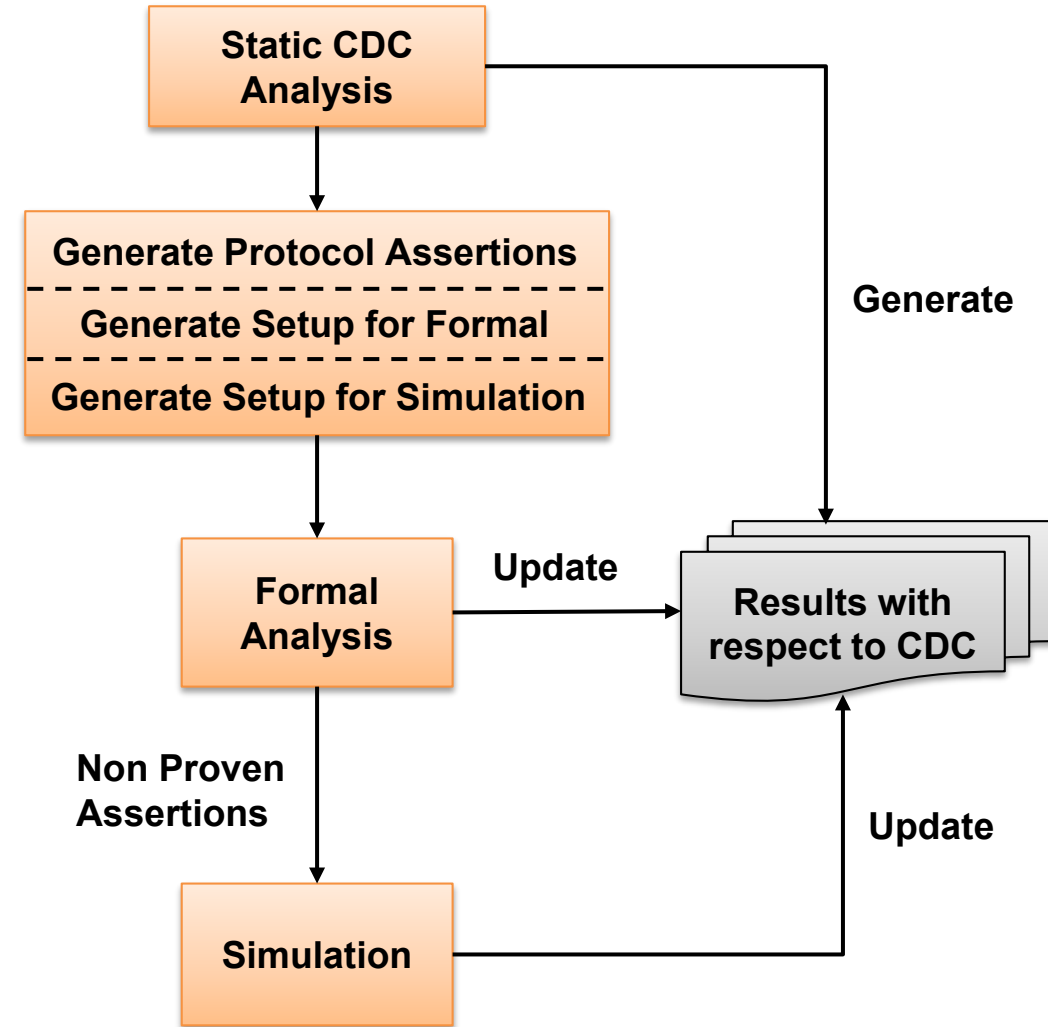
Correlation Challenge

- Formal, Simulation environments very different from CDC
- Complex synchronizers have multiple assertions
 - Treated as separate entities in Formal, Simulation but relate to a single CDC
 - Correlating results is cumbersome, time consuming
 - Errors during result correlation can lead to missed bugs



Proposed Verification Methodology

- Perform static CDC analysis
- Generate:
 - Assertions for synchronizer protocols
 - Setup for Formal
 - Setup for Simulation
- Validate assertions in formal
 - Formal analysis using generated setup
- Validate assertions in simulation
 - Simulate design using generated setup
 - Only formal non-proven assertions







Verification Methodology

- Automated design setup for Formal & Simulation
 - Static analysis setup parsed & converted to constraints
- Reduced formal firing debug effort
 - Unconstrained formal firings do not reflect real design behavior
- Formal & simulation results correlated to CDC paths
 - Enables faster review of CDC paths, coverage closure
 - Avoids manual correlation of assertion results required
- Leverage formal efforts in simulation
 - Formally proven assertions not exported to simulation

Correlated Results View

- Formal, Simulation results correlated to CDC
 - Enables faster review of CDC paths, coverage closure
 - No manual correlation of assertion results required

CDC Protocol Results			
CDC ID	Protocol ID	Formal Result	Simulation Result
handshake_7492	cdc_protocol.handshake_7492	Fired	Fired
bus_two_dff_1183	cdc_protocol.bus_two_dff_1183	Fired	Covered
handshake_5883	cdc_protocol.handshake_5883	Inconclusive	Uncovered
two_dff_19174	cdc_protocol.two_dff_19174	Inconclusive	Covered
bus_two_dff_4271	cdc_protocol.bus_two_dff_4271	Proven	-
fifo_2332	cdc_protocol.fifo_2332	Proven	-
two_dff_68078	cdc_protocol.two_dff_68078	Proven	-

			
CDC	Protocol Assertion Generation	Formal	Simulation

Comparative Results of Methodologies (Formal)

FORMAL RESULTS USING EXISTING METHODOLOGY

CDC Protocol Verification with Formal						
Design	Setup Time	Assertions			Run Time	Coverage
		Total Generated	Failed	Proven		
A	1w 3d	170	79	91	24s	100%
B	2w 2d	800	304	437	5hrs	92.60%
C	5w 4d	8552	5673	877	7hrs	76.60%

Reduction in setup time

Reduction in false firings

Coverage indicates actual scenario

CDC Protocol Verification with Formal						
Design	Setup Time	Assertions			Run Time	Coverage
		Total Generated	Failed	Proven		
A	2d	170	32	138	55s	100%
B	5d	800	119	654	6hrs	96.60%
C	1w	8552	1825	4907	10hrs	78.70%

FORMAL RESULTS USING PROPOSED METHODOLOGY

Comparative Results of Methodologies (Simulation)

SIMULATION RESULTS USING EXISTING METHODOLOGY

CDC Protocol Verification with Simulation (after Formal)					
Design	Setup Time	Assertions		Run Time	Coverage
		Total Simulated	Failed		
A	10min	170	14	15min	85.90%
B	17min	800	83	25min	84.50%
C	30min	8552	127	50 min	77.20%

Reduction in setup time

Formal effort utilization

Coverage indicates actual scenario

CDC Protocol Verification with Simulation (after Formal)					
Design	Setup Time	Assertions		Run Time	Coverage
		Total Simulated	Failed		
A	1min	32	14	15min	84.40%
B	1min	146	83	25min	82.90%
C	5min	3645	127	50 min	62.30%

SIMULATION RESULTS USING PROPOSED METHODOLOGY

Conclusion

- Dynamic CDC Protocol Verification is crucial
 - CDC bugs missed if synchronizer protocols not validated
- Proposed methodology helps achieve faster design closure
 - Significant reduction in verification time, effort
 - Reduced chances of error as automated setup generation
 - Helps overcome challenges of Formal, Simulation methods
 - Enables benefit, effort utilization of both methods
 - Seamless to adopt

Questions?