

A Novel Variation-Aware Mixed-Signal Verification Methodology to achieve High-Sigma Variation coverage at nanometer designs

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Abstract- Variation analysis is significantly important in modern nanometer process geometries. Traditional verification approaches to analyze statistical variations are time consuming and provides inadequate coverage. In this paper we discuss a novel ‘variation aware mixed signal verification’ methodology that relies on designers knowledge and use of machine learning based EDA tools. This approach is applied for a Time-Domain 2-step ADC architecture which is used in automotive RADAR application and is fabricated with 22nm FDSOI Global Foundry process.

I. INTRODUCTION

Analog-to-Digital Converters (ADCs) are prevalent in today’s SoC designs. The next-generation automotive, mobile and high-performance computing applications demand the use of nanometer nodes, to deliver more functionality and higher performance with lower power consumption. These ADCs have a very stringent specifications and are inherently mixed signal in nature and so their performance metric can be measured only by means of a mixed signal simulation, which can also verify the correctness of the design. . To produce a high yield design, designers need to perform extensive brute force mixed-signal simulations to account for all potential design variation. However, at advanced nodes, the number of process, voltage and temperature (PVT) corners and parametric variation grow exponentially making the simulation impractical and costly. Design teams are forced to adopt extrapolation methods to shorten the verification cycle and meet time to market demands, at the risk of impacting the design yield. This necessitates the need to develop a new methodology that can help achieve high sigma variation coverage in a mixed signal design without running millions of brute-force simulations.

II. MOTIVATION

The motivation for Time-Domain 2-step ADC architecture

The Analog Value team selected the Time-Domain 2-step ADC architecture for their client’s automotive RADAR application using a 22nm FDSOI Global Foundries process node. The traditional voltage domain high-resolution ADC at nanometer process nodes does not have enough dynamic range as the supply voltage level goes down. In contrast, the Time-domain 2-step ADC exhibits high resolution and better performance at nanometer nodes. This is achieved by converting the analog input into a time pulse and then digitizing it into digital codes [1]. The architecture consists of a substantial amount of digital logic content to perform the bubble correction encoding and manage the algorithms to avoid meta-stability [2]. The sensitive and high precision analog blocks, such as the comparator, are a vital part of this architecture. The dominance of and a bias towards digital design provides the opportunity to take advantage of automated design methodologies, resulting in high design efficiency and productivity. Recently, this has led to the proliferation of time-domain ADC circuits that are not dependent on the supply voltage, but take advantage of the benefits that come with high-performance nanometer nodes.

Figure 1 shows the Time-Domain 2-step ADC implemented by Analog Value. In the input stage (lower-left corner of the diagram) the voltage is converted to the time domain by using a pulse width modulation (PWM) technique so

that each sample of the input signal is transformed into a time difference between two signal edges. The voltage-to-time conversion and measurements are performed in two steps. Analogous to a measuring tape, with coarse and the fine divisions, the coarse time division is measured using the counters by counting the number of clock cycles. The fine time division is determined by using a set of close and equally distant clock phases. In this specific ADC, a set of 90 clock phases is used, and time resolution was approximately 5ps.

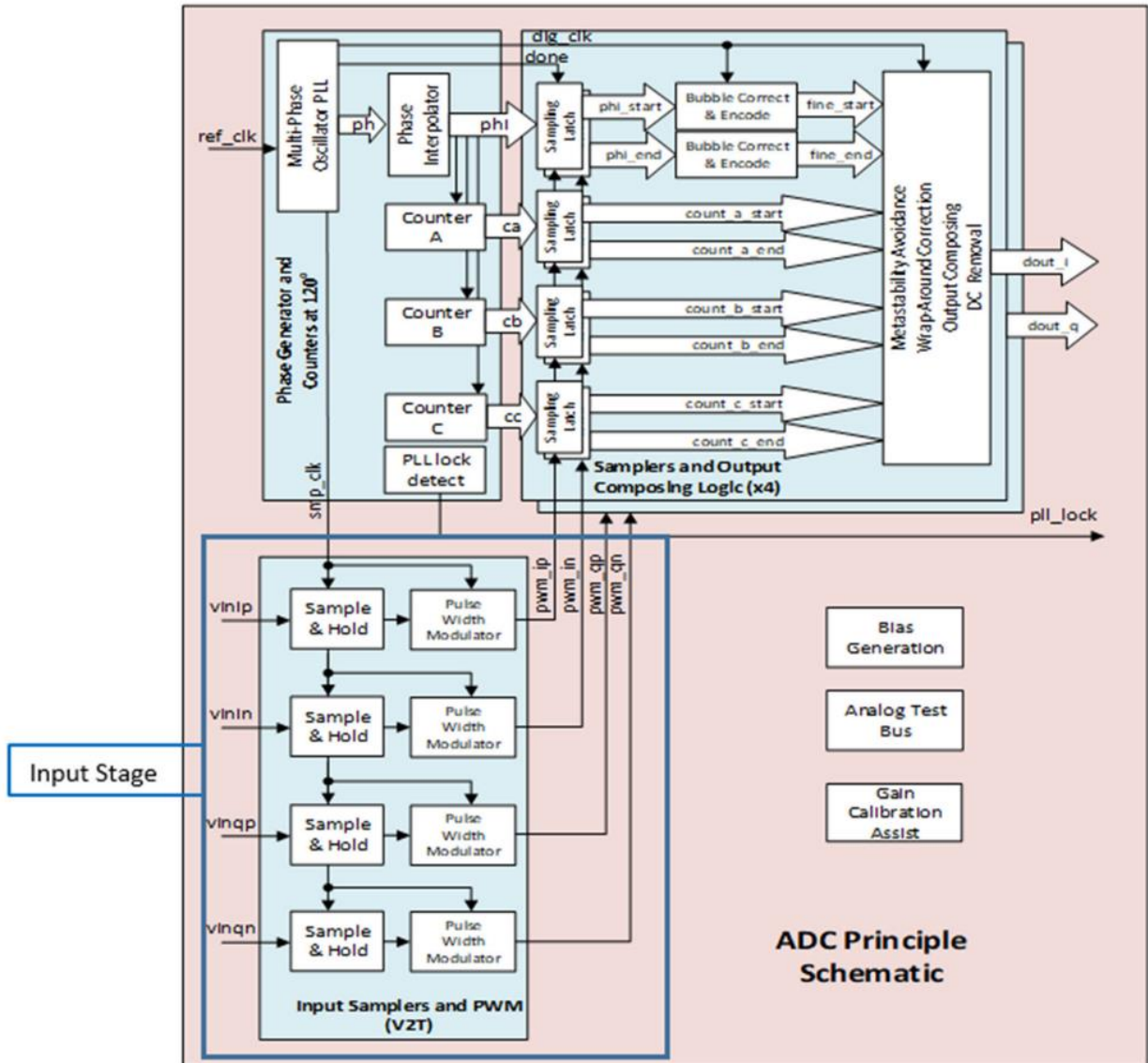


Figure 1: Time-Domain 2-step ADC block diagram

III. THE CHALLENGE

The challenges with the existing traditional statistical variation verification

The presence of interlaced analog-digital logic along with sensitive blocks such as comparators makes verification of these ADCs a very challenging task. One needs to rely on a mixed signal simulator for the functional verification of the top level design. However the key objective in this case-study was to measure the impact of the comparator-latch sub-block's statistical variation on the overall ADC's performance, measured in "effective number of bits"

(ENOB). Existing statistical variation verification methodology presented several challenges. (Table 1 shows the # of process corners and simulation parameter variation range)

Process corners	4
Voltage supply variation	+/-5%
Temperature	-40 and 125 °C

Table 1: Simulation parameters

Performing the full brute force SPICE accurate Monte Carlo simulation for all stages of the ADC is practically impossible as it required tens of millions of simulations. Design team could only run a limited set of brute force Monte Carlo simulations, 200 per corner, for a total of 3200 simulation. Then they used extrapolation to calculate the 4-sigma performance of the comparator-latch sub-block. However, to measure the influence of the comparator-latch statistical variation on the full ADC, design team could run only few top-level simulations. Extrapolation was again used to calculate the ADC's target 3-sigma performance, introducing the risk of compromising the accuracy of the results.

In addition, analyzing and identifying devices that are most sensitive to statistical variation and have the potential to cause functional failure in the ADC design was a considerable challenge. The synthesized digital block performing the bubble correct encoding was modeled in Verilog-A for top-level verification. Running SPICE-level simulation at the top using Verilog-A model was very slow and did not verify the actual logic circuit that will go into the chip.

IV. PROPOSED METHODOLOGY

It is clear from the above explanation that accessing the effect of a specific circuit element (comparator latch in this case) on the performance of the top level design over a large set of corners is not only cumbersome but also impractical to achieve by directly running mixed signal Monte Carlo simulations. To address this, in this section we propose a two-phase methodology that uses designer's knowledge and a machine learning based variation aware analysis tool in conjunction with a mixed signal simulator.

- (I) In phase one, designer define the performance metric of the component that will predominantly affect the performance of the whole design. In this case it is the standard deviation of the offset of the comparator. This is not done by any tool but is identified by the designer based on their knowledge of the design. Design team then starts with the verification of this sensitive component (comparator) using a machine learning based variation analysis tool. This tool generates Monte Carlo samples for a target sigma and runs those sample to build and verify a machine learning-based model. It then uses this model to identify the worst-case corners quickly (without running millions of brute-force simulations which are needed in traditional approach).
- (II) In phase two, design team then applied the worst-case corner extracted from comparator-latch simulation (in phase I) and performed 100 mixed-signal simulations at the top-level ADC to achieve the desired target 3-sigma variation coverage.

Phase 1: Verifying the Comparator Latch

For simulating the comparator-latch we apply a sine wave input and the required control signals generated by Verilog-A blocks (the 5 blocks at the middle of the schematics). On the left top corner we have the bias circuit with its two diode connected transistors. The latch itself is on the right side, connected to load capacitors and a bias resistor

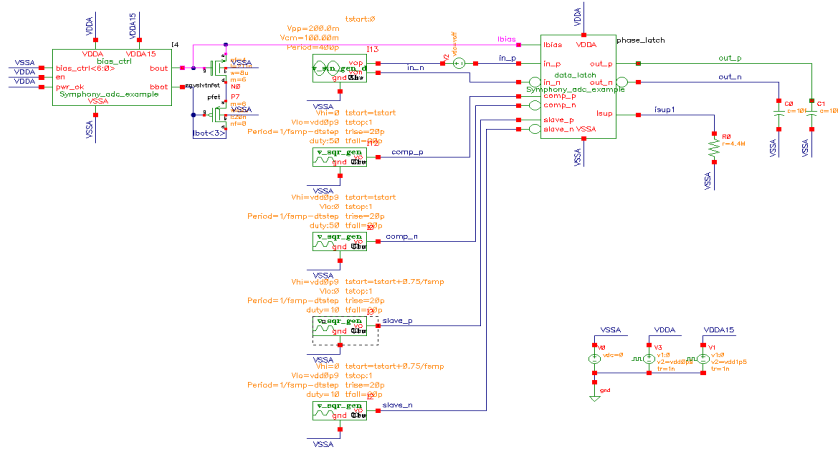


Figure 2: Latch Simulation Setup

As you can see in the Latch schematic (Fig. 3), input signals applied from the top, feed the gates of two PMOS devices. The conductivity of these two devices will determine the direction in which the cross-coupled regenerative feedback circuit (middle of the schematics) will flip. On the two sides (left and right) are level 2 digital latches for the positive and negative output signals.

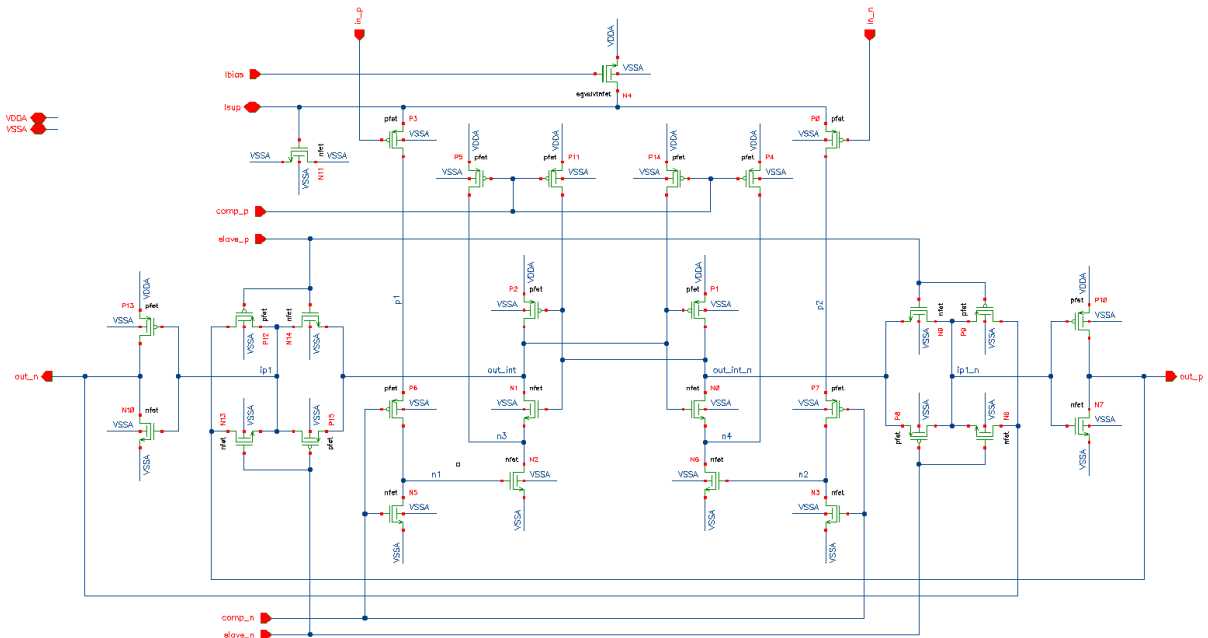


Figure 3: Latch Schematic

Analog Value used Mentor's Solido PVTMC Verifier tool to perform PVT corners and Monte Carlo simulation to accurately extract the worst-case corner for the comparator-latch offset at the target 4-sigma without using extrapolation.

The measurement of interest for the comparator-latch simulation with PVTMC Verifier is the maximum standard deviation of the Offset_ps and its impact on ENOB. Figure 4 shows the worst-case standard deviation. The standard deviation offset of 7.2ps is unacceptable given the ADC LSB is specified at 5ps.

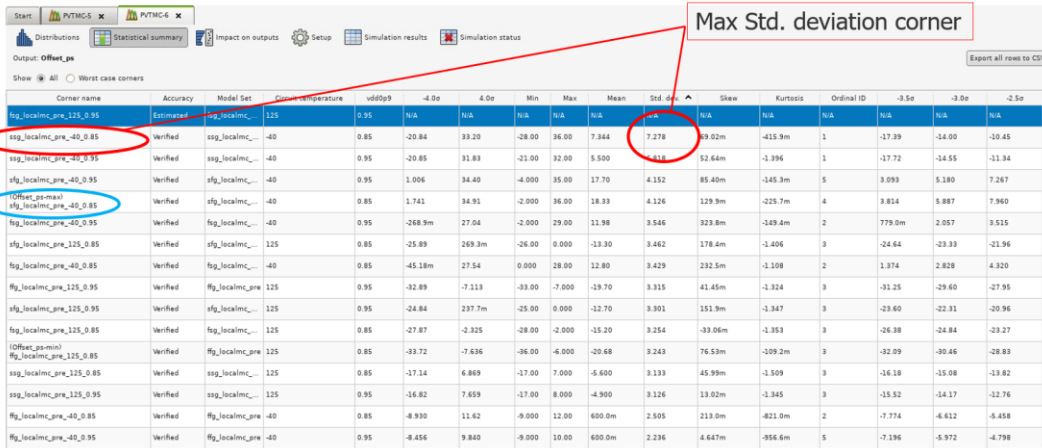


Figure 4: PVTMC Verifier statistical summary

This discrepancy in the resolution of the LSB was vital information for making design adjustments. The other key observation was that the quantile plot of Offset_ps (Figure 5) shows that the tail of the distribution is non-Gaussian. Hence, this is further validation that the existing statistical variation methodology based on extrapolation with the assumption that it is a Gaussian distribution would have led to inaccurate results, compromising the target yield of the ADC

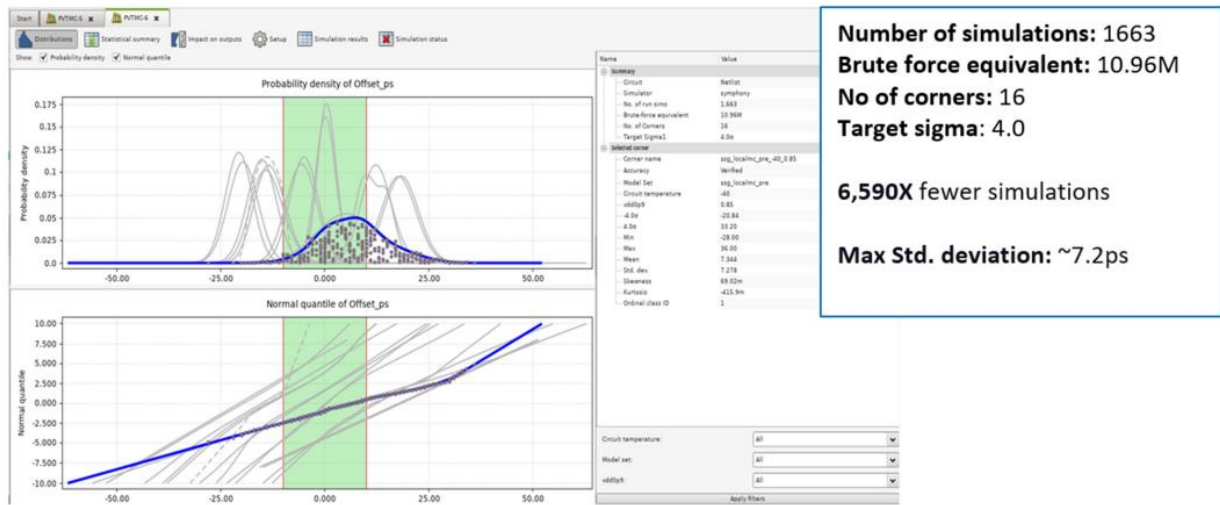


Figure 5: Comparator-latch PVTMC Verifier simulation results

Improving the Comparator Latch Design

The built-in sensitivity analysis capability in PVTMC Verifier helped identify the device in the comparator-latch with the most sensitivity to statistical variation and the most impact on the measured output. The designer gained insight on potential design adjustments to make and improve the performance of the comparator-latch design. In figure 6, the bar chart graph shows the device “phase latch p3” as the most sensitive to statistical variation. The scatter plot on the right shows its impact on the measured output offset.

boundary elements in the simulation. Figure 8 shows the Gaussian distribution and simulation results with an order-of-magnitude fewer simulations and the accuracy of brute force.

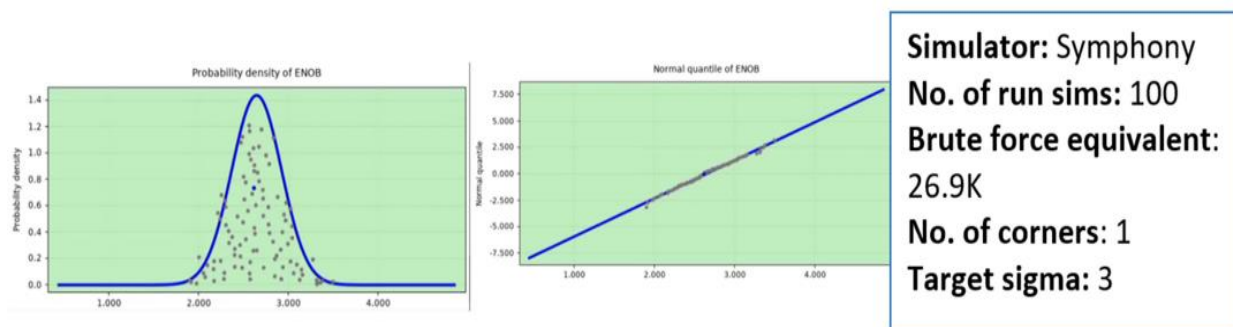


Figure 8: ADC top-level simulation results

The ENOB loss of ~ 1.5 LSB for the 12-bit ADC is required to achieve the performance specification of $\text{ENOB} \geq 10.5$ bit. PVTMC Verifier provided the full real 3-sigma simulation data to verify the ENOB result.

V. CONCLUSION

Analog Value's previous statistical variation verification methodology required extensive brute force simulation and extrapolation to calculate the target sigma performance at the analog sub-block level and for the top-level ADC. In addition, performing efficient variation-aware mixed-signal simulation with sensitivity analysis was not possible, thus introducing potential risk of missing the ADC design yield at nanometer nodes.

Analog Value and Mentor team established this new two-phase methodology that uses a machine learning based variation aware analysis tool in conjunction with a mixed signal simulator. The idea of these technology is to start by simulating a small amount of sample space and build an accuracy-aware ML model. This model can very quickly predict the outcomes for the rest of the variation space. It then use the predicted values to decide which cases are interesting and simulate those to assure that accuracy is achieved throughout the space without running expensive simulation for the entire space. This approach helped design team gained significant productivity boost with 6590X fewer simulations than brute force Monte Carlo at the target 4 sigma. Subsequently, for top-level ADC, which is a mixed signal design with RTL & Spice, the integrated Solido with Symphony enabled an accurate variation-aware mixed-signal verification. This methodology also helped identify the devices with the most sensitivity to variation. With this information, the design team easily and quickly made design adjustments to meet the ADC's performance and achieved high design yield.

REFERENCES

- [1] A New Highly-Linear Highly-Sensitive Differential Voltage-to-Time Converter Circuit in CMOS 65nm Technology 2015 (IEEE International Symposium on Circuits and Systems (ISCAS), At Lisbon).
- [2] Implementation of Mux Based Encoder for Time To digital Converters Architecture (International Journal of Engineering and Techniques - Volume 4 Issue 3, May 2018)