A concept for expanding a UVM testbench to the analog-centric toplevel

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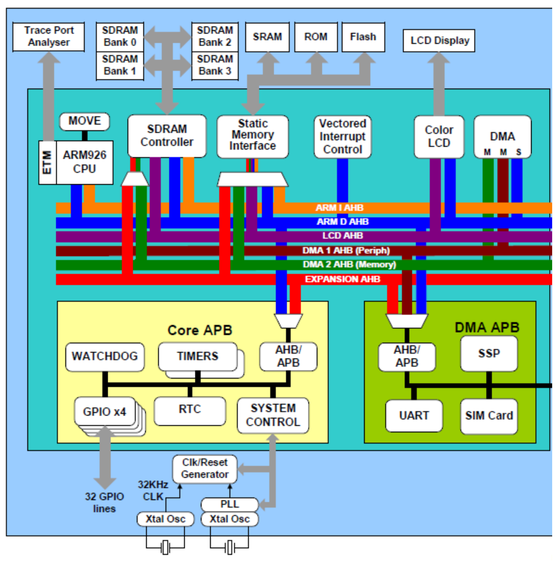
INTRODUCTION

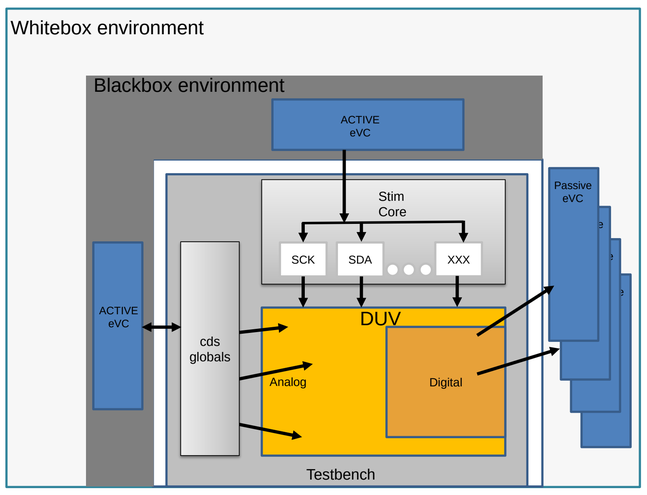
Challenges in todays mixed signal designs:

- Analog and digital together (highest complexity)
- DUV communicates via pins and protocols (SPI/I²C)
- Different verification scenarios like Wafer Level Test, Module Test or Normal operation
- NVM/RAM/EPROM/… need to be configured
- Analog-, digital- and verificationteam need to work closely
  - But everybody has a different understanding about verification
- How to bring everything together?



Requirements for an analog-centric verification environment

- Analog- and digitalteam need always working testbench
- Coverage and checks for verification team only
- Interactive features like register read/write or pin read/write
- Configurable testbench to cover different verification scenarios
- We need a special testbench architecture and an AMS driven simulation flow



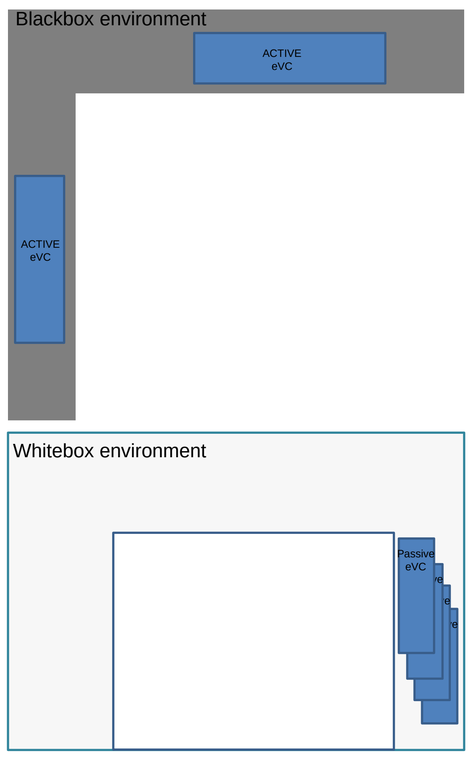
Blackbox/Whitebox approach

Blackbox:

- Testcase development
- Always working, contains interface UVC's only
- No checks
- Contains interactive command interface for debugging
- Contains configuration sequences
- Generates RAM and NVM
- For gate level

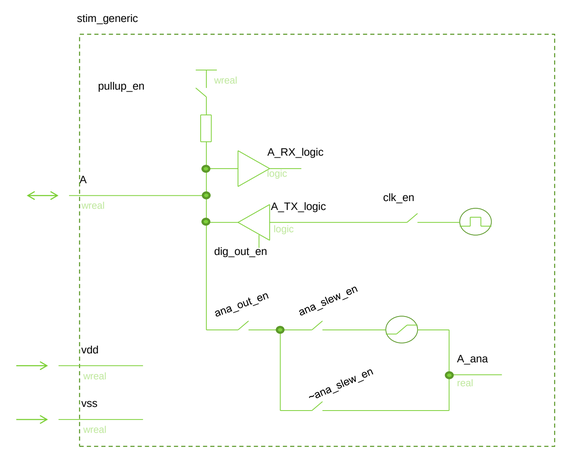
Whitebox:

- For regression
- Contains all UVC's
- Imports Blackbox for modular reuse
- All tests from Blackbox can be run in Whitebox
- All Blackbox features are usable



AMS driven simulation flow

- Generic pin modules (digital/analog stimulus, pullup, supply ramp, …)
- VAMS file to configure analog models (cds_globals), controlled by UVC
- Model analog sub blocks only (model as close as possible to transistor level)
- Supply sensitive connect modules
- Use of config views for netlisting to cover different scenarios



CONCLUSIONS

- One toplevel testbench
- Efficient testcase creation
- Efficient analog component adjustment
- Simulation time speedup (10s vs. 5min with different configurations)
- Analog-, digital- and verificationteam work closely together

Next steps:

- Verification of analog models
- Enhance interactive mode
- Testbench qualification

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