A Comprehensive Verification Platform for RISC-V based Processors

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Agenda

- Introduction
- Motivation
- Proposed Methodology
- Preliminary Results
- Conclusion
- Future Work

Introduction

- RISC-V ecosystem[1] enables SoC designers to benefit from
  - more than 100 core/SoC design and implementations
  - instruction set simulators
  - toolchains

- RISC-V ISA specification allows to extend the instruction set with specialized extensions[2,3]

- It is estimated that there will be about 62 billion RISC-V based CPU cores in the market by 2025[4,5].

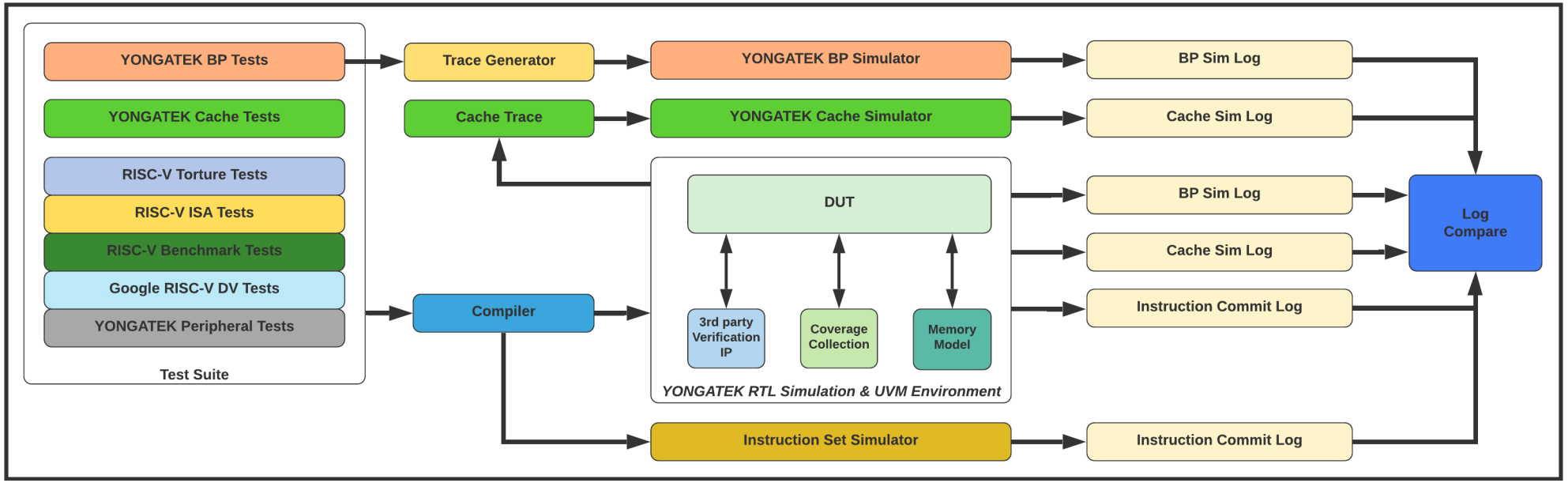
Motivation

- RISC-V's licensing model allows to reduce non-recurring engineering (NRE) costs
- There is no condition or restriction on how a RISC-V based system will be designed and implemented
- Verification of a RISC-V based SoC should not only include the verification of the core itself, but rather the verification of the whole system!

Proposed Methodology

- We present a comprehensive and UVM based RISC-V verification platform
- Our platform provides verification at both SoC, core, and block levels
- Module level verification of branch predictor and cache blocks
- Presents functional as well as stress tests in addition to standard test suites
- Provides a logging mechanism that includes committed instructions, cache transactions, branch predictor operations, etc.
- Supports debugging via OpenOCD + GDB + JTAG

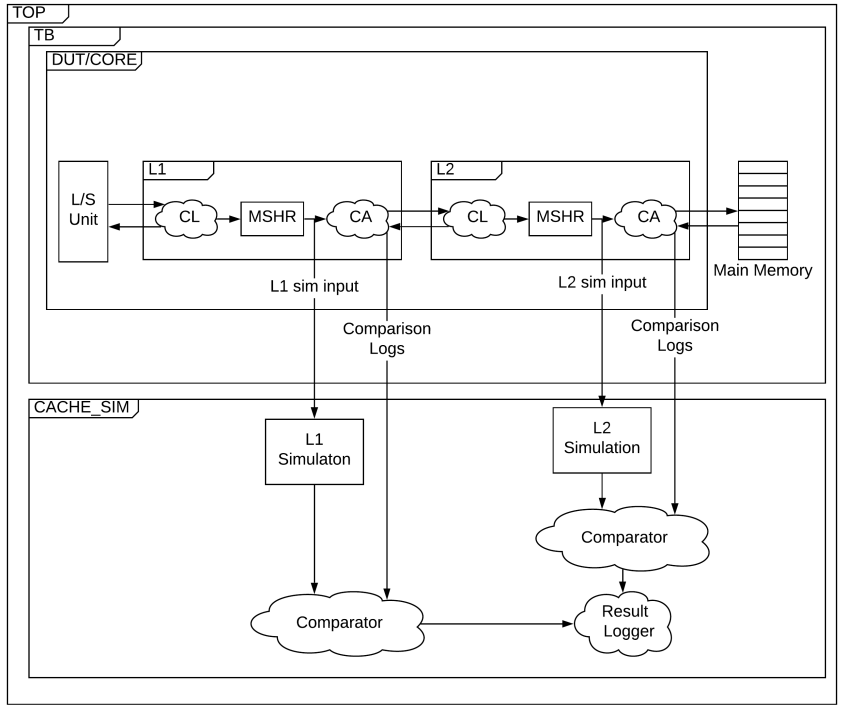
Proposed Methodology (cont'd)



YONGATEK RISC-V Verification Flow

Proposed Methodology (cont'd)

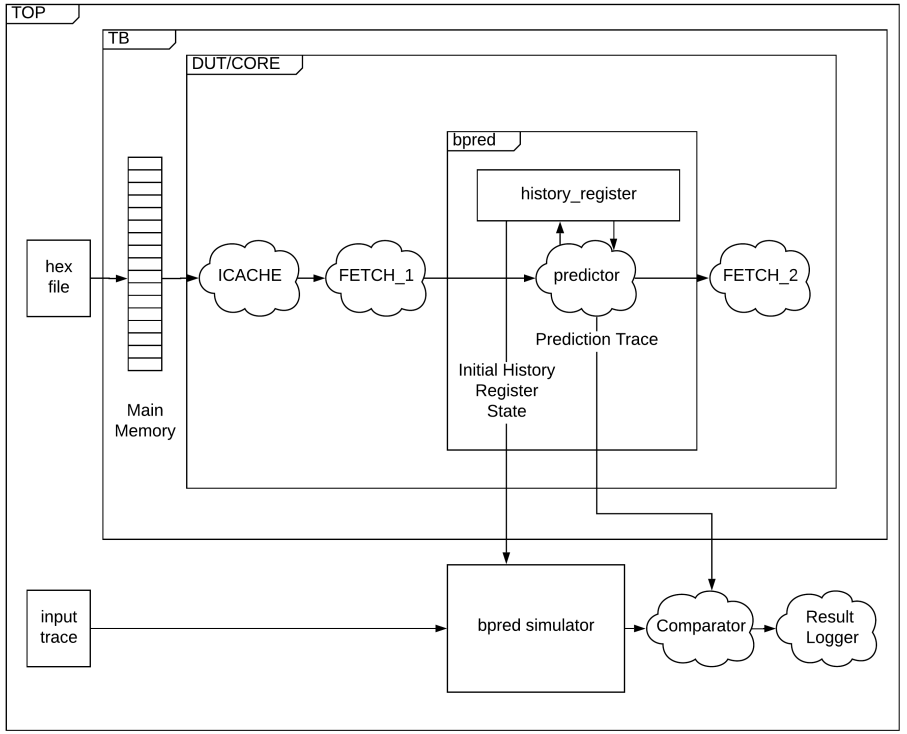
- Cache simulator
  - supports different cache configurations
  - placement: direct-mapped, set-associative, fully associative
  - replacement: random, LRU, FIFO
  - request handling: blocking/non-blocking
  - error handling: ECC
- Written in C++



Cache verification flow

Proposed Methodology (cont'd)

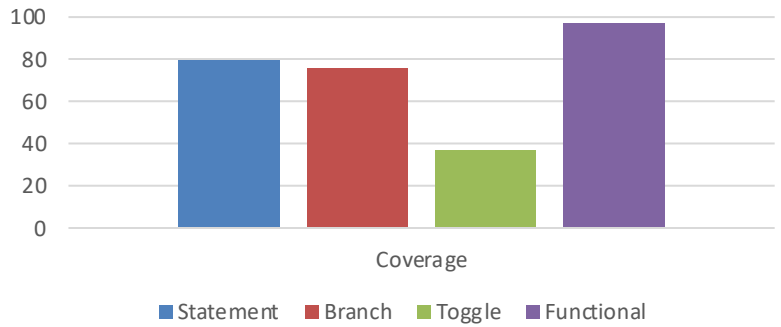
- Branch predictor simulator
  - supports bimodal, g-share, hybrid predictor models
- Written in C++



Branch predictor verification flow

Preliminary Results

- Regression consists of 300+ test cases
- Created about 10,000 covergroup elements, containing coverpoints and crosses
- Obtained on a customized SoC based on BOOM [24]



Code coverage and functional coverage

	Register Fields			
Instruction Type	Field #1	Field #2	Field #3	Field #4
LOAD	100.0	94.20	N/A	N/A
STORE	96.88	99.22	N/A	N/A
BRANCH	100.0	100.0	N/A	N/A
JALR	56.25	62.50	N/A	N/A
JAL	96.88	N/A	N/A	N/A
LOAD-FP	57.29	70.83	N/A	N/A
STORE-FP	46.88	68.75	N/A	N/A
OP	100.0	100.0	100.0	N/A
OP-32	100.0	100.0	100.0	N/A
OP-IMM	100.0	100.0	N/A	N/A
OP-IMM-32	100.0	100.0	N/A	N/A
OP-FP	94.06	92.50	90.56	N/A
AMO	12.07	4.38	13.07	N/A
(N)MADD/(N) MSUB	85.68	86.2	24.5	89.1

Instruction coverage

Conclusion

- Our verification platform
  - can support all the base instruction set and standard extensions of RISC-V ISA
  - provides verification at SoC, core, and block levels
  - gathers different features of different verification environments under a single platform

Future Work

- Trace interface and encoder support
- JTAG VIP
- Flow management GUI

Questions

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