VirtualATE: SystemC support for Automatic Test Equipment

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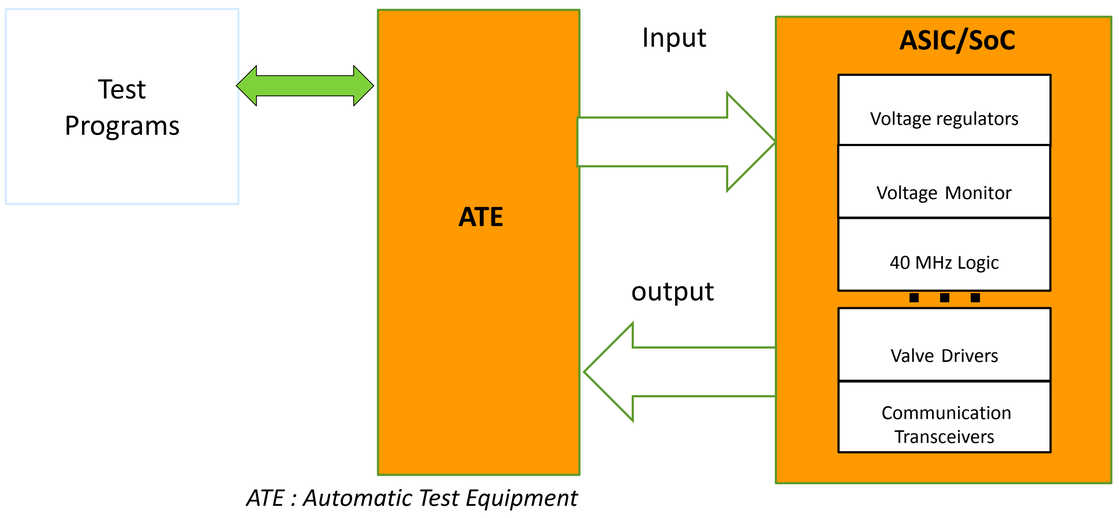
INTRODUCTION

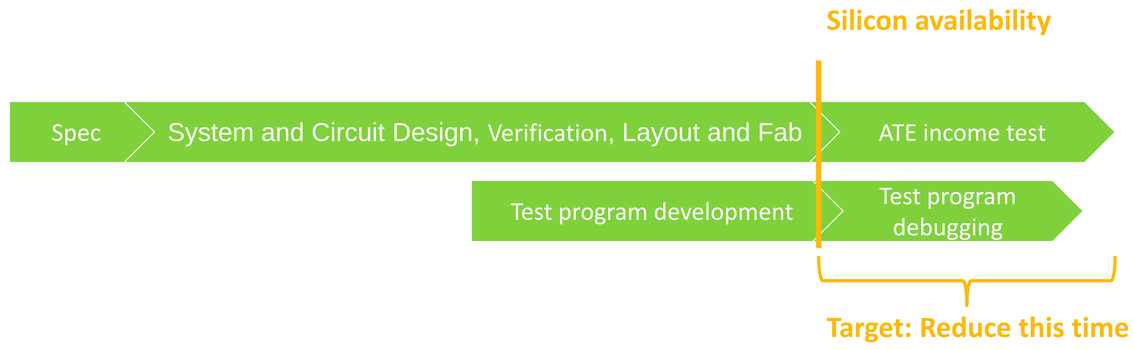
General ATE testing



ATE : Automatic Test Equipment

Bottleneck: Time for test-program development

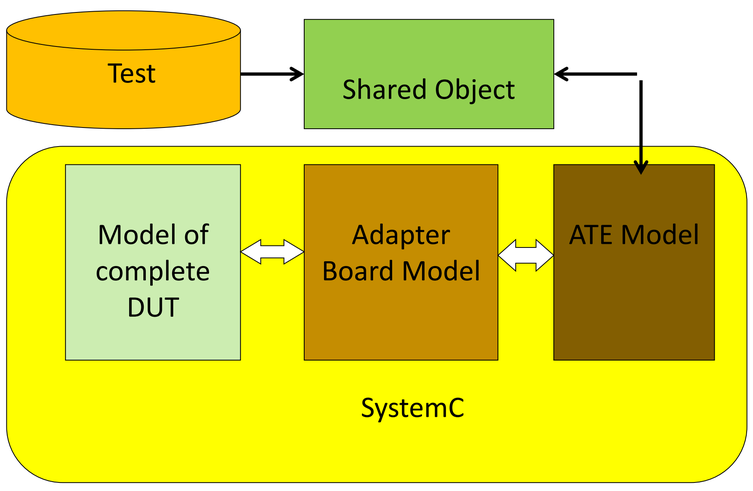
- Can't verify them until DUT silicon is available.



Even after Silicon is available,

- Difficult to debug some aspects without internal register visibility.
- Time Consuming as one can not work in parallel unless one acquires several very expensive ATE systems.

System to be modelled



Implementation of Virtual ATE

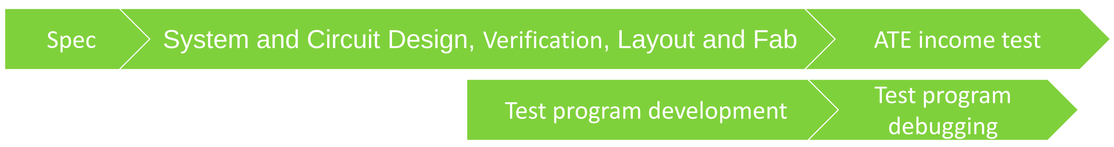
- Test cases compiled into shared object to be loaded at runtime of test system
- Test program interpreter of ATE model written in C++ running in separate thread
- Adapter board and DUT modeled in SystemC
- Time synchronization for communication from ATE model to adapter board by TLM payload event queue
- ATE model supplies the inputs to the DUT and collects the outputs from the DUT
- Outputs are compared against a golden reference file to verify the test cases
- The result file is generated in the same format as on the real ATE system

RESULTS

Typical test case issues dectected with Virtual ATE

- Wrong address used in SPI transfer
- Wrong range expected for result
- Result stored in wrong location
- Saturation of ADC not handled correctly
- Endless loops due to not changing condition
- Mixing voltages and currents
- Missing initialization
- Wrong ADC range

Conventional development



Development with VirtualATE

CONCLUSIONS

- SystemC can be used to front load the development of ATE test programs for mixed-signal ICs.
- Ability to develop complete test suites for the ATE system before silicon availability.
- Saves development time of 3 to 6 month.
- VirtualATE allows more efficient debugging of the test-cases by parallelizing work and the possibility to trace all relevant signals of the DUT.

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