2022 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

MUNICH, GERMANY
DECEMBER 6 - 7, 2022

Verification of High-Speed Links through IBIS-AMI Models

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MathWorks®

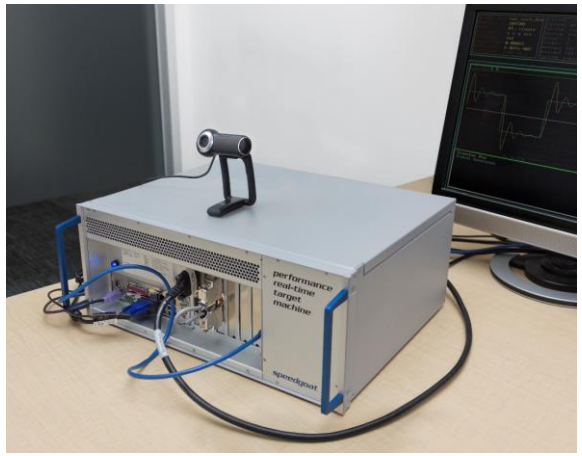
accellera SYSTEMS INITIATIVE

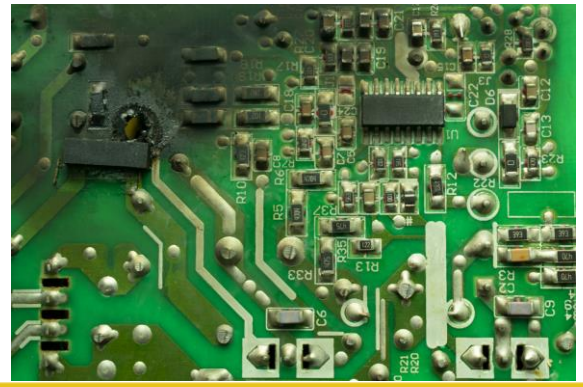
Outline

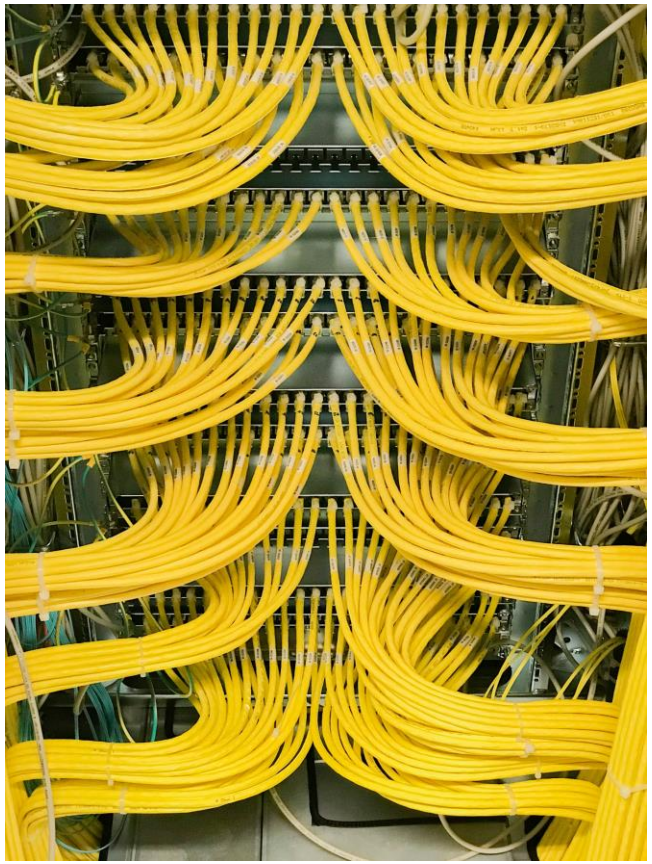
- Introduction to high-speed links
- System-Level modeling workflow
- Performance verification
  - Statistical Domain
  - Time-Domain
- Generation of IBIS-AMI
- Regression checks
- Channel Pre-layout and Post-layout
- Compliance Checking
- Summary

Introduction to High-Speed Links

- High speed digital links or wired links are ubiquitous
- Wide variation of speed and applications, operating conditions
- Limited ports requiring multiplexing at high-speeds
- Growing demand of higher data rate and throughput

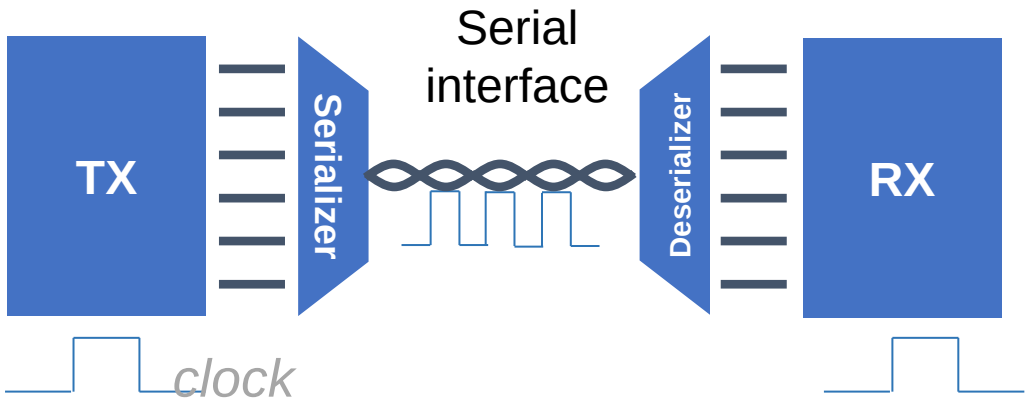


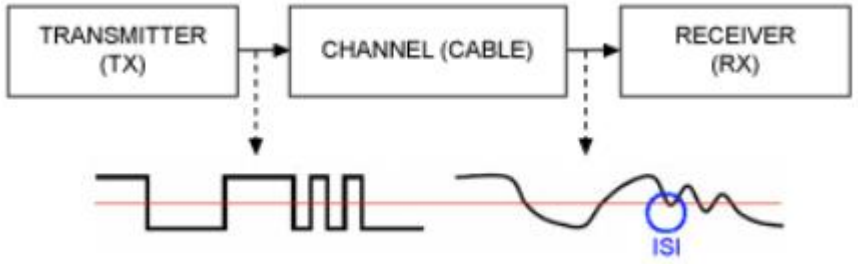




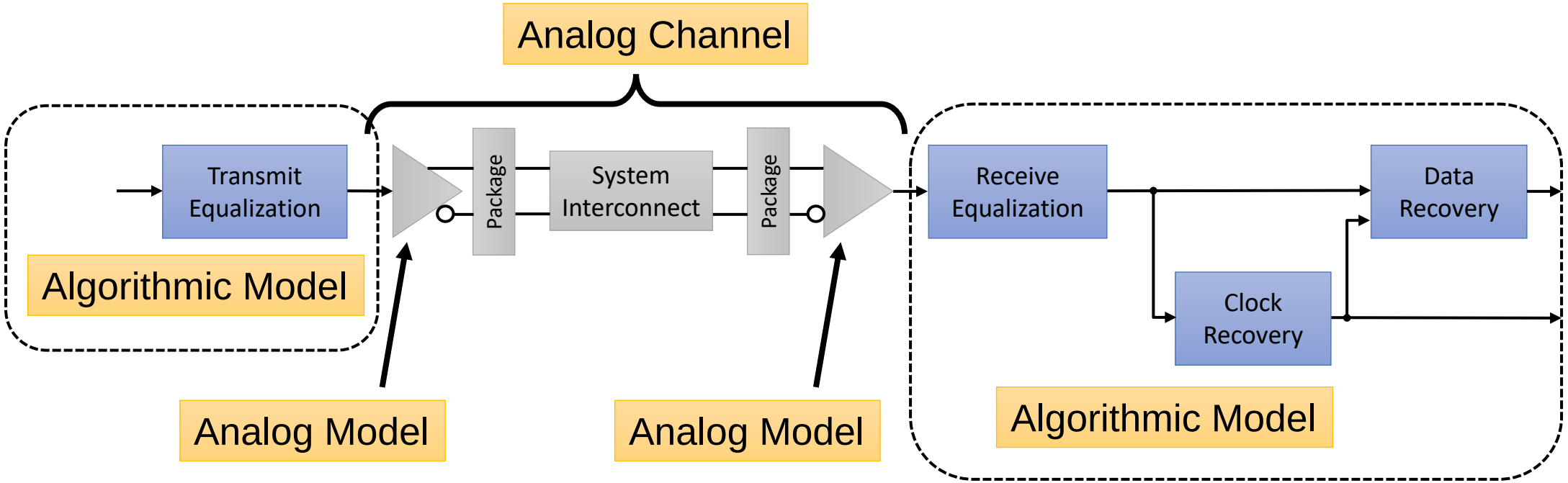
SerDes

- Serializer Deserializer
  - Send Data and Clock
  - Constant increase in speed (~100Gbps)
  - Special case of Mixed-Signal (DSP+RF)
  - Evaluating Equalization techniques
- Example
  - Ethernet
  - Universal Serial BUS
  - DDR (with CDR)
  - PCI



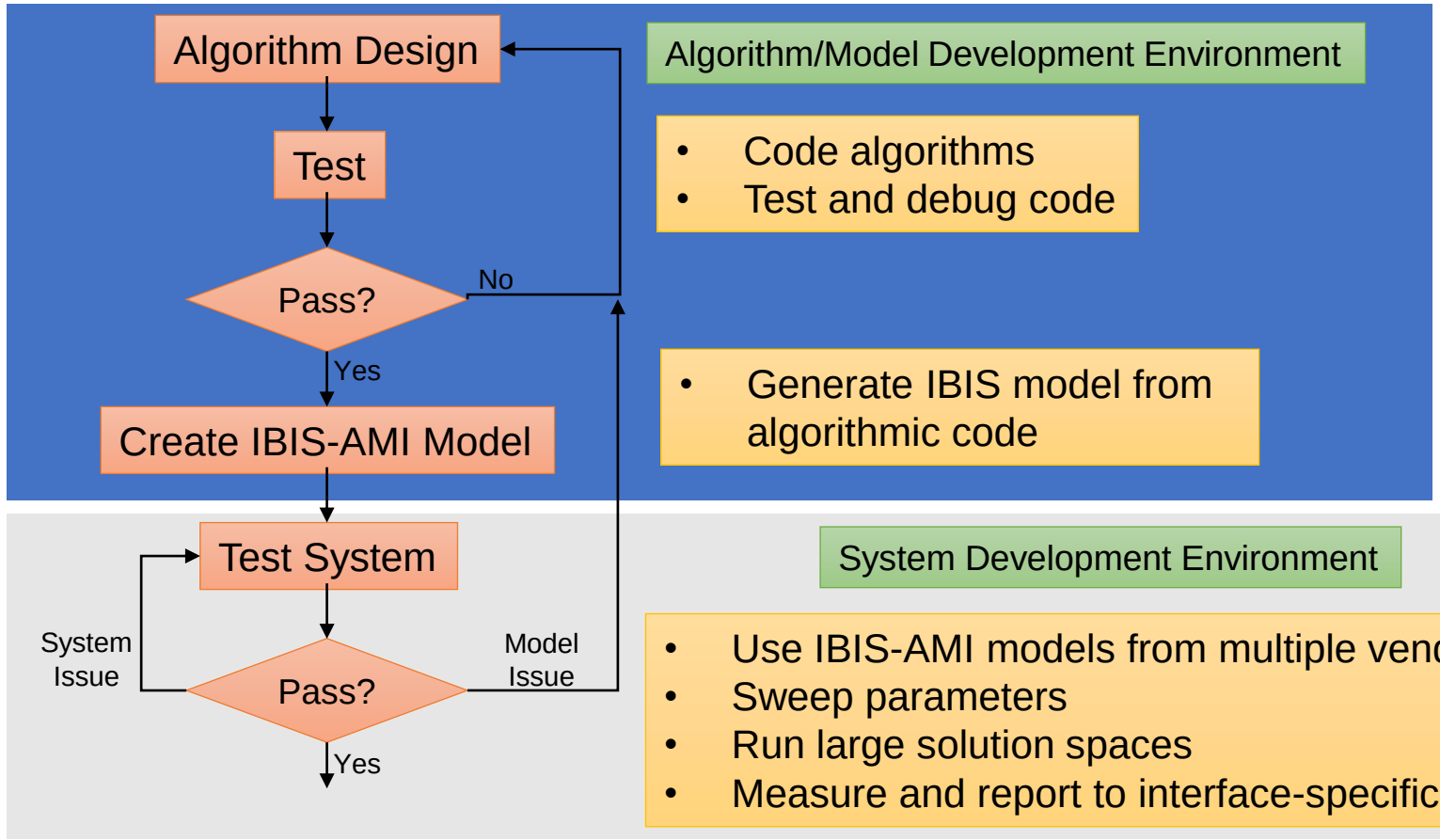


Typical SerDes system: TX, RX and channel



Typical workflow

- Needs multiple expertise
- Iterative and long verification
- Hard to model analog effects



Algorithm/Model Development Environment

- Code algorithms
- Test and debug code

- Generate IBIS model from algorithmic code

System Development Environment

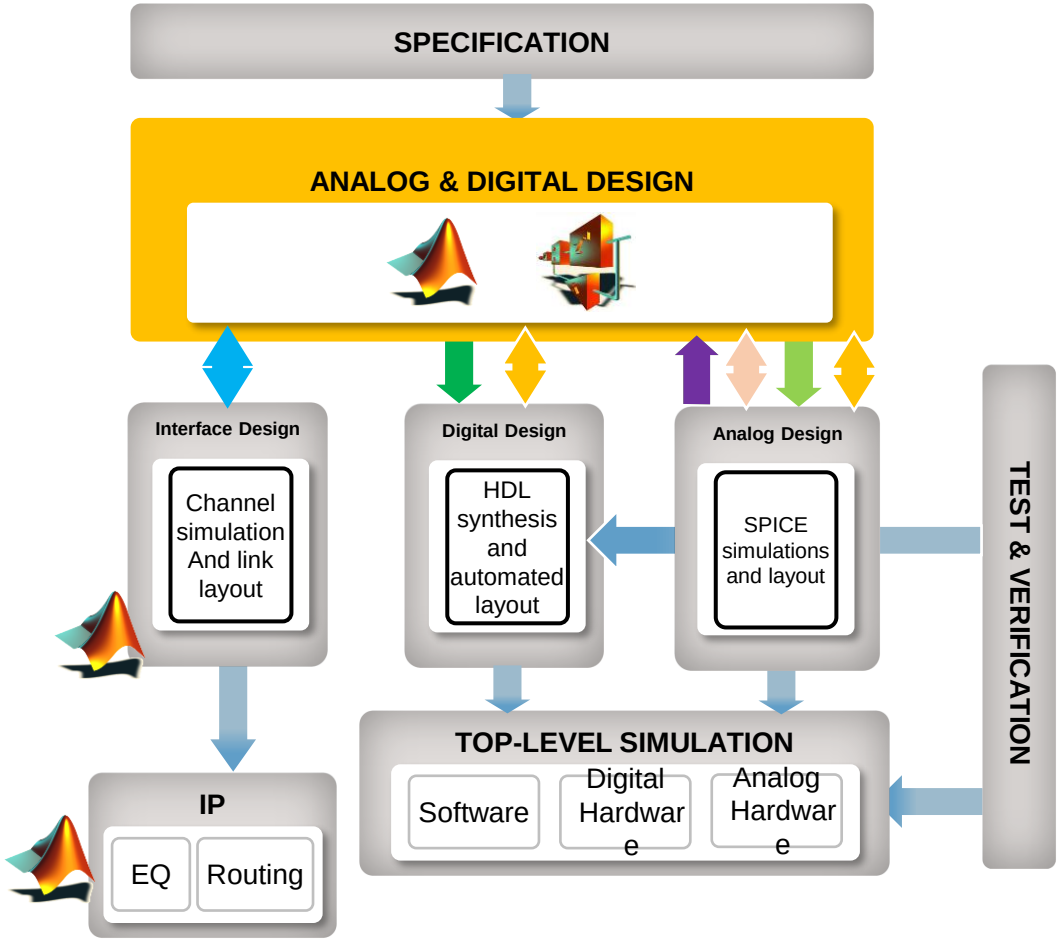
- Use IBIS-AMI models from multiple vendors
- Sweep parameters
- Run large solution spaces
- Measure and report to interface-specific masks

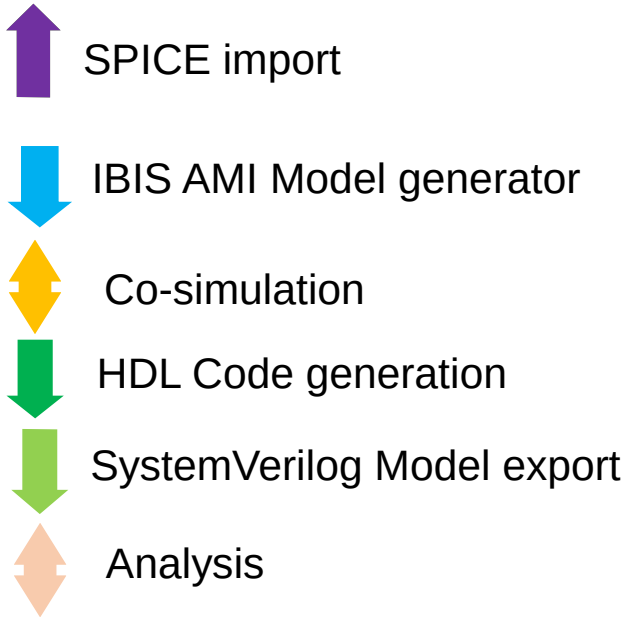
SerDes Architect/
Analog/Mixed Signal Designer

IBIS-AMI Modeler

SI Engineer

Mixed-Signal Design with MATLAB and Simulink



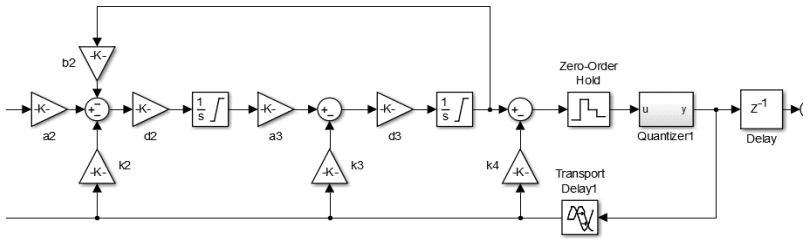


Modeling Approaches

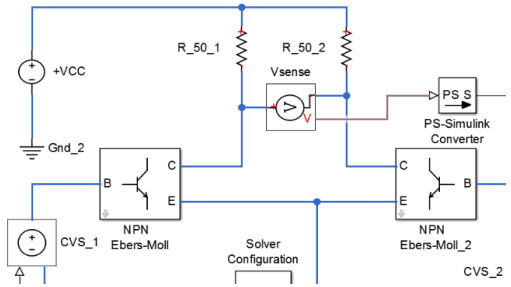
```
%% Hemispherical Conformal Arrays
% You can also model nonplanar arrays. In many applications, sensors must
% conform to the shape of the curved surface they are mounted on. Next is
% an example of an antenna array whose elements are uniformly distributed
% on a hemisphere.
R = 2;                          % Radius (m)
az = -90:10:90;                 % Azimuth angles
el = -80:10:80;                 % Elevation angles (excluding poles)
[az_grid, el_grid] = meshgrid(az,el);
poles = [0 0; -90 90];          % Add south and north poles
nDir = [poles [az_grid(:) el_grid(:)]']; % Element normal directions
N = size(nDir,2);               % Number of elements
[x, y, z] = sph2cart(degtorad(nDir(1,:)), degtorad(nDir(2,:)),R*ones(1,N));
ha = phased.ConformalArray('ElementPosition',[x; y; z],...
                           'ElementNormal',nDir);

viewArray(ha,'Title','Hemispherical Conformal Array');
view(90,0)
```

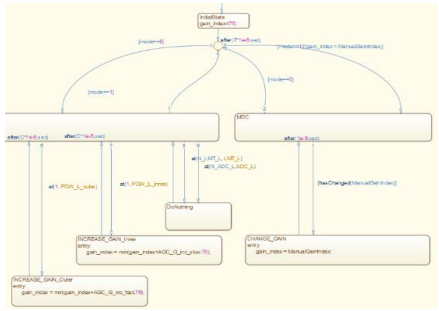
Algorithms



Behavioral Models



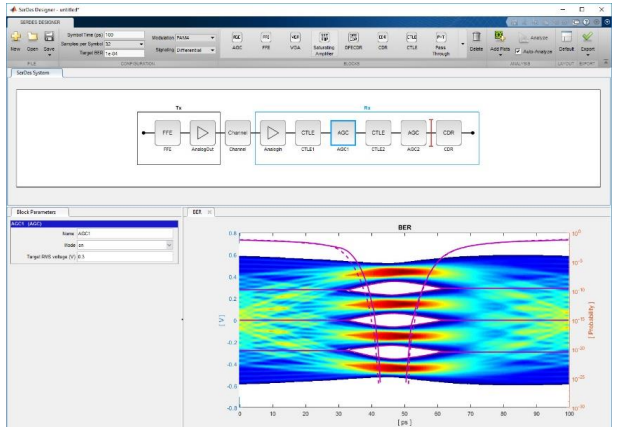
Physical Network

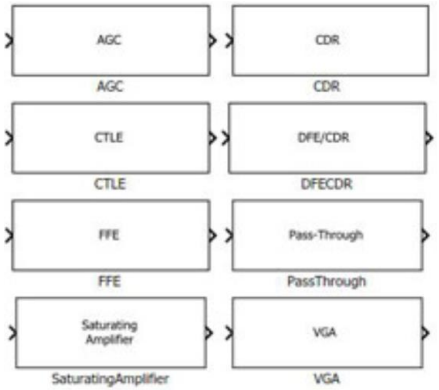


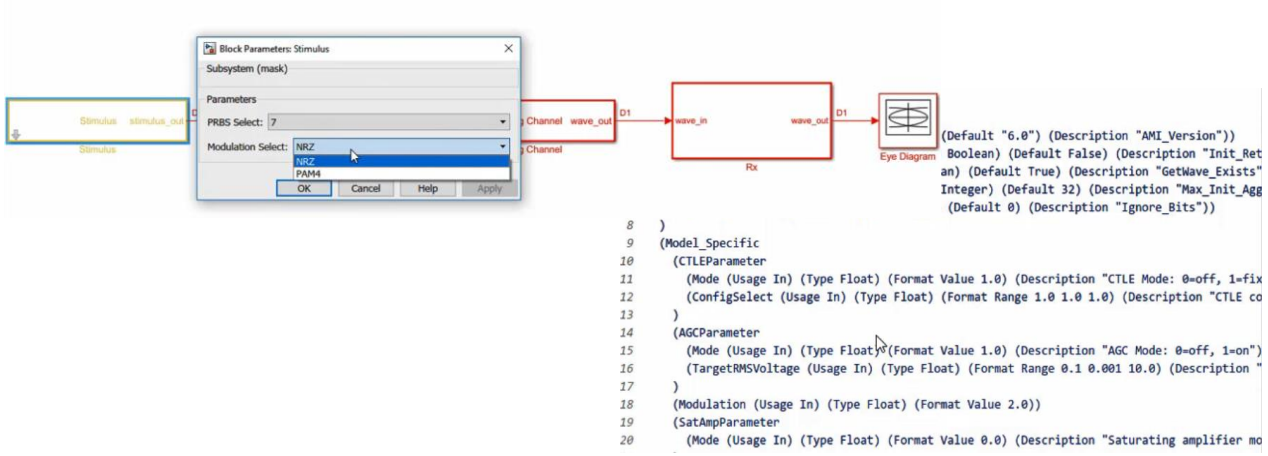
Control Logic

System-level modeling workflow

- Design and analyze transmitters and receivers with the SerDes Designer app
- Develop equalization algorithms with MATLAB System objects and Simulink blocks
  - FFE, DFE, AGC, CDR, CTLE, etc…
- Perform SerDes statistical analysis and time-domain simulation
- Generate **dual IBIS-AMI models** for 3rd party channel simulators
- Use reference designs for high-speed links such as Ethernet CEI-56G, DDR5, PCI-Gen4





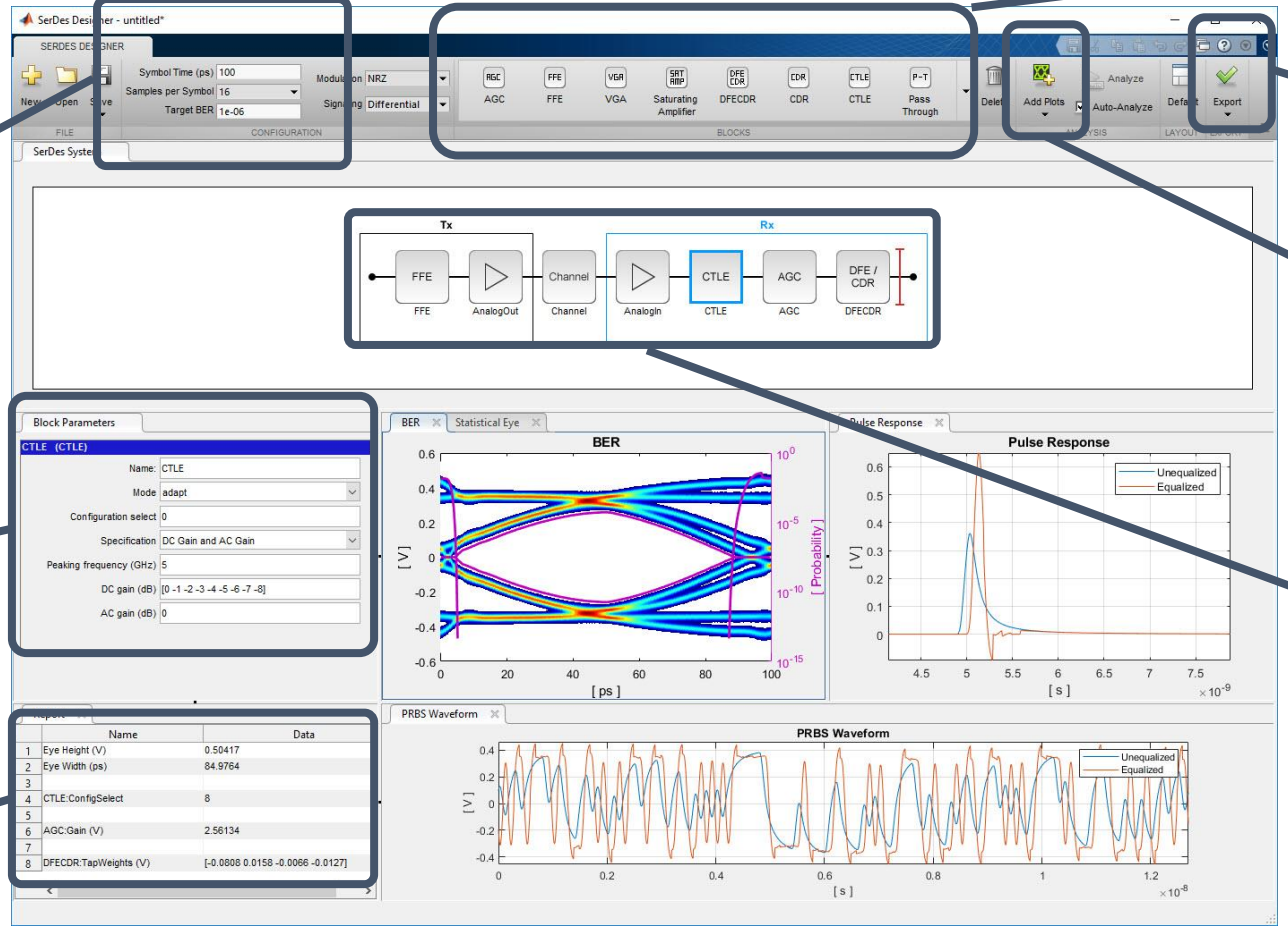


Starting point: SerDes app

Add SerDes components

- Modulation
- Sample rate
- Signalling

Export to:
- MATLAB
- Simulink
- IBIS-AMI



Component specifications

Report

Plot analysis results

High-speed link

SerDes Designer - untitled*

SERDES DESIGNER

New Open Save

FILE

Symbol Time (ps) 100
Samples per Symbol 16
Target BER 1e-06
Modulation NRZ
Signaling Differential

CONFIGURATION

AGC FFE VGA Saturating Amplifier DFECDR CDR

Delete

Add Plots Analyze Auto-Analyze

ANALYSIS

Default

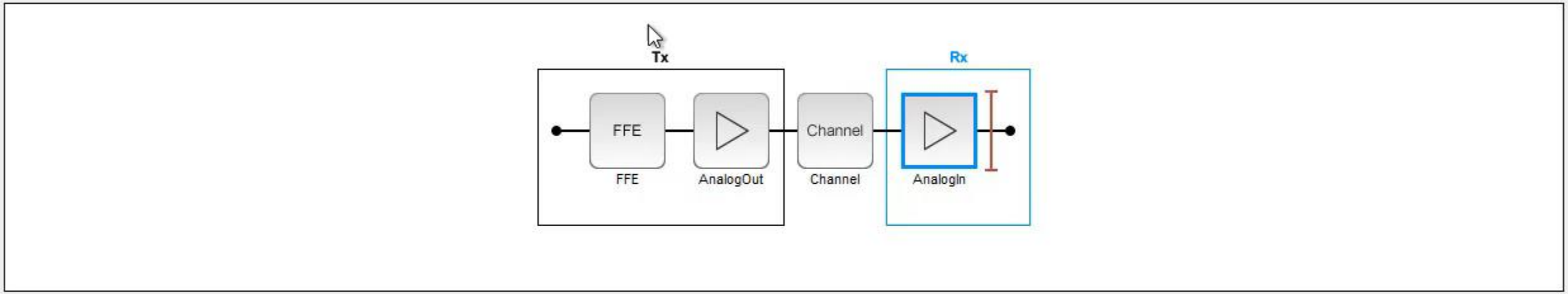
LAYOUT

Export

EXPORT

BLOCKS

SerDes System



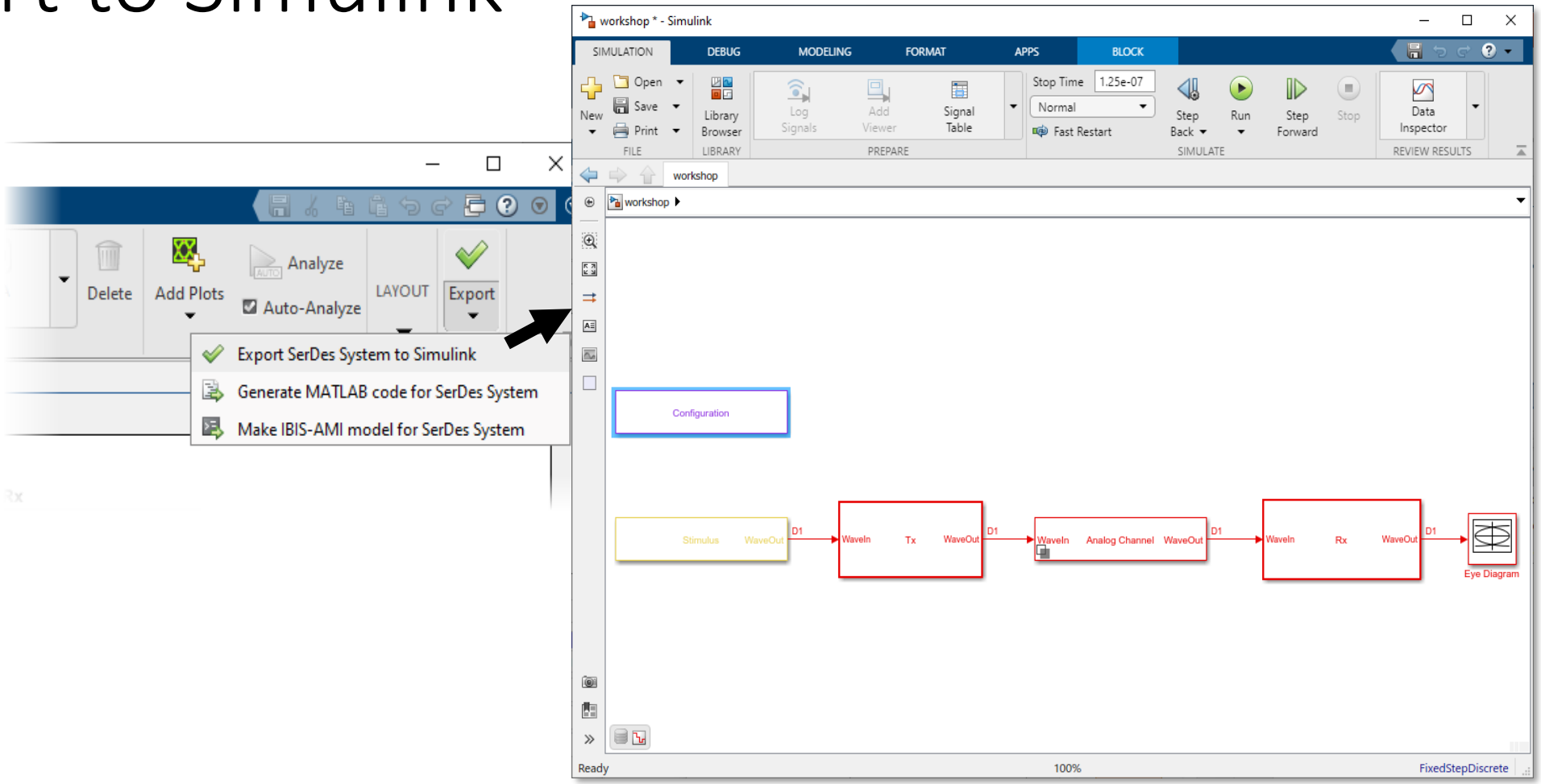
Block Parameters

AnalogIn

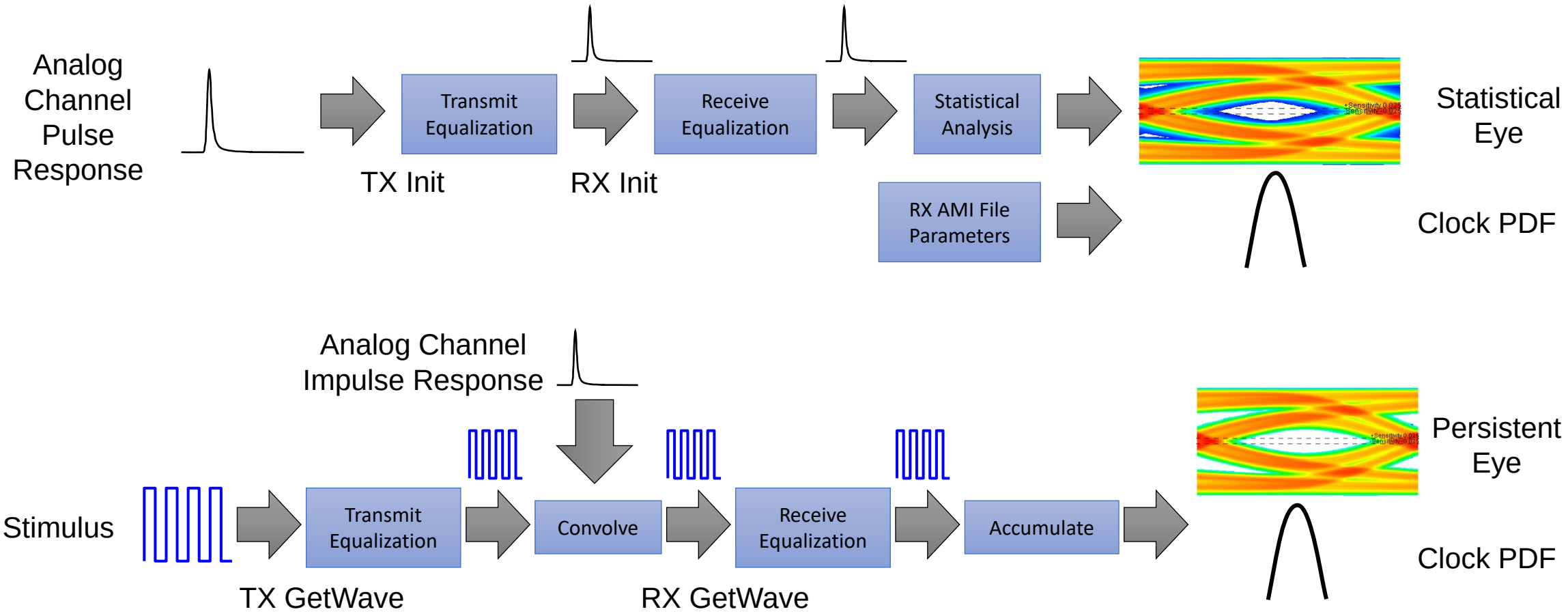
R (Ohms) 50
C (pF) 0.2

Plots

Export to Simulink

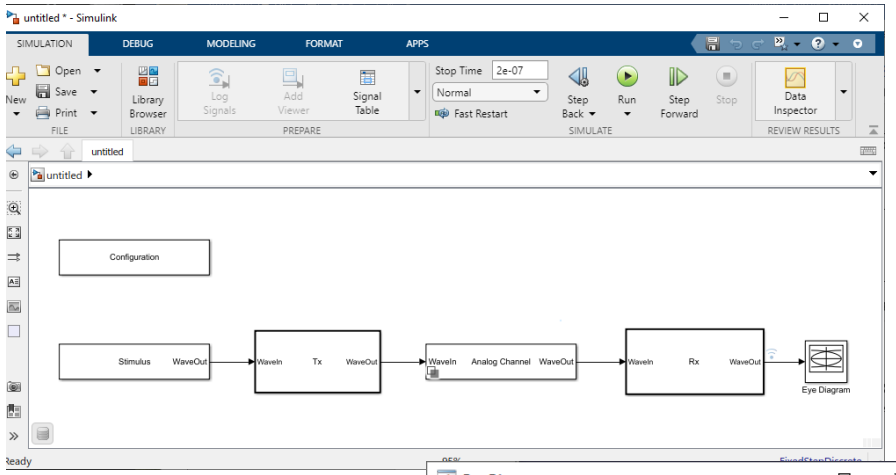


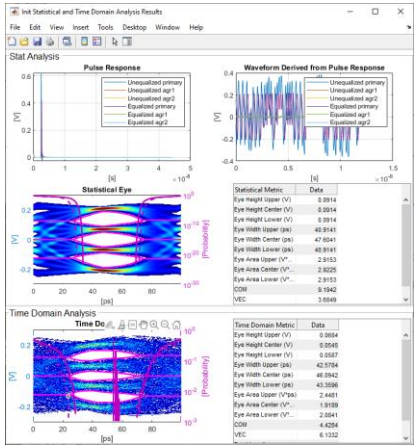
Statistical vs. Time Domain

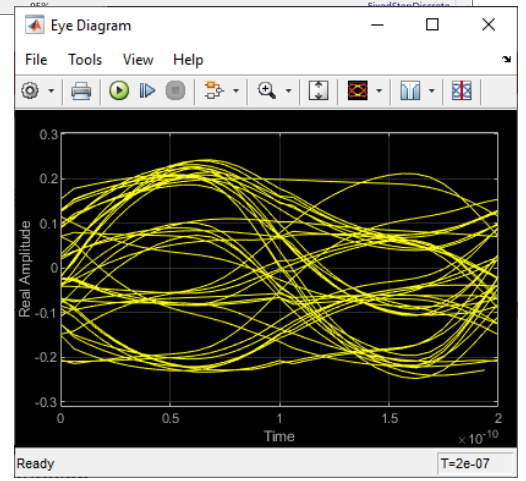


Performance verification

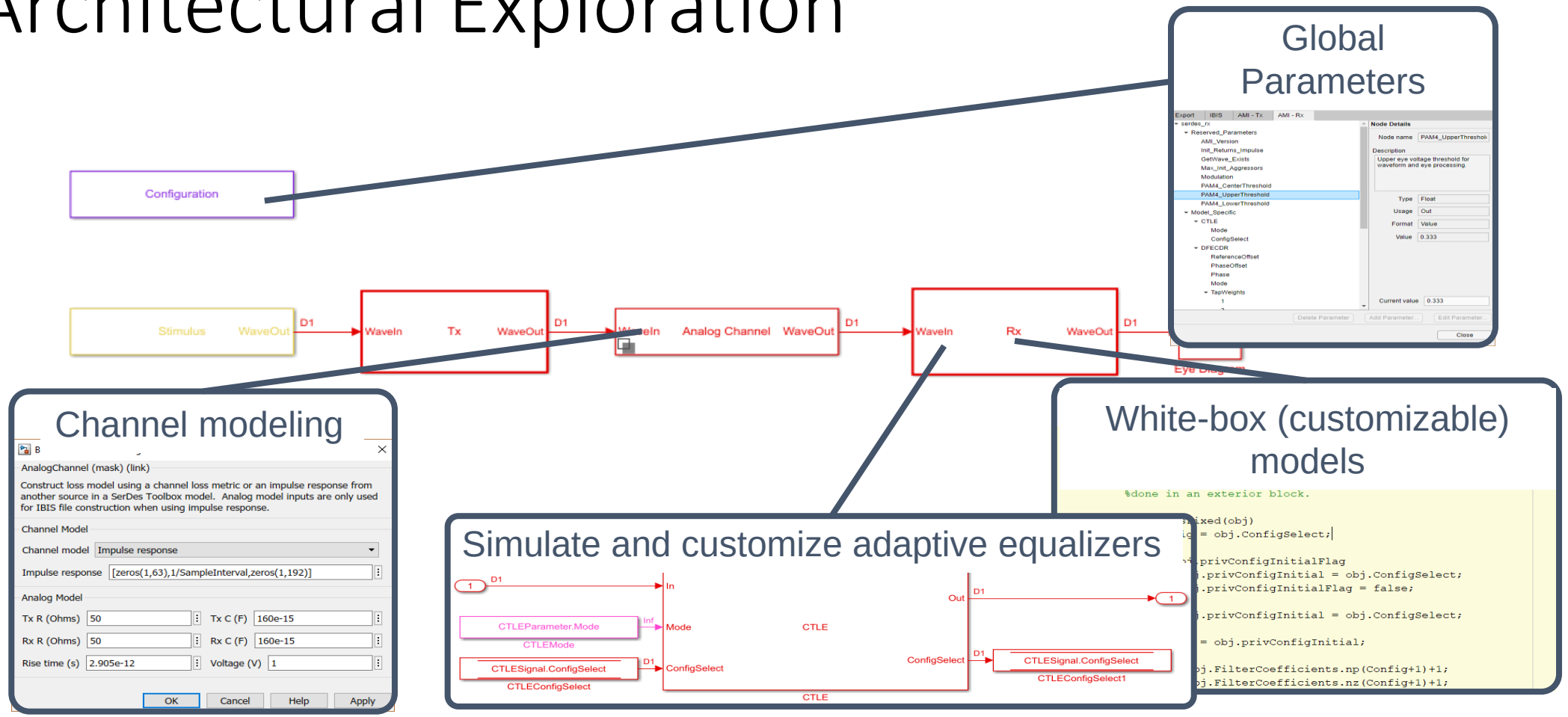
- Export to Simulink models for time-domain simulation
- Model non-linear effects such as saturation
- Customize blocks and equalization algorithms
- Enable global adaptation, and back-channel optimization



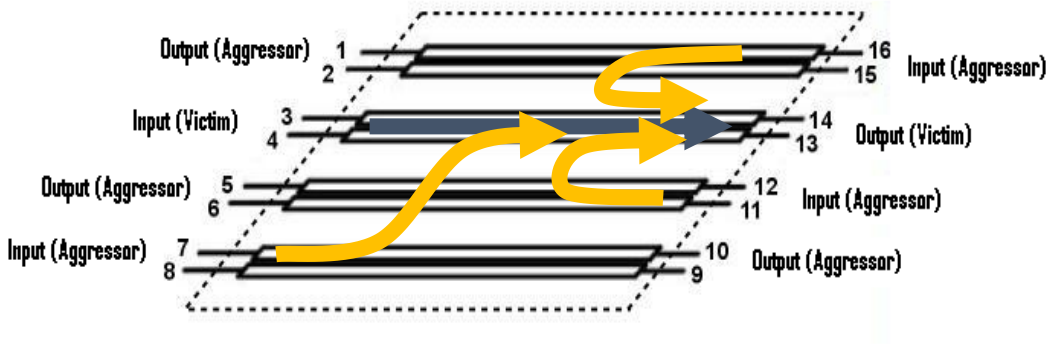




Architectural Exploration



Channel & CTLE Modeling



- Manipulate frequency data to extract the desired information
  - Convert single ended **S-parameters**, select port-pair configuration
  - Analyze impedance, attenuation, phase delay
- Use rational fitting for time-domain simulation
  - Analyze and enforce passivity
  - Causal by construction
  - No overfitting of noise
- Analyze impulse response, poles and zeros

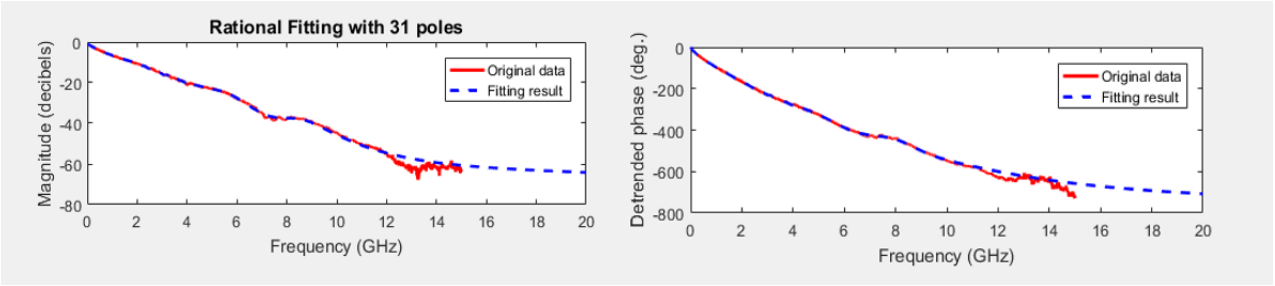
$$f(s) = \left(\sum_{k=1}^{N} \frac{C_k}{s - A_k} + D \right) e^{-st_d}$$

Residues

Time delay

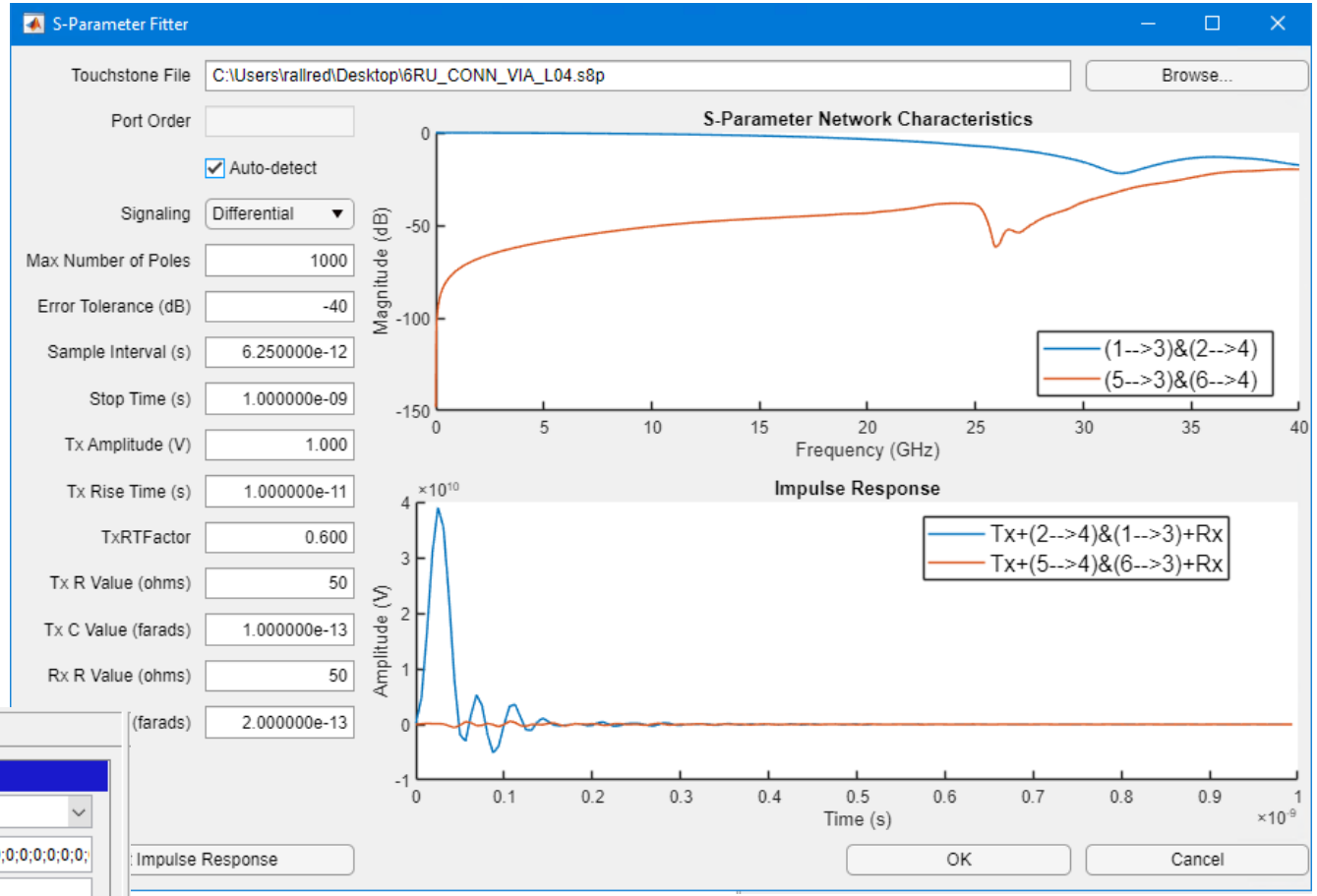
Direct feedthrough
(value at ∞ frequency)

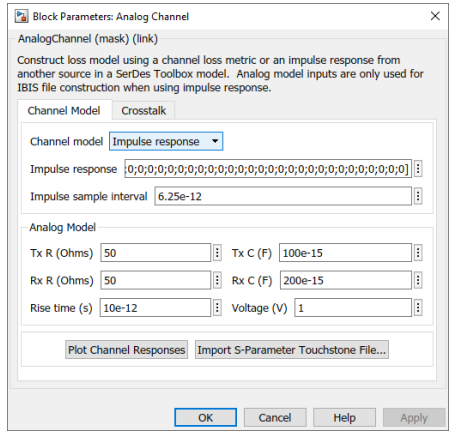
Poles

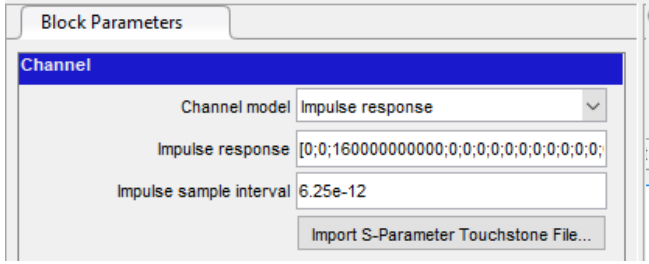


S-Parameter Import

- S-Parameter Fitter App
  - Accessible from SerDes Designer App, Analog Channel block in Simulink, and command line
  - Push button experience customers want!
- S-Parameter Fitter Class enhanced
  - Signal-Ended support (DDR5)
  - Crosstalk support

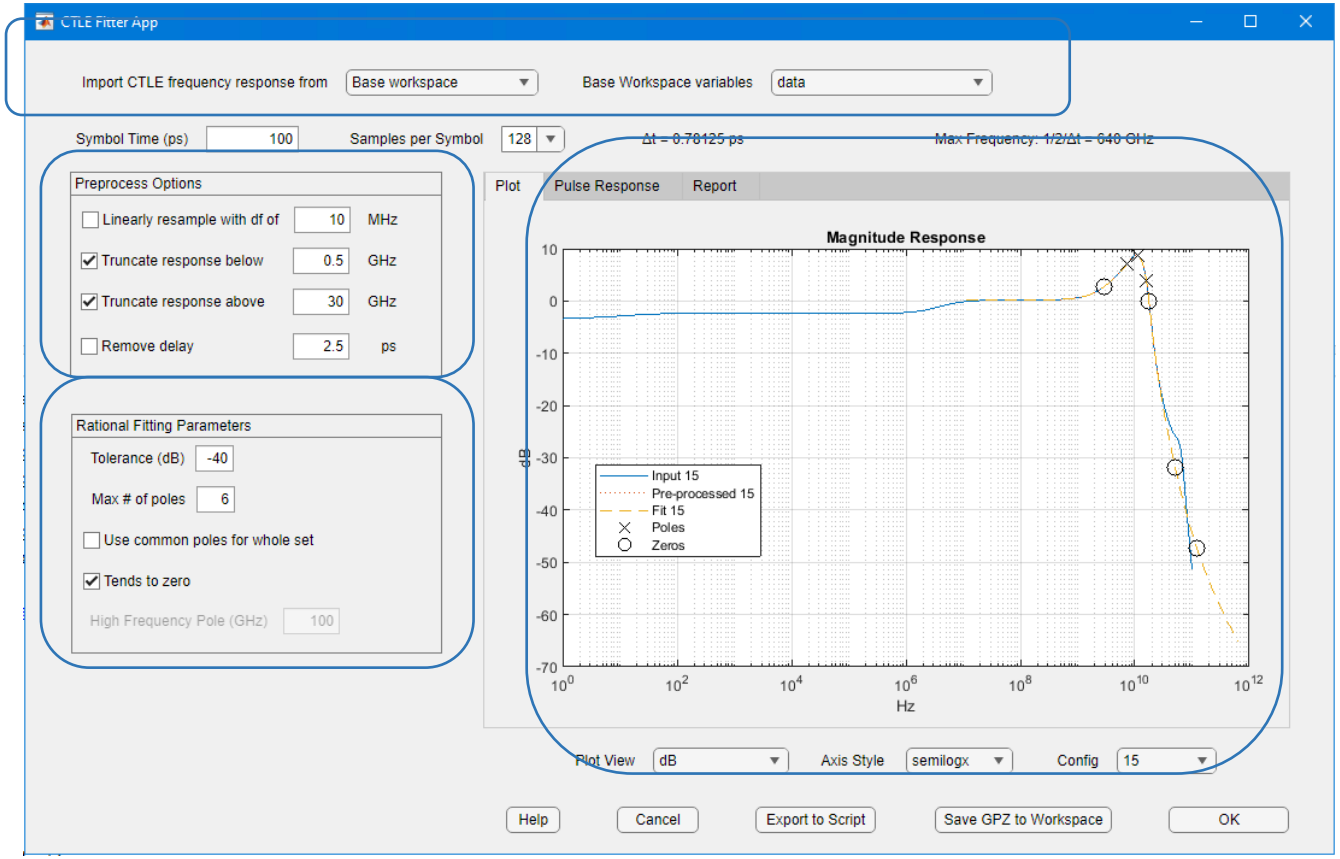




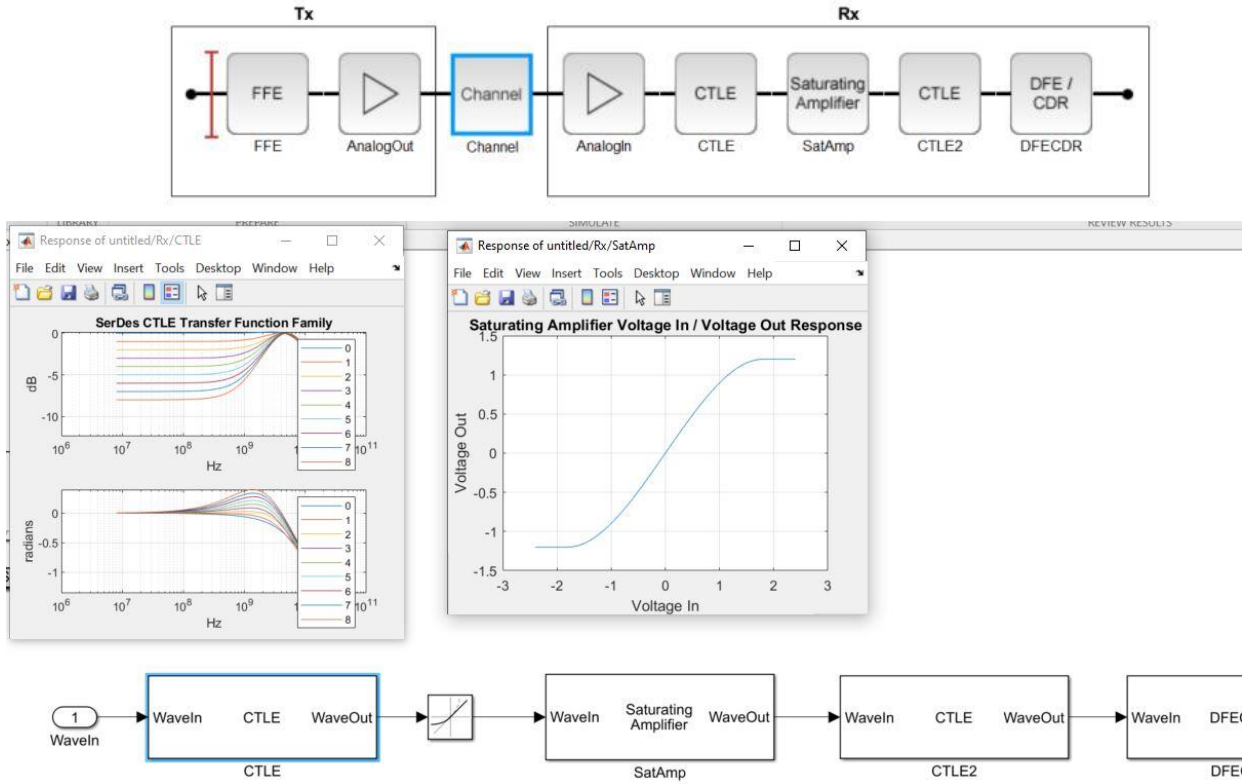


Improved accuracy with bottom-up modeling

- Import Data
- Preprocess Data
- Fit Data
- Visualize Data & Fit
- Integrated with
  - SerDes Designer App
  - CTLE Blocks



Example of inclusion of Non-Linearity



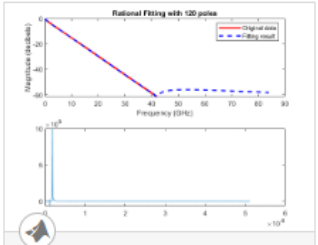
SerDes App

Simulink Export

Rate limiter

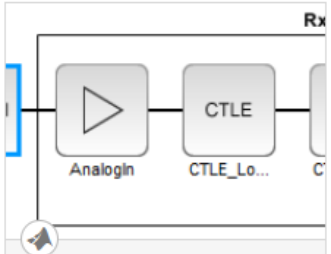
New Examples

- S-Parameter to Impulse Response
- Global Optimization
- Custom Block Workflow – Edit CTLE
- Custom Block Workflow – Use any Simulink block



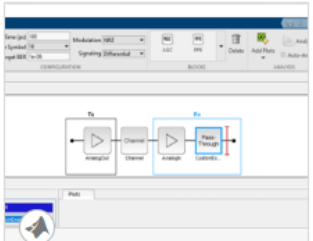
Convert Scattering Parameter to Impulse Response for SerDes...

Covers two topics: the first focuses on the concatenation of three scattering parameters (S-Parameters) that represent a



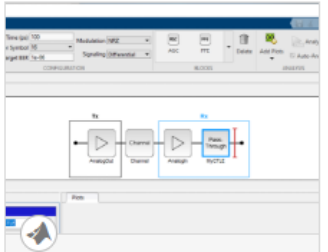
Globally Adapt Receiver Components Using Pulse Response Metrics to...

Perform optimization of a set of receiver components as a system using function optPulseMetric to calculate metrics such as eye



Customizing Datapath Building Blocks

Customize a PassThrough block in Simulink® using other Simulink library blocks. This example shows the implementation of a receiver

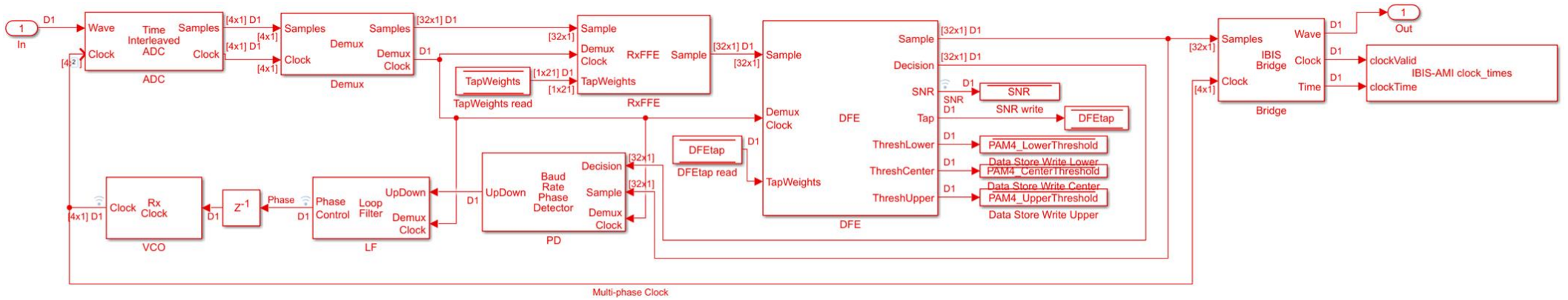


Implement Custom CTLE in SerDes Toolbox PassThrough Block

Customize a PassThrough Block in Simulink® to implement a CTLE System Object™ with user defined AMI parameters. You can use this

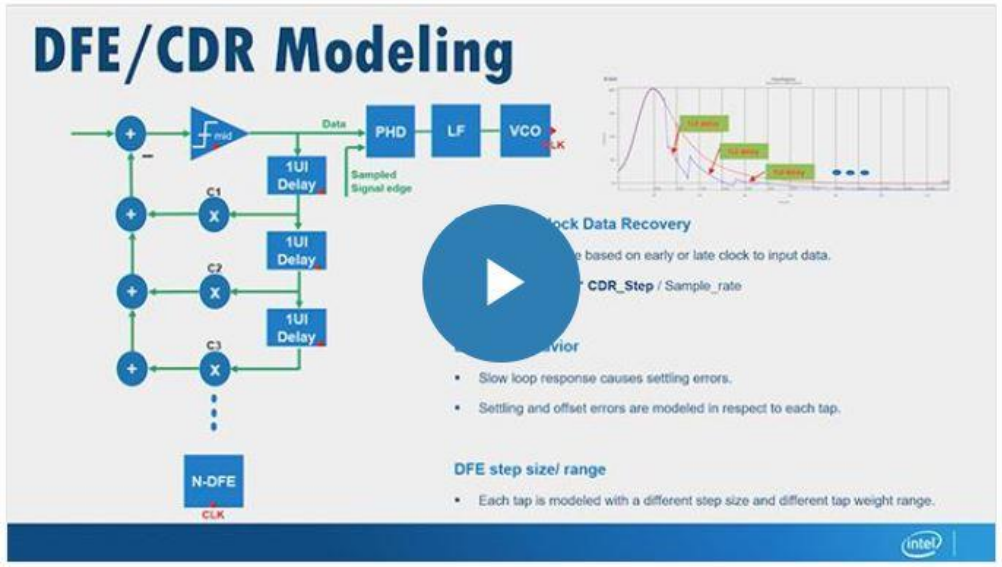
Advanced example for high speeds

- Show how to more precisely **explore the tradeoffs** between:
  - Number of interleaved ADCs
  - Gain, timing, bandwidth and voltage offsets between the interleaved ADCs
  - Demux width
  - DSP adaptation loops



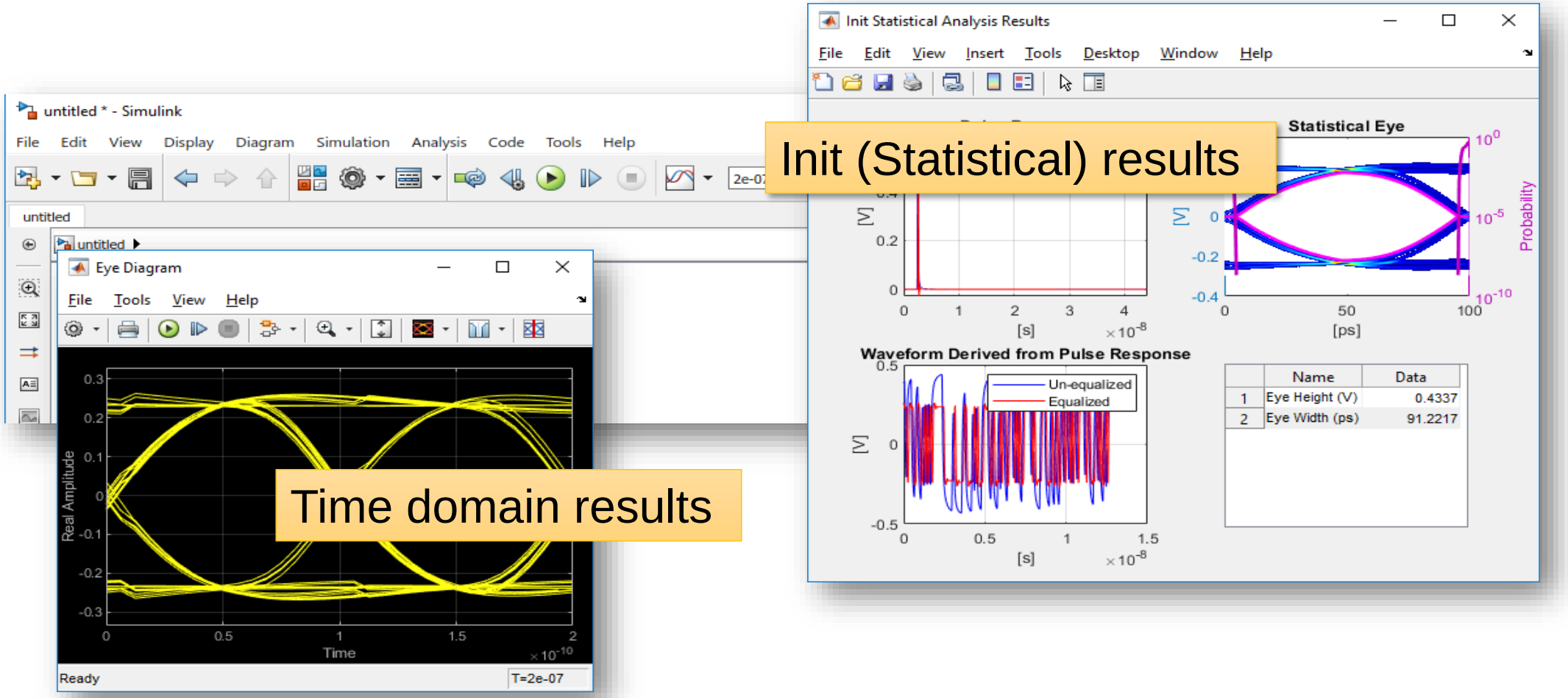
Customer reference: Intel

- 56G PAM4 IBIS-AMI Model



- DesignCon 2020 –
  - DfA (Design for AMI) – A New Integrated Workflow for Modeling 56G PAM4 SerDes Systems

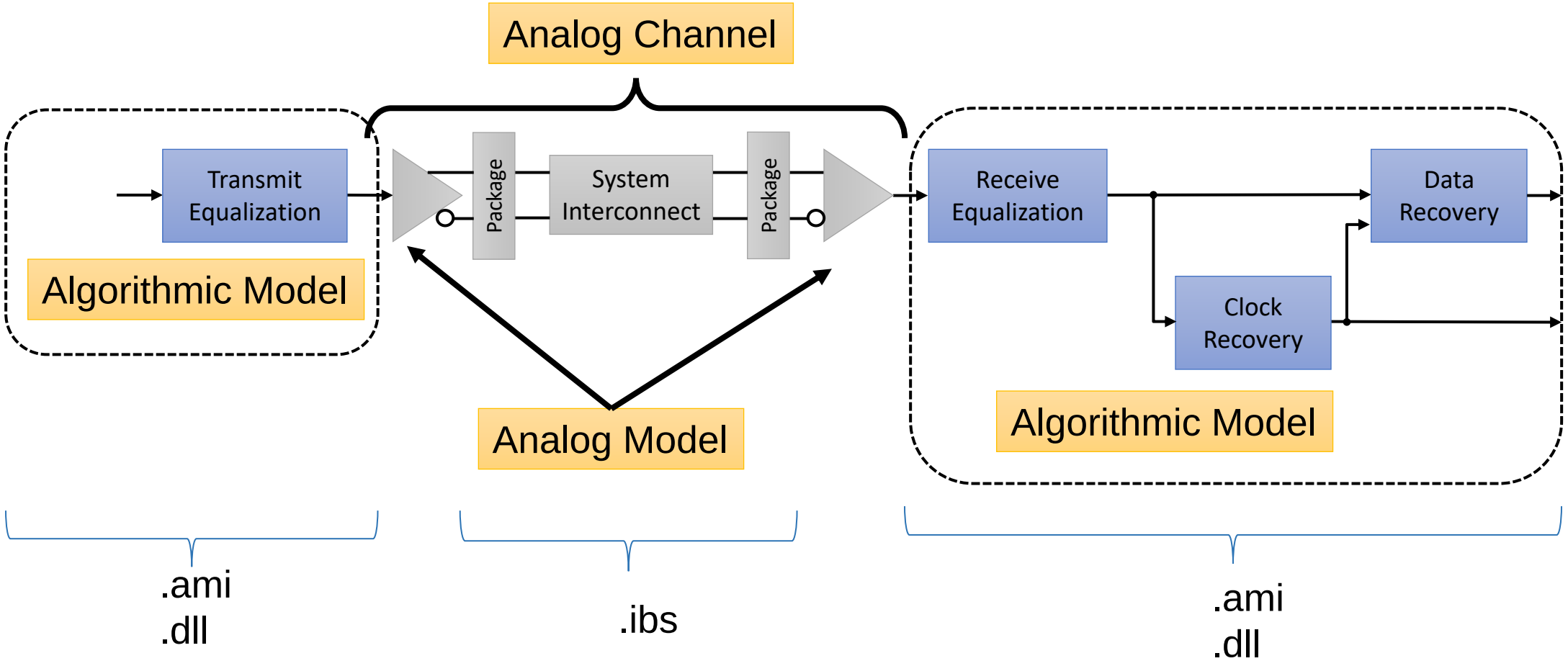
Correlated Simulations



Init (Statistical) results

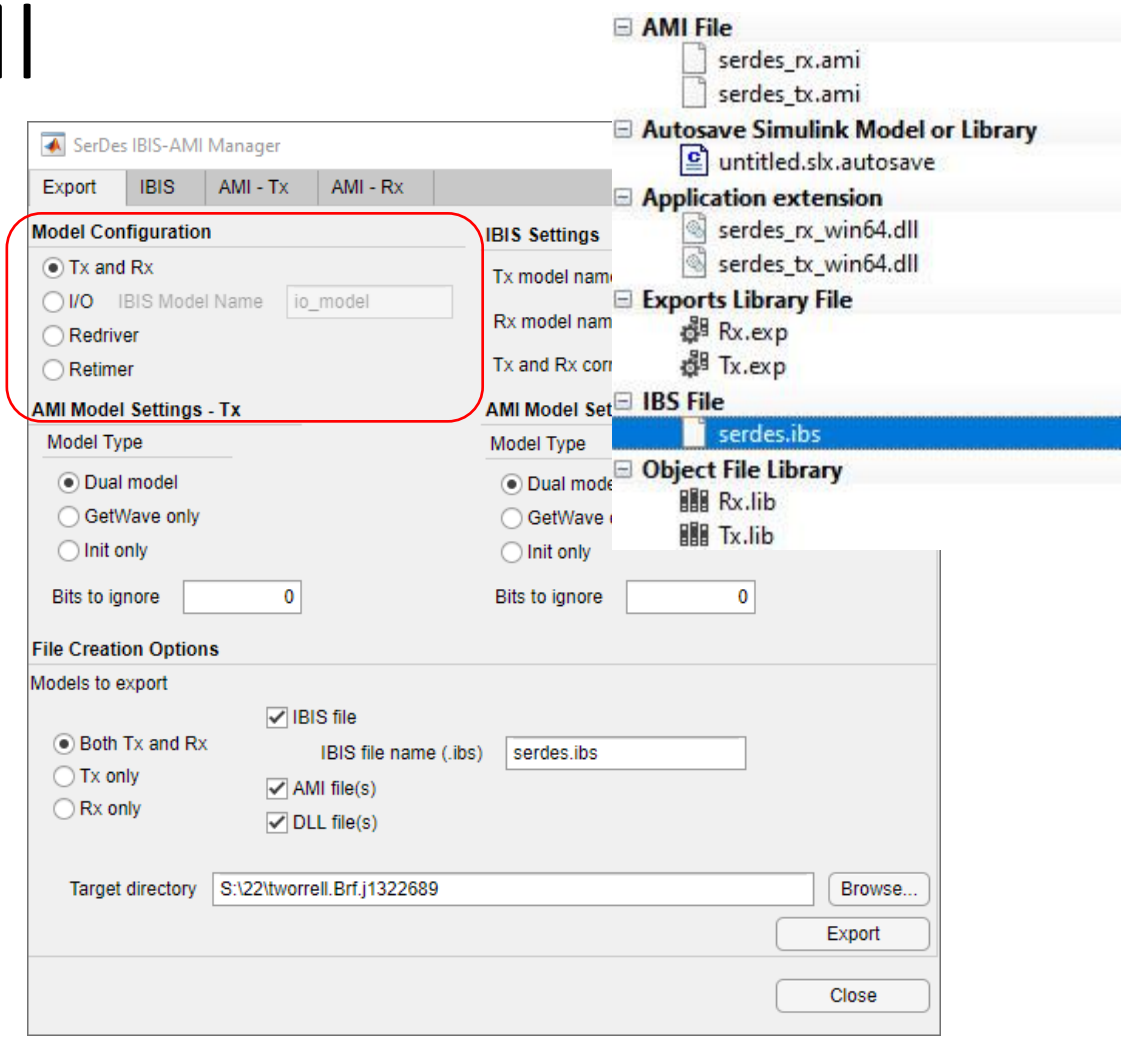
Time domain results

Generation of IBIS-AMI

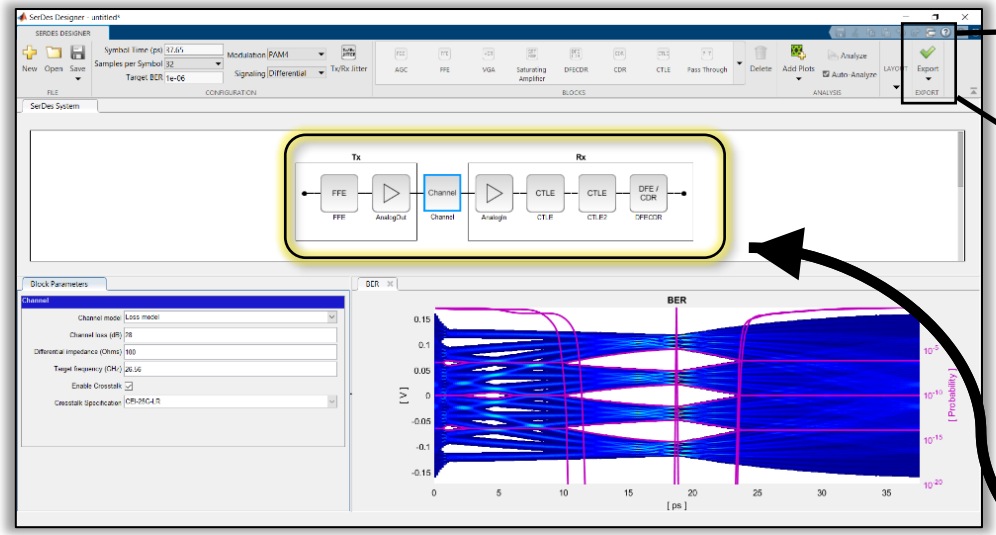


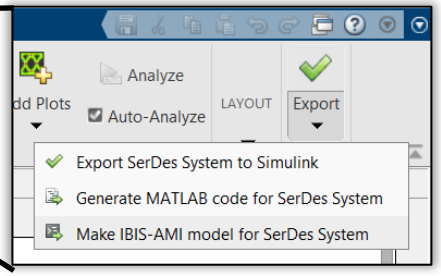
Generation of IBIS-AMI

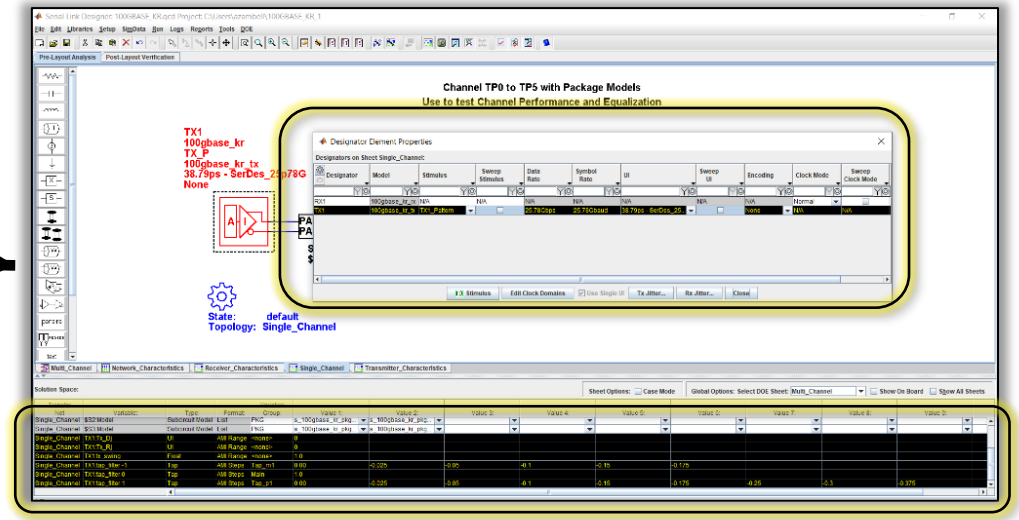
- Generate standard-compliant Init and GetWave IBIS-AMI models
- Generate associated analog IBIS model
- Customize the model interface by managing the IBIS- AMI-parameters
- Retimer & redriver:
  - Connects Rx to Tx per IBIS-AMI spec
- I/O: Bi-directional for DDR applications



Integration for testing



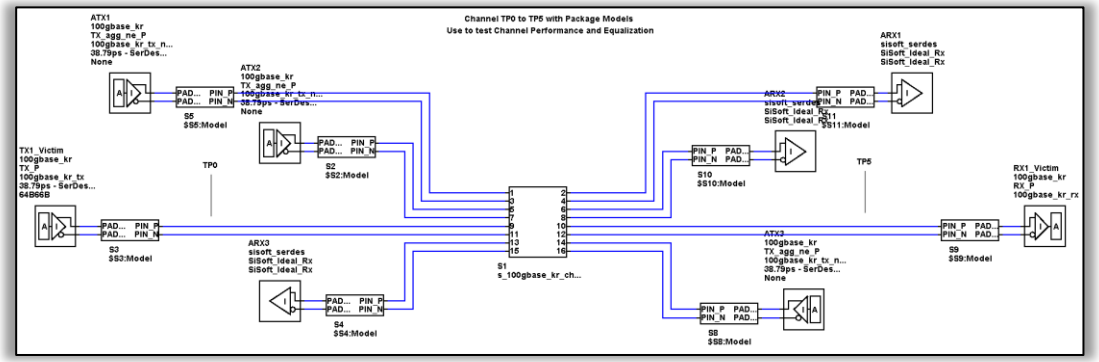


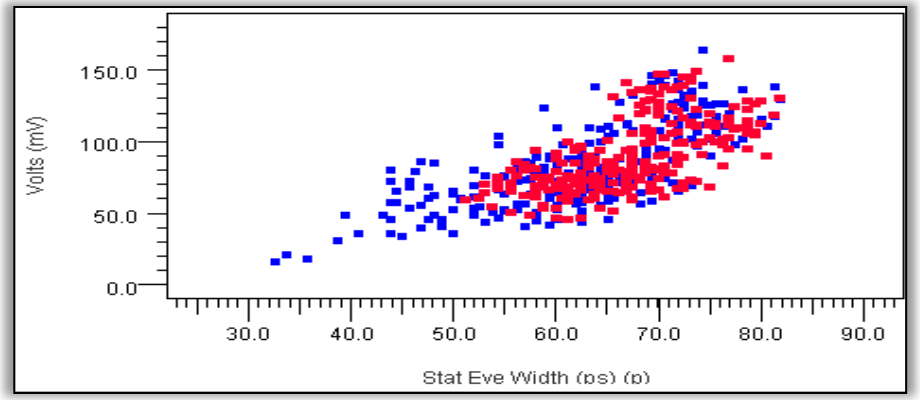


- Build your model in SerDes Toolbox and export an IBIS-AMI model directly into Signal Integrity Toolbox for Regression Analysis
- Sweep your IBIS-AMI model parameters to test them with various channels in Signal Integrity Toolbox
- If there are any issues, the test case can be pushed back to SerDes Toolbox / Simulink where you have full debug capabilities

Verifying the IBIS-AMI model with the channel

- Sweep parameters to explore the to find the best solution
- Build schematics to test the signal integrity of high-speed end-to-end serial and parallel links
- Test components and/or system designs for industry standard compliance
- Perform channel, statistical, and time-domain analyses and visualize the results
- Import PCB files for post-layout verification
- Import IBIS-AMI models for testing

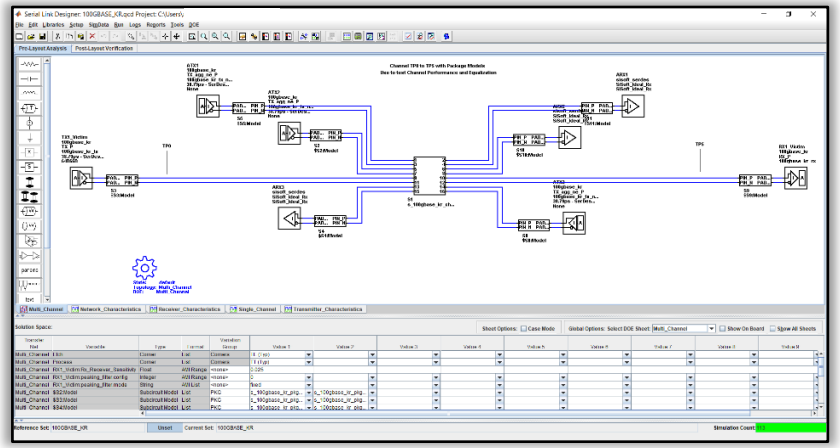




Pre-layout Analysis workflow

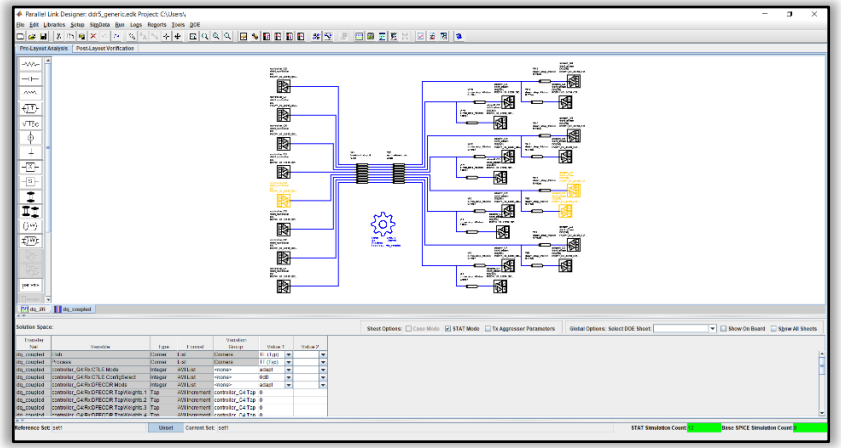
- Serial Link

- Determine optimal equalization settings
- Predict operating margins and bit error rates
- Perform network, statistical, and time-domain analysis



- Parallel Link

- Determine setup/hold timing and voltage margins
- Conduct waveform and timing analysis
- Analyze interfaces for timing and signal integrity compliance

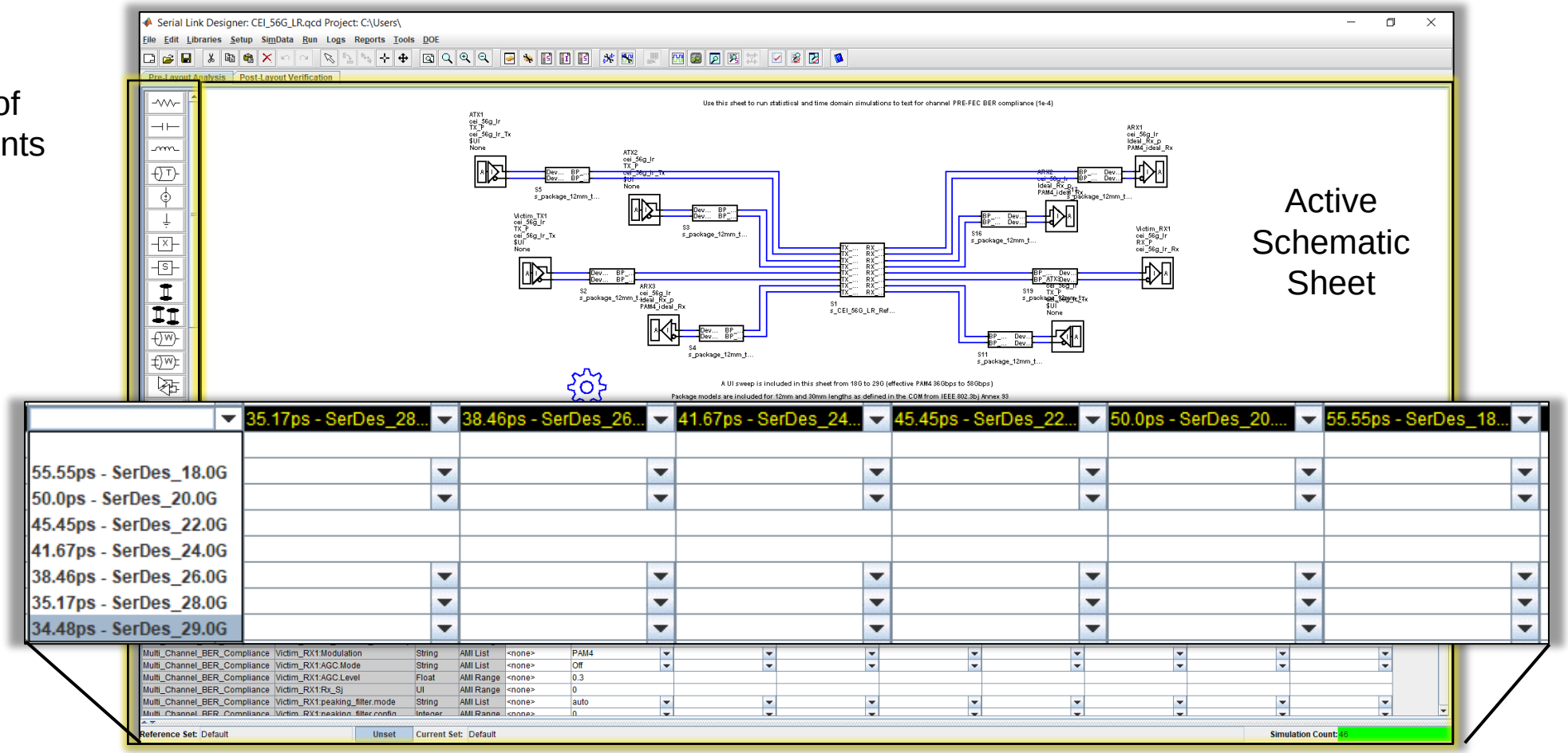


Pre-layout Analysis: solution space

List of Elements

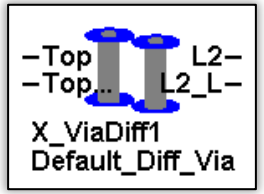
All Schematic Sheets

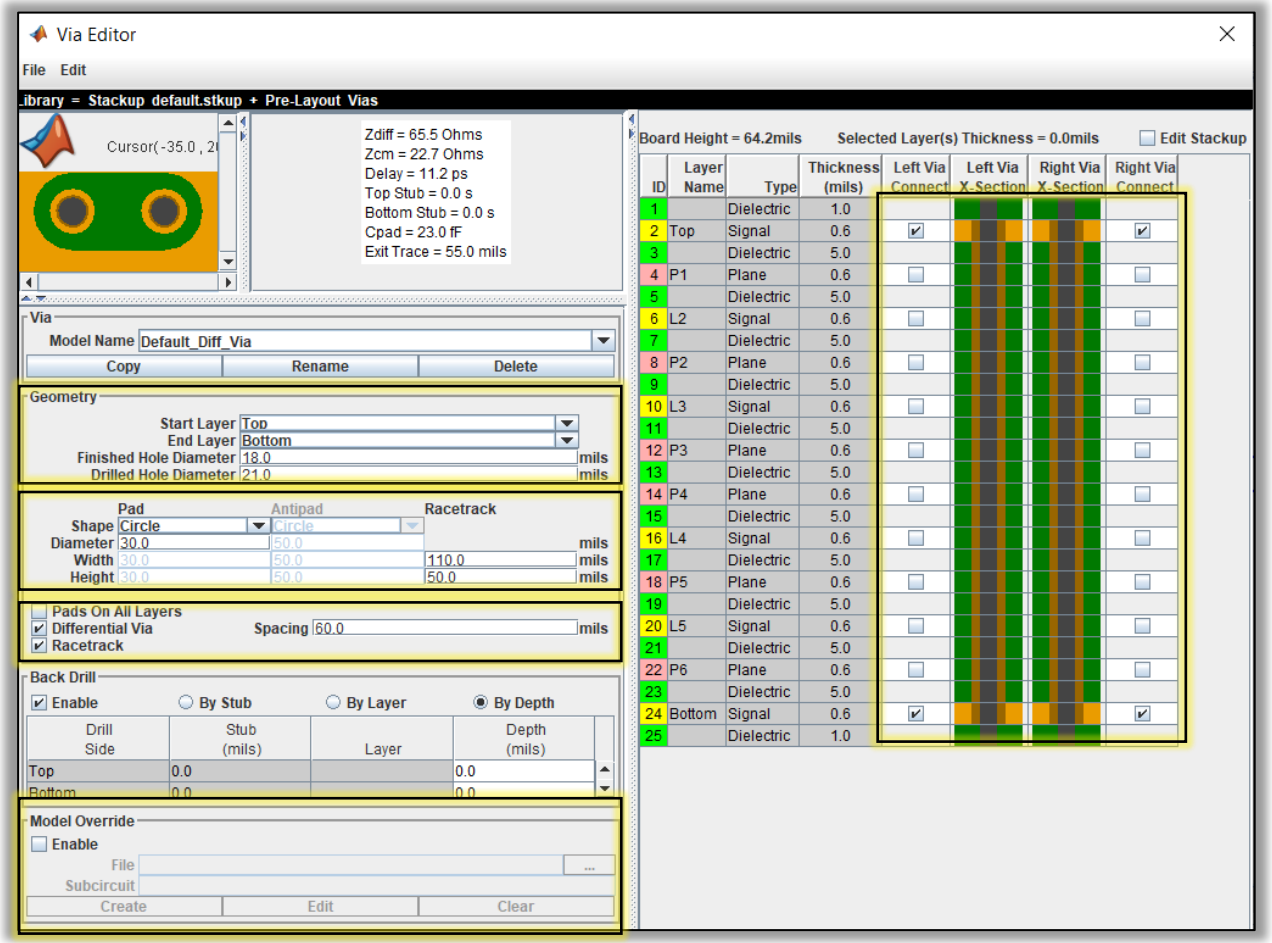
Solution Space



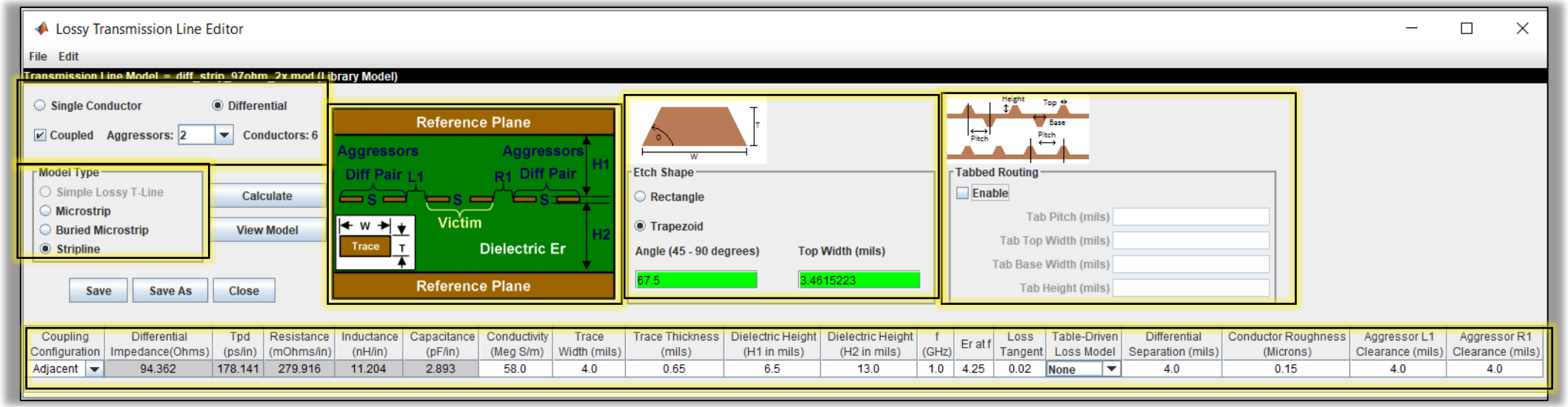
Active Schematic Sheet

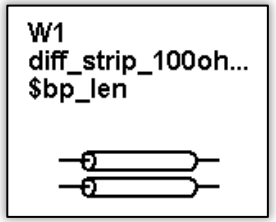
Building schematic: Configure Via



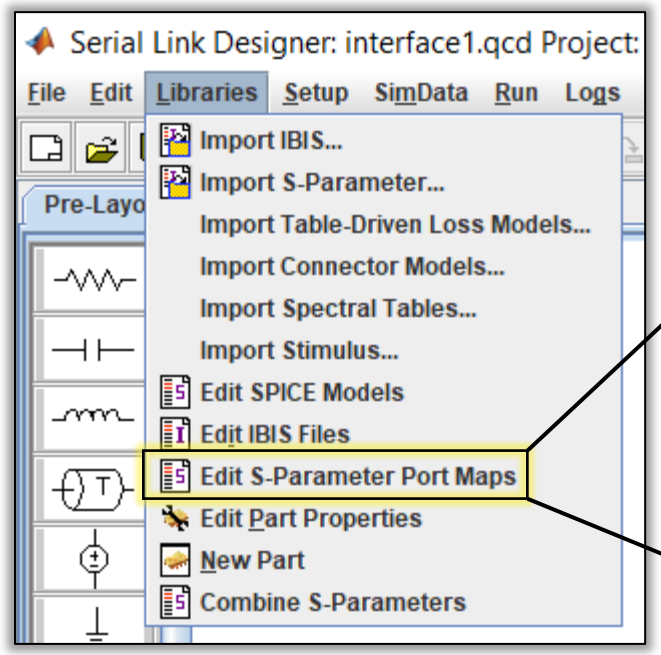


Building schematic: Configure Transmission Line

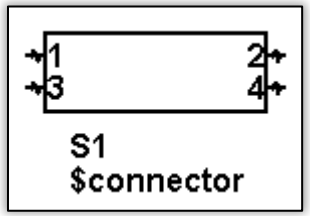


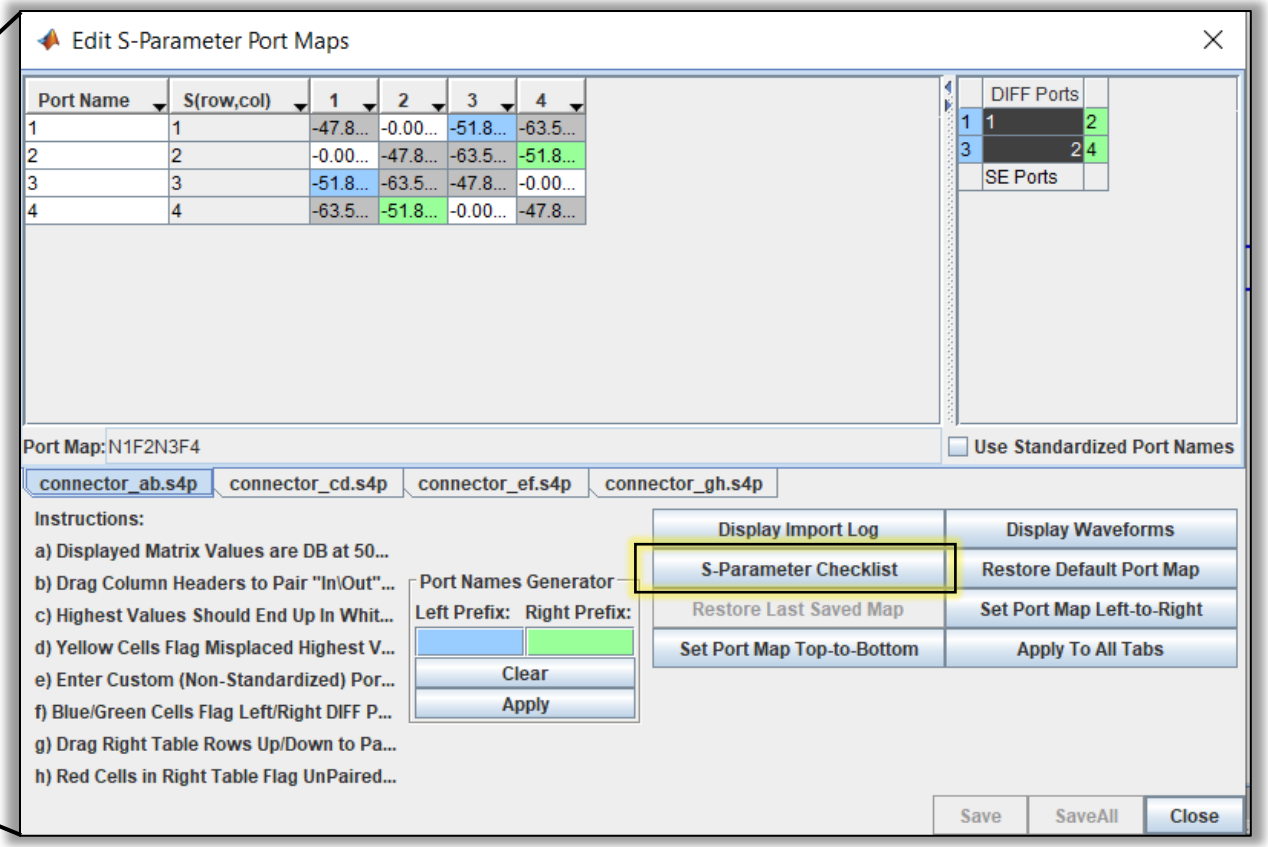


Importing and Edit s-parameter Models



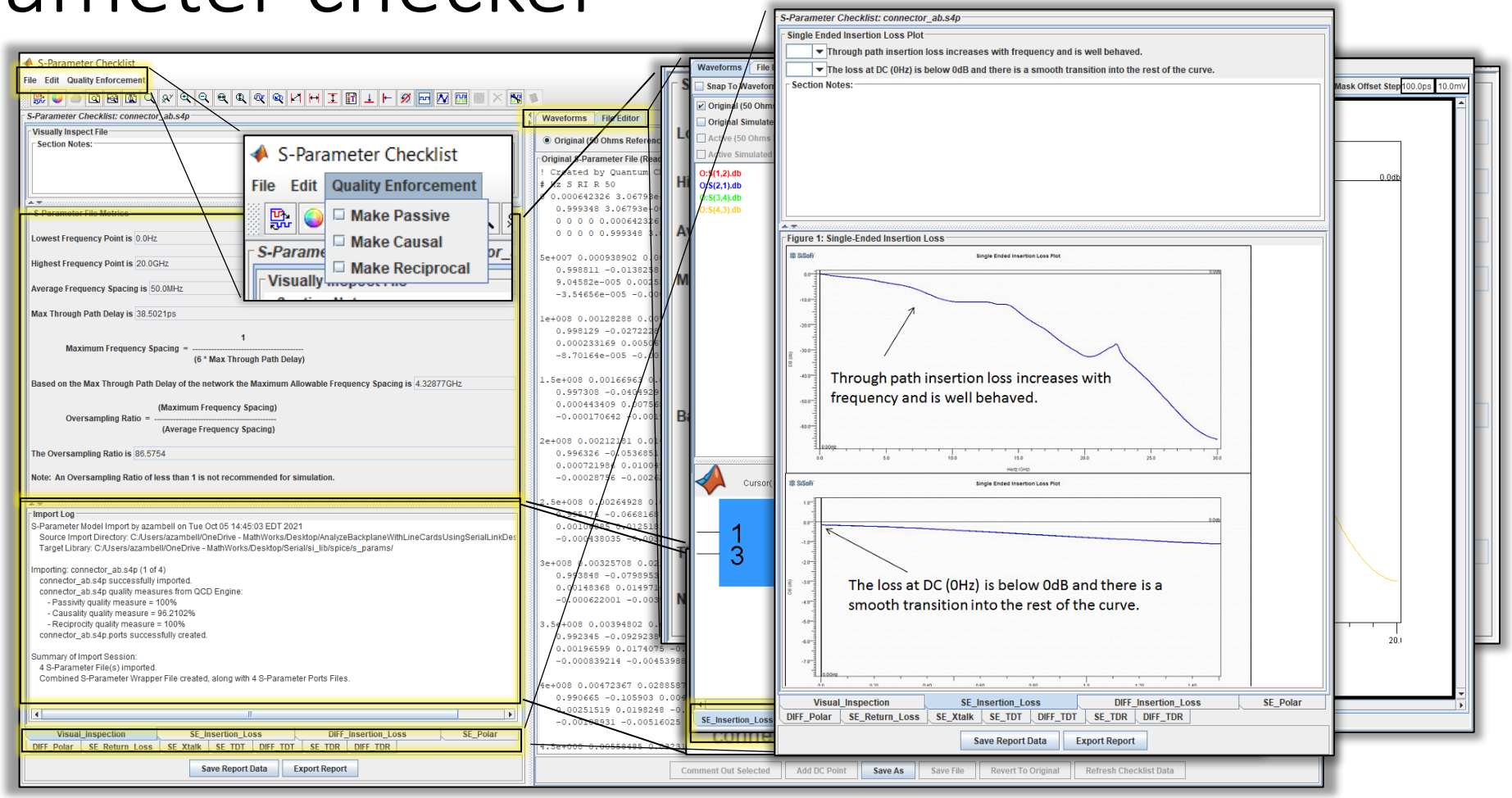
Import and manage various types of models



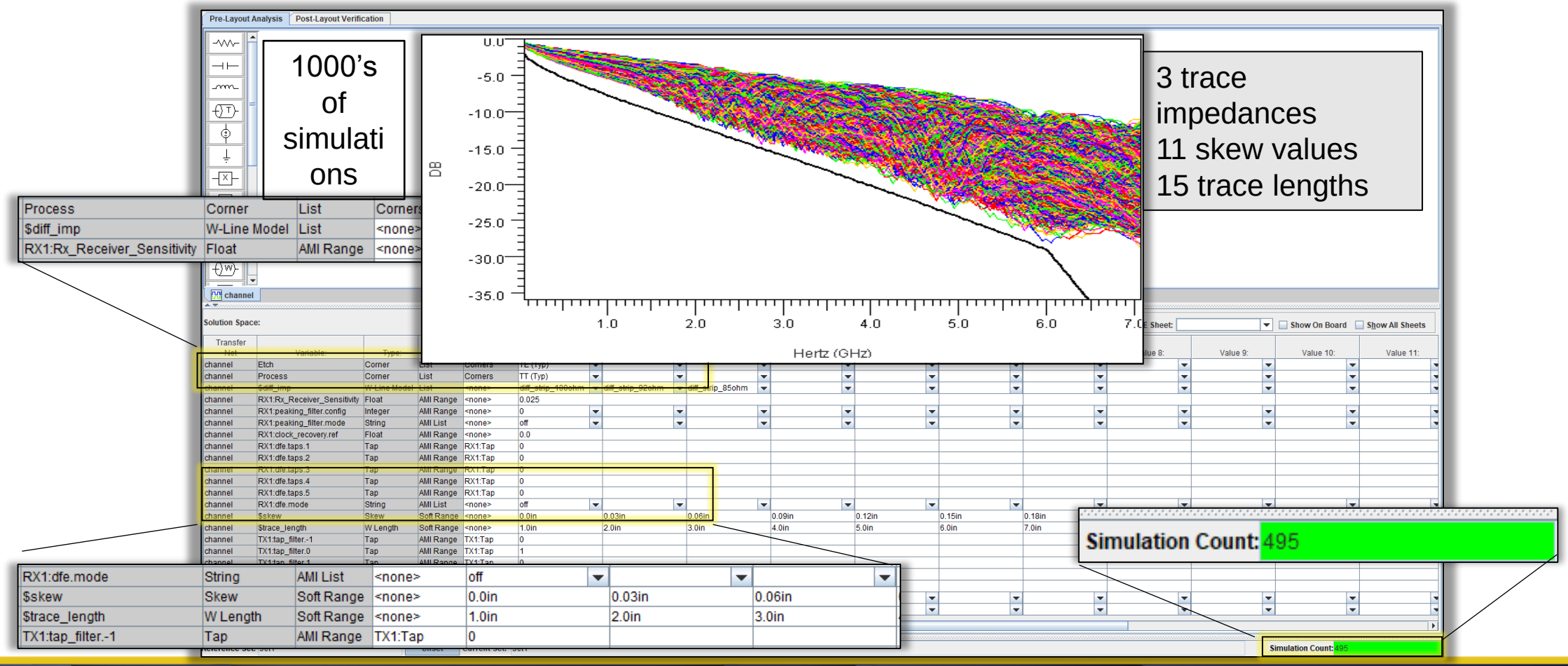


When importing S-Parameters, use the S-Parameter Checklist to verify their quality before use

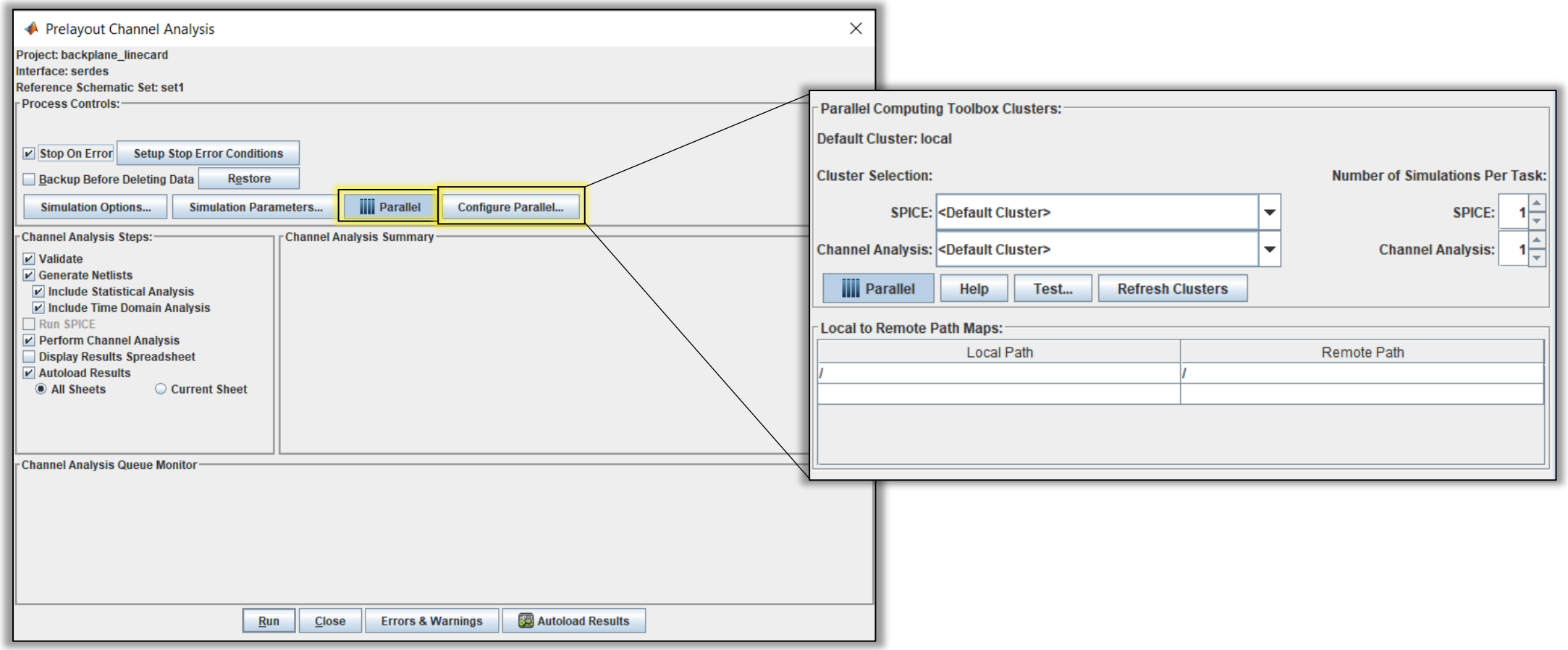
S-parameter checker



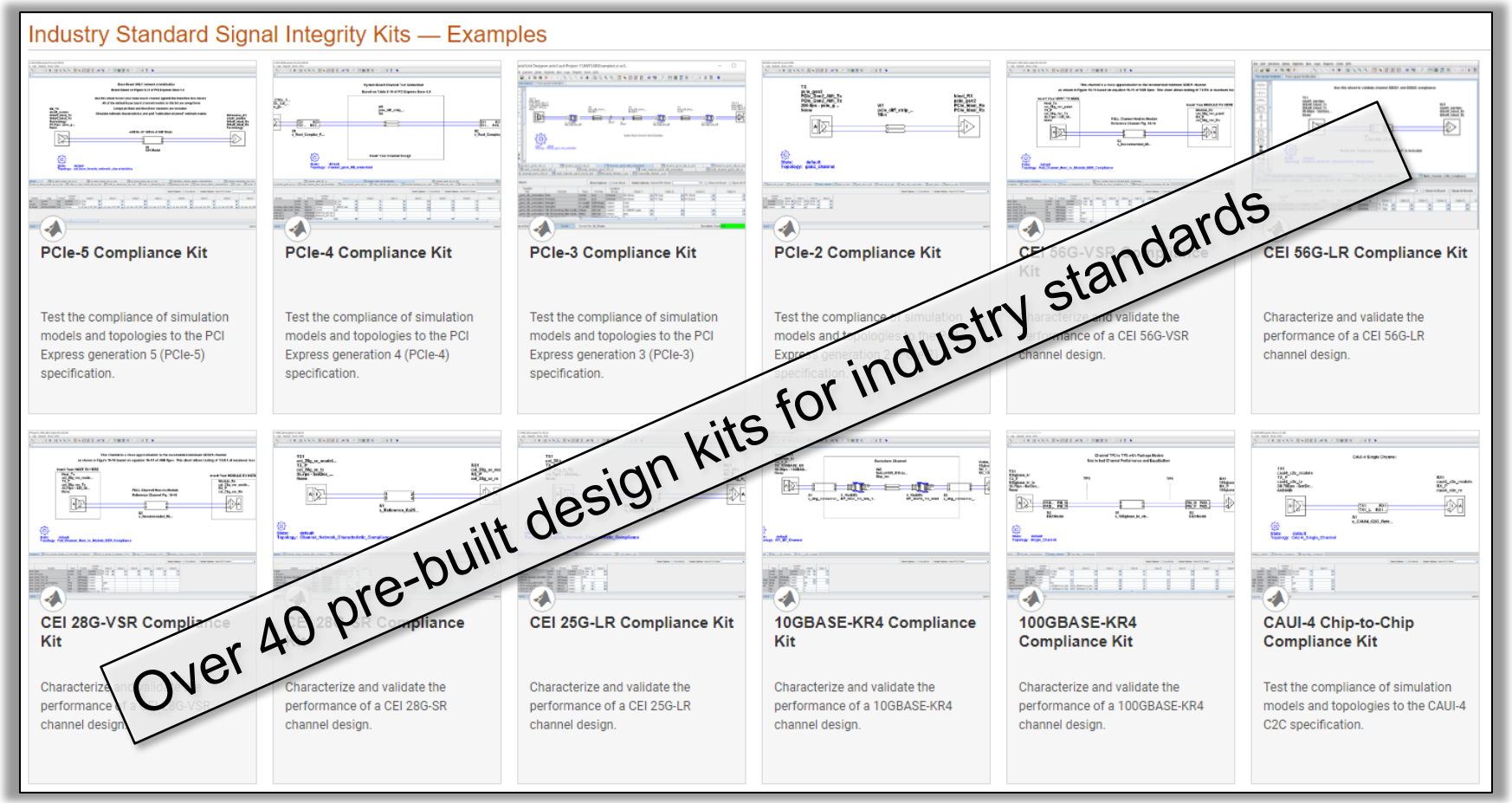
Design Space Exploration – Sweep parameter



Design Space Exploration - Parallelization

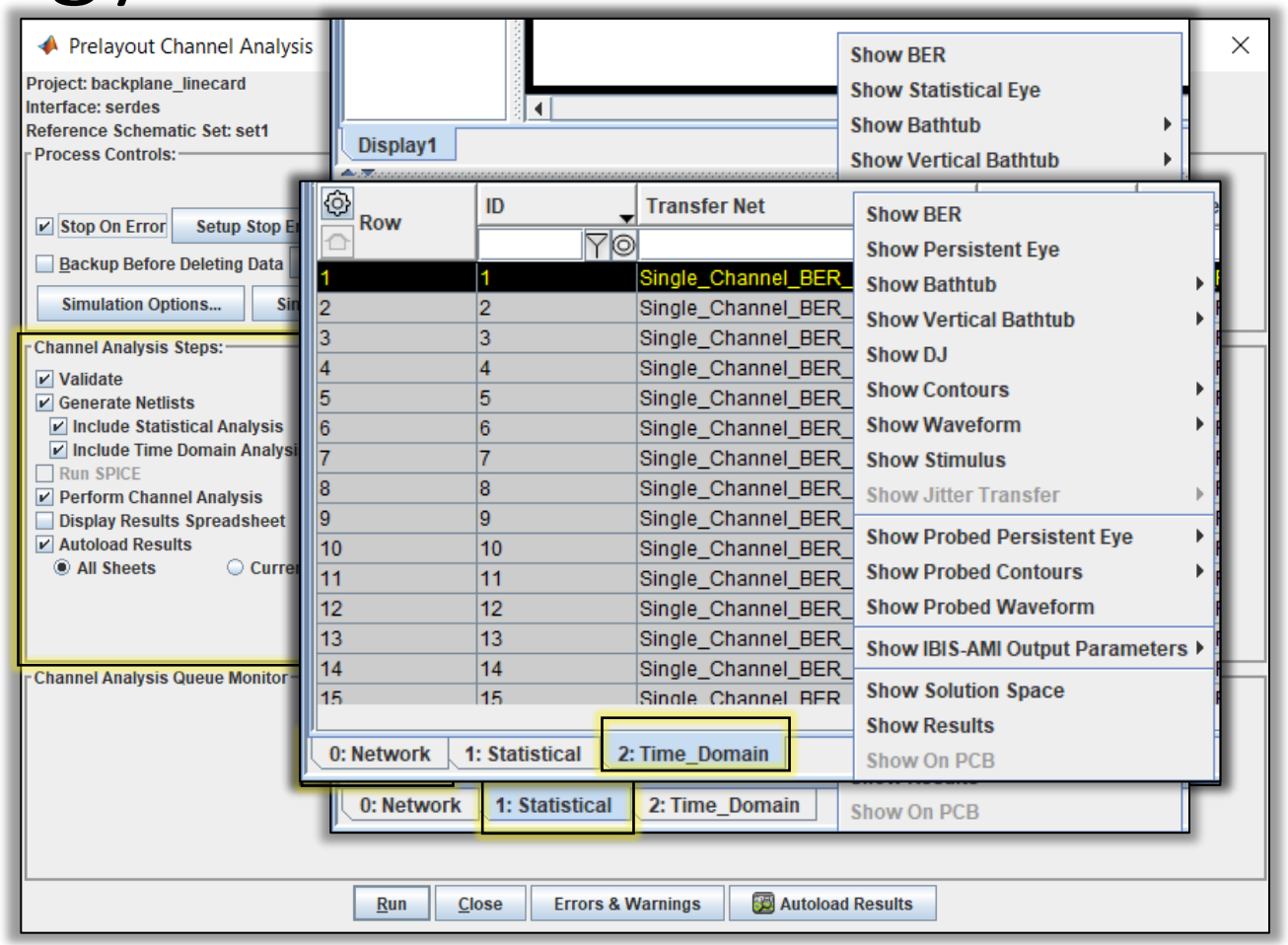


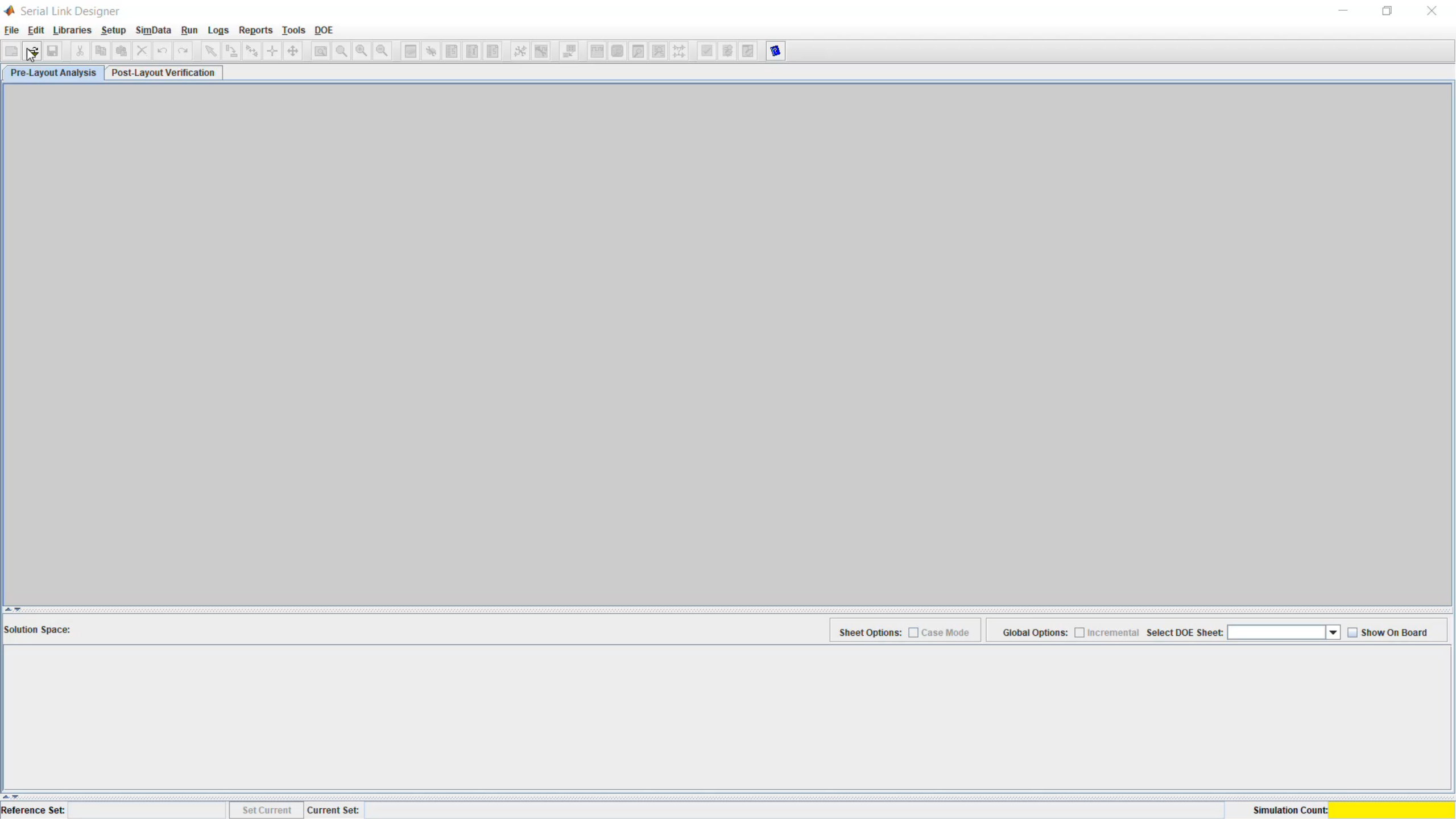
Design Kit for Industry Standards



Simulation Technology

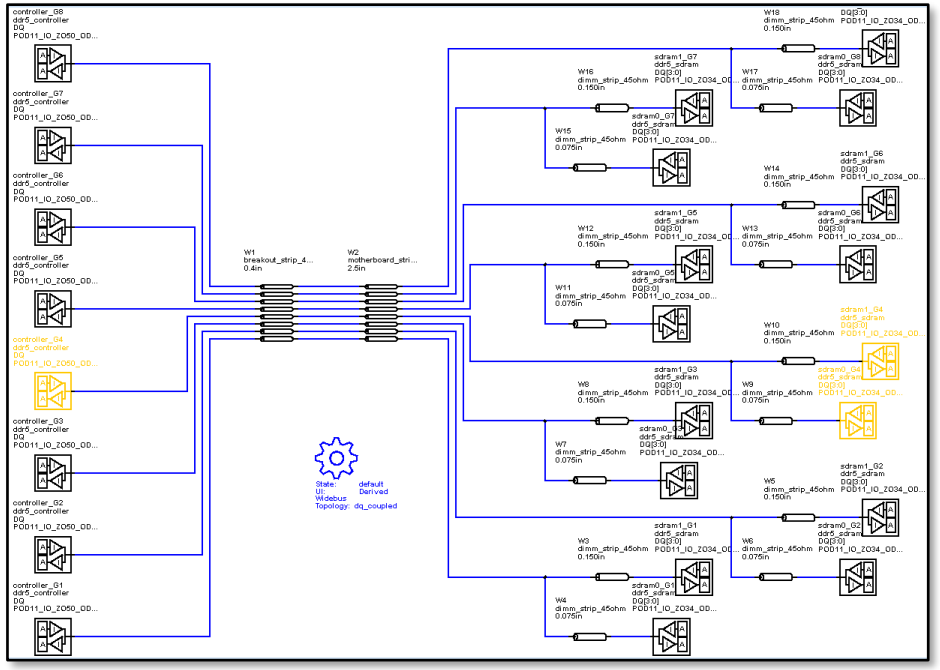
- Perform Channel Analysis – provides network characterization results which includes un-equalized system responses such as impulse response, step response, pulse response, S-Parameters, transfer functions, and more.
- Include Statistical Analysis – results such as statistical eye, BER, bathtub, contour, crosstalk, and more.
- Include Time-Domain Analysis – results such as persistent eye, BER, bathtub, contour, deterministic jitter probability function, crosstalk, and more.




Serial Link Designer
File Edit Libraries Setup SimData Run Logs Reports Tools DOE
Pre-Layout Analysis
Post-Layout Verification
Solution Space:
Sheet Options: Case Mode
Global Options: Incremental
Select DOE Sheet:
Show On Board
Reference Set:
Set Current
Current Set:
Simulation Count:

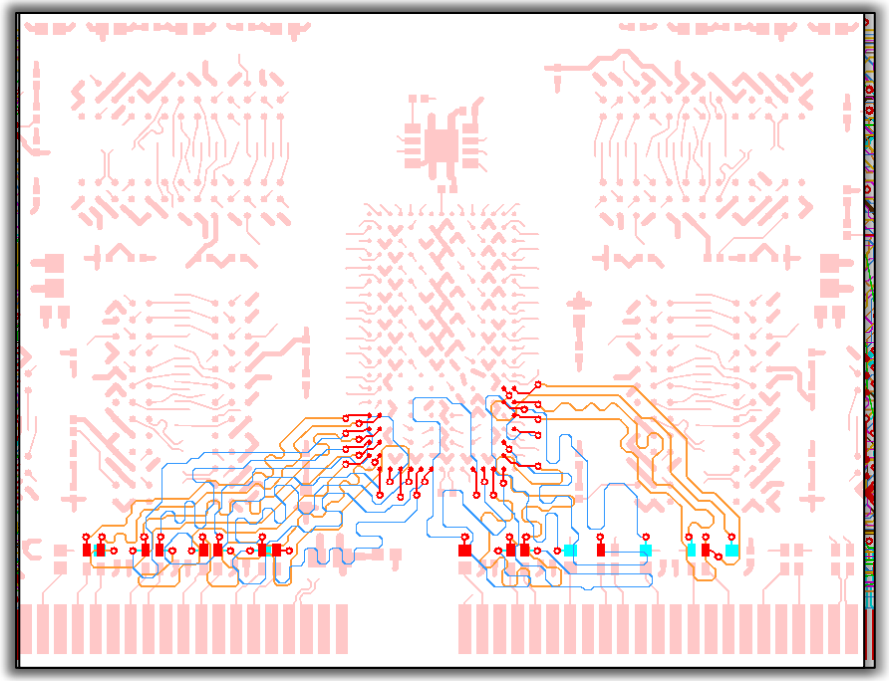
Post-layout

Pre-layout



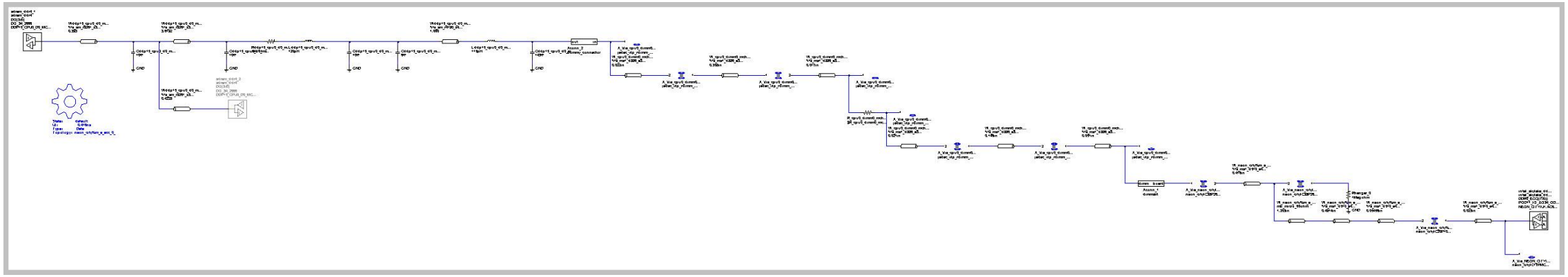
- Use RF PCB Toolbox to import PCB files
- Compare pre- and post-layout nets to each other
- Easily identify any issues
- Incorporate fixes and re-simulate

Post-layout



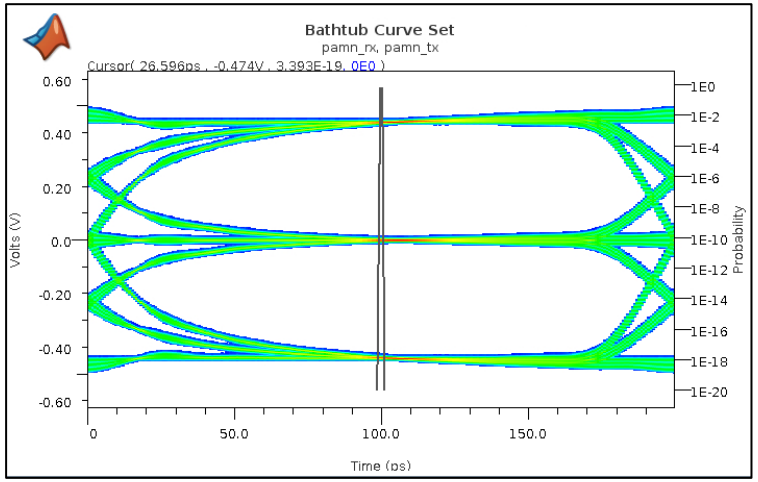
- Altium Designer
- Cadence Allegro
- Cadence APD
- IBIS EBD
- Intercept Pantheon
- Mentor Board Station
- Mentor Expedition PCB
- Mentor PADS Layout
- ODB++
- Zuken

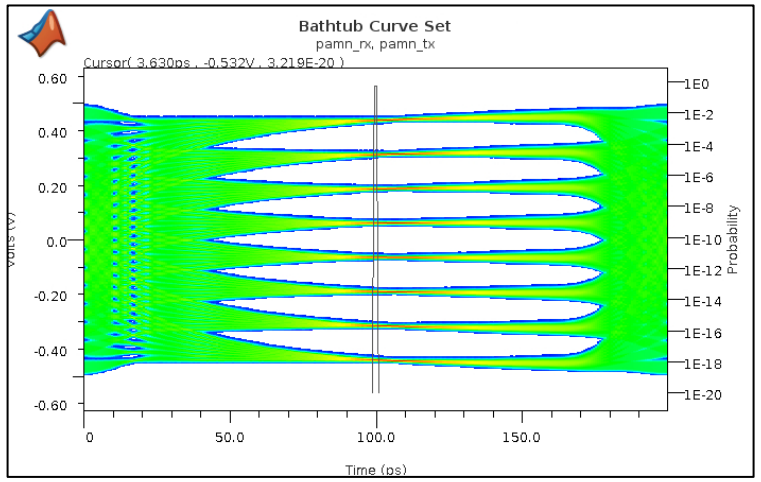
Post-layout to Pre-layout

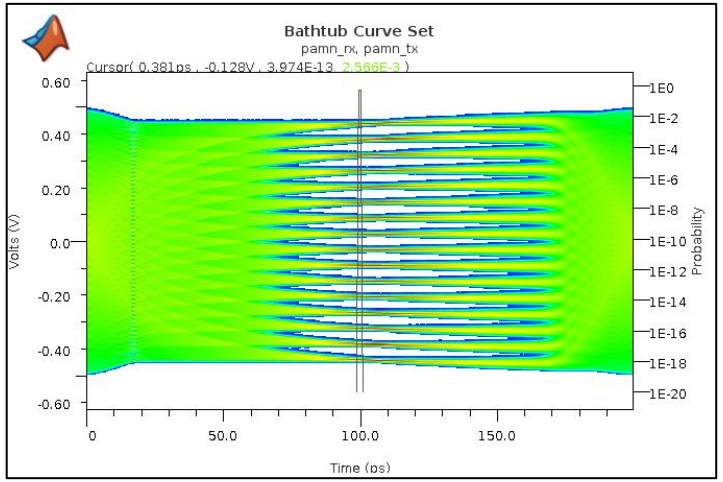


- Includes etch, vias, connectors, and discrete components for each board
- Topology can now be modified using Pre-Layout GUI to find solution

New for R2022b – PAMn IBIS-AMI Model Support

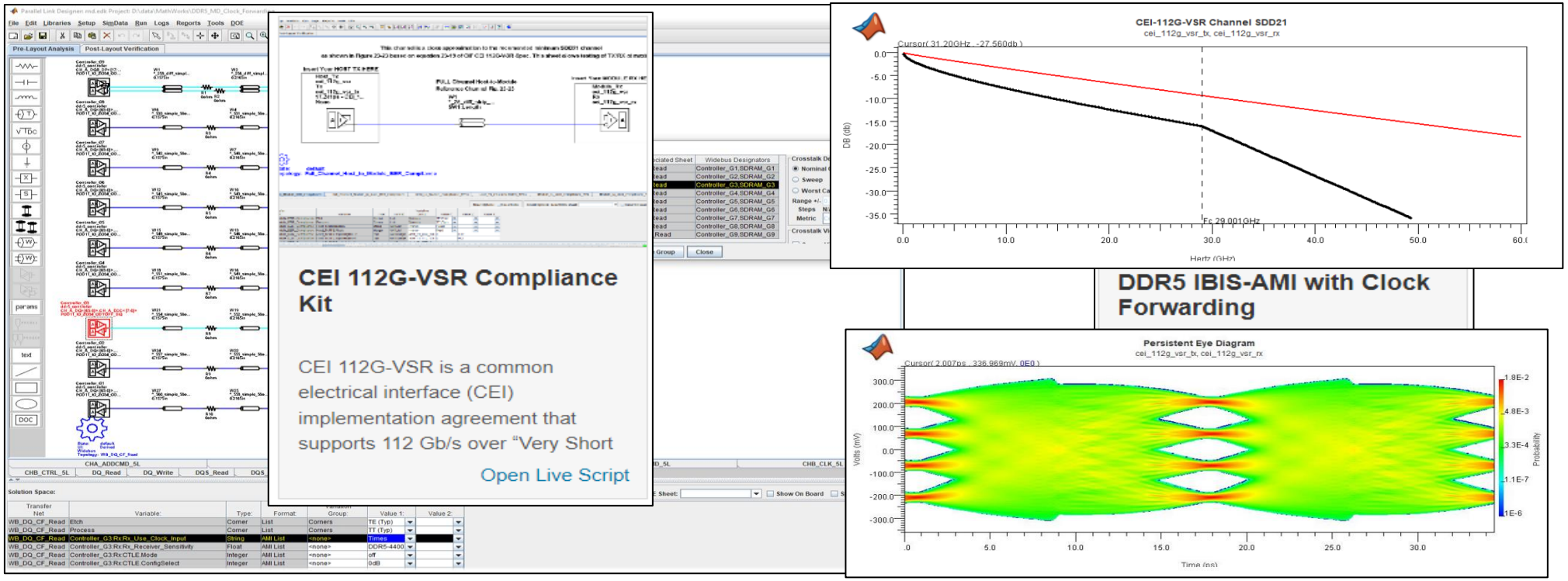






Now use IBIS-AMI models with PAM3, PAM8, PAM16 modulation for use with next generation USB4, GDDR7, MIPI A-PHY, and Automotive SerDes Alliance Motion Link

New for R2022b – Design Kits for Industry Standards



Two DesignCon 2022 Best Paper Award Winners!

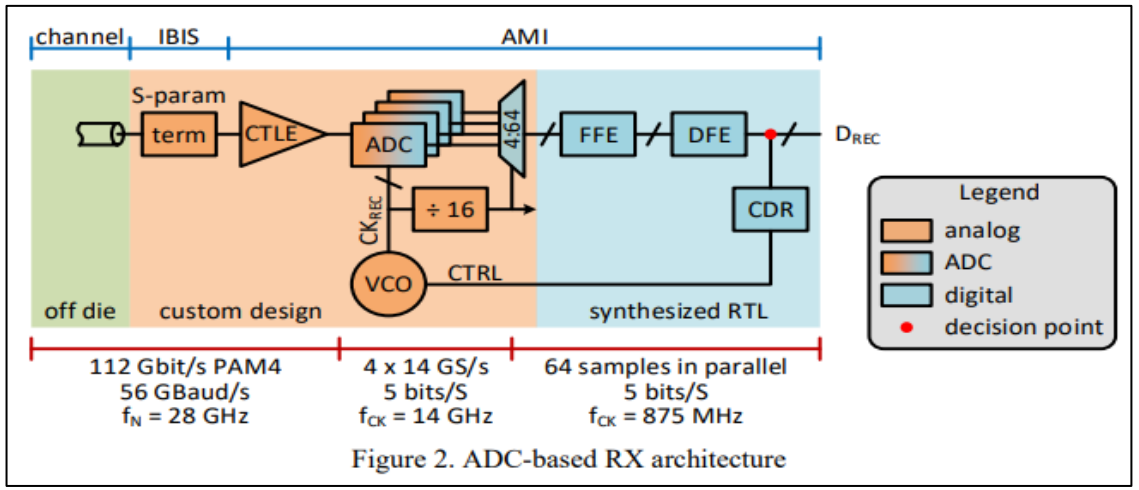


Figure 2. ADC-based RX architecture

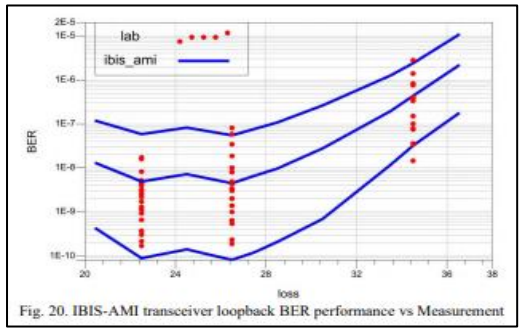


Fig. 20. IBIS-AMI transceiver loopback BER performance vs Measurement

DESIGNCON 2022
WHERE THE CHIP MEETS THE BOARD

IBIS-AMI Modeling and Correlation Methodology for ADC-Based SerDes Beyond 100 Gb/s

Aleksey Tyshchenko, SeriaLink Systems
aleksey@serialinksystems.com

David Halupka, SeriaLink Systems

Richard Allred, MathWorks

Tripp Worrell, MathWorks

Barry Katz, MathWorks

Clinton Walker, Alphawave IP

Adrien Auge, Alphawave IP

Infineon Accelerates Development of IBIS-AMI Models for SerDes Designs

Challenge

Produce a complete IBIS-AMI model of a SerDes system for a key customer on an aggressive schedule

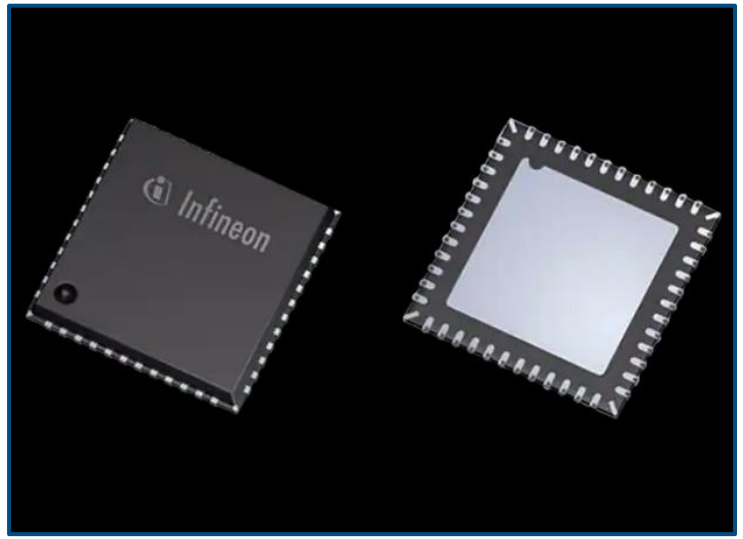
Solution

Use Simulink and SerDes Toolbox to develop, verify, and deliver an IBIS-AMI model in two weeks

Results

- **Complete IBIS-AMI models delivered in two weeks**
- Development ramp-up accelerated
- In-house IBIS-AMI capability developed

Link to user story

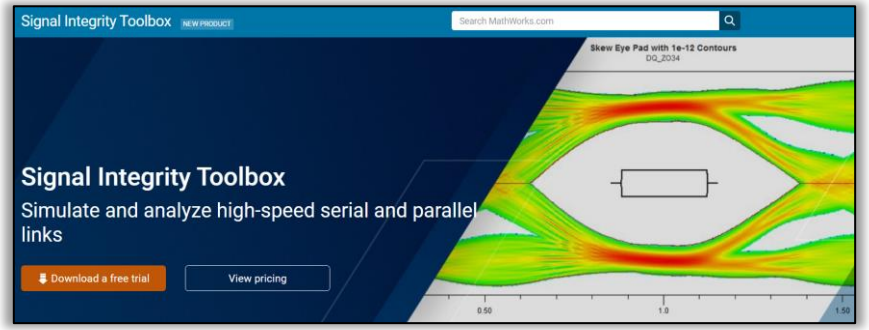


Infineon semiconductor.

"The process of creating and configuring IBIS-AMI models with SerDes Toolbox is straightforward and fast to learn. After completing it once ourselves, we had full control over IBIS-AMI model creation, and eliminated our dependence on contractors."

- Syed Babar Raza, Infineon

Summary


Signal Integrity Toolbox
NEW PRODUCT
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Skew Eye Pad with 1e-12 Contours
DQ_2034
Signal Integrity Toolbox
Simulate and analyze high-speed serial and parallel links
Download a free trial
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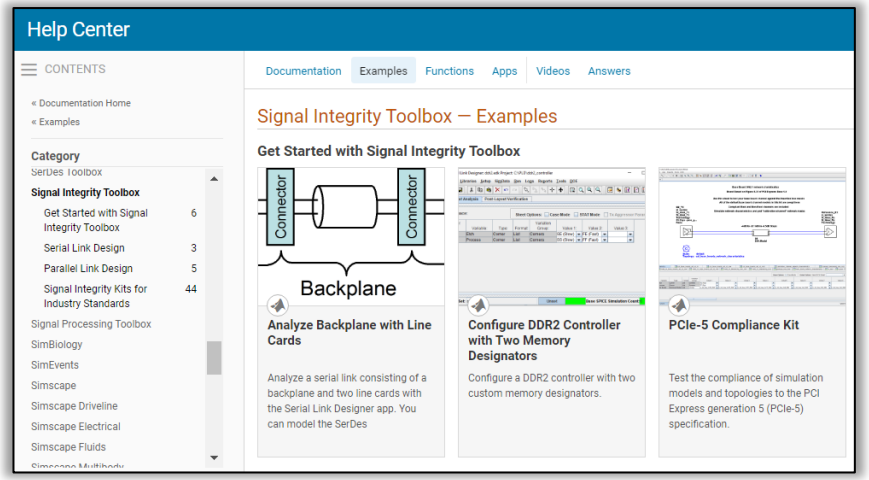
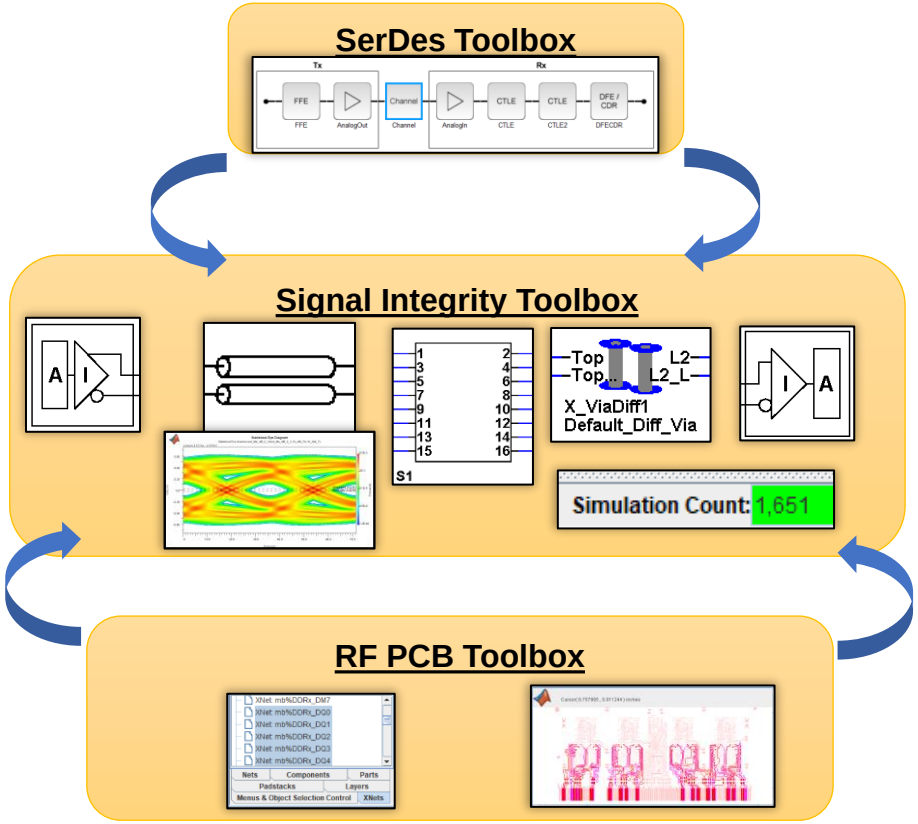

Help Center
CONTENTS
« Documentation Home
« Examples
Category
SerDes Toolbox
Signal Integrity Toolbox
Get Started with Signal Integrity Toolbox 6
Serial Link Design 3
Parallel Link Design 5
Signal Integrity Kits for Industry Standards 44
Signal Processing Toolbox
SimBiology
SimEvents
Simscape
Simscape Driveline
Simscape Electrical
Simscape Fluids
Documentation
Examples
Functions
Apps
Videos
Answers
Signal Integrity Toolbox — Examples
Get Started with Signal Integrity Toolbox
Connector
Connector
Backplane
Analyze Backplane with Line Cards
Analyze a serial link consisting of a backplane and two line cards with the Serial Link Designer app. You can model the SerDes
Configure DDR2 Controller with Two Memory Designators
Configure a DDR2 controller with two custom memory designators.
PCIe-5 Compliance Kit
Test the compliance of simulation models and topologies to the PCI Express generation 5 (PCIe-5) specification.


SerDes Toolbox
Tx
Rx
FFE
Channel
CTLE
CTLE
DFE / CDR
Signal Integrity Toolbox
A
I
S1
Top
Top...
L2
L2_L
X_ViaDiff1
Default_Diff_Via
I
A
Simulation Count: 1,651
RF PCB Toolbox
Nets
Components
Parts
Padstacks
Layers
Menus & Object Selection Control
XNets

Key takeaway

- Start with statistical analysis
- Refine model with architectural/circuit-level details
- Generate IBIS-AMI model ensuring equivalence
- Regression testing with different channels
- Make sure there is enough margins in all conditions
- Compliance check with the standard

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DECEMBER 6 - 7, 2022

Questions?

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