



2022  
DESIGN AND VERIFICATION™  
**DVCON**  
CONFERENCE AND EXHIBITION  
**EUROPE**  
MUNICH, GERMANY  
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# Taking Design Automation to the next level with User Experience Design

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# The Team



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**Bodo Hoppe**

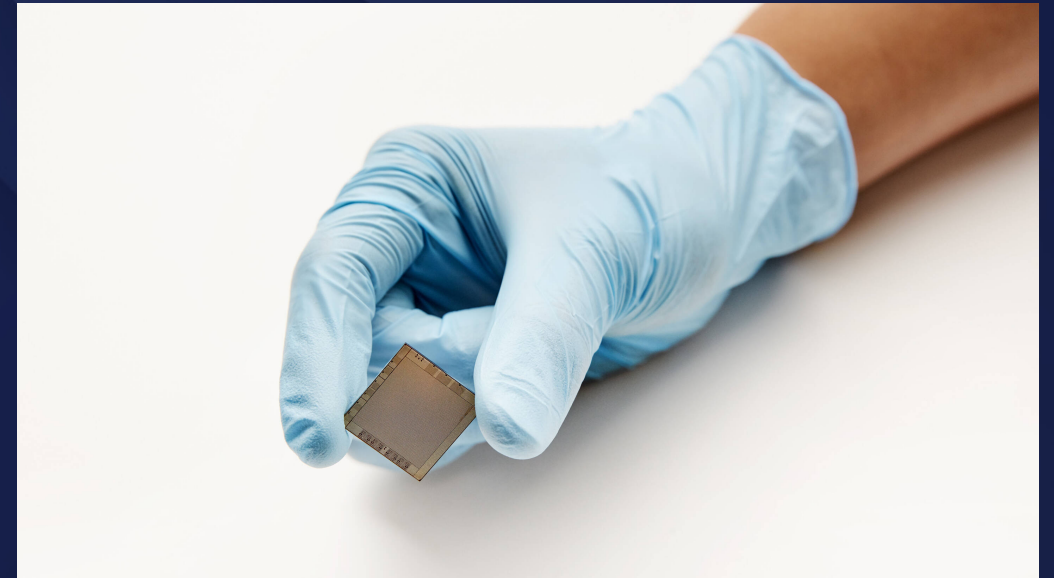
Distinguished engineer, IBM Z Hardware  
[bohopp@de.ibm.com](mailto:bohopp@de.ibm.com)

# The IBM Telum Processor

> 5 GHz  
frequency

> 22 Billion  
Transistors on a module

> 19 Miles  
of wires on a module



# Development of the IBM Telum Processor

1,500,000,000,000,000  
Simulation Cycles in software Simulation

> 500K  
unique discrete coverage events in the  
design

+ Millions of  
cross-product events

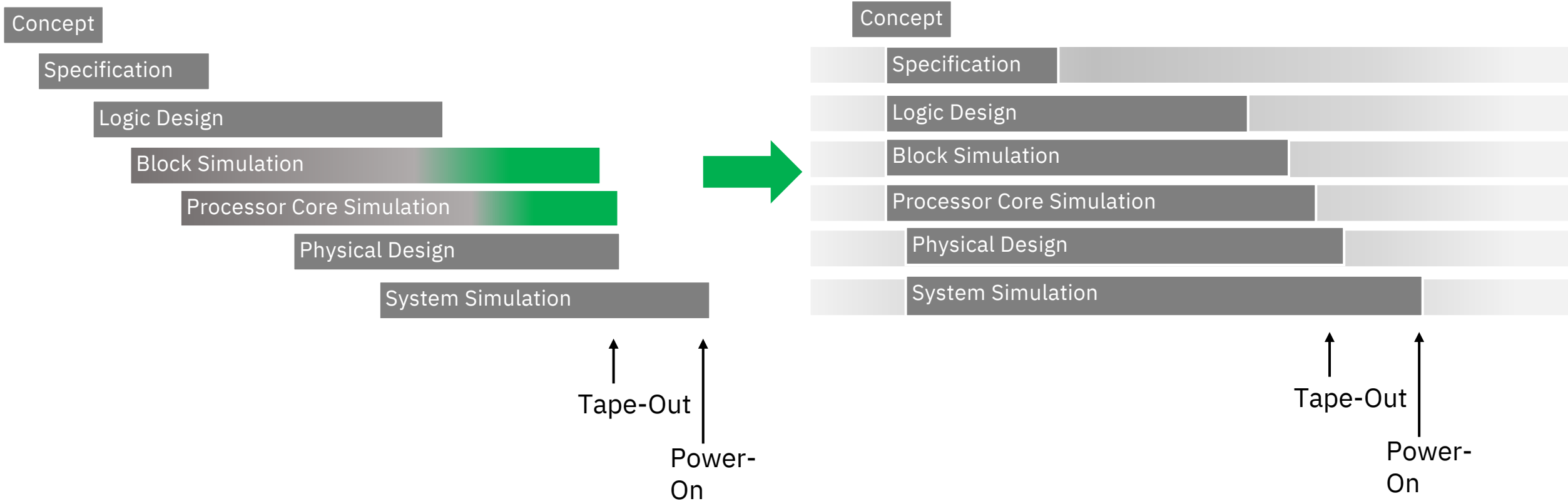


# Logic Designers and Verification Engineers spend a huge amount of time on

- Defining coverage
- Implementing coverage
- Debugging coverage
- Analyzing coverage holes
- **Hitting important coverage events**

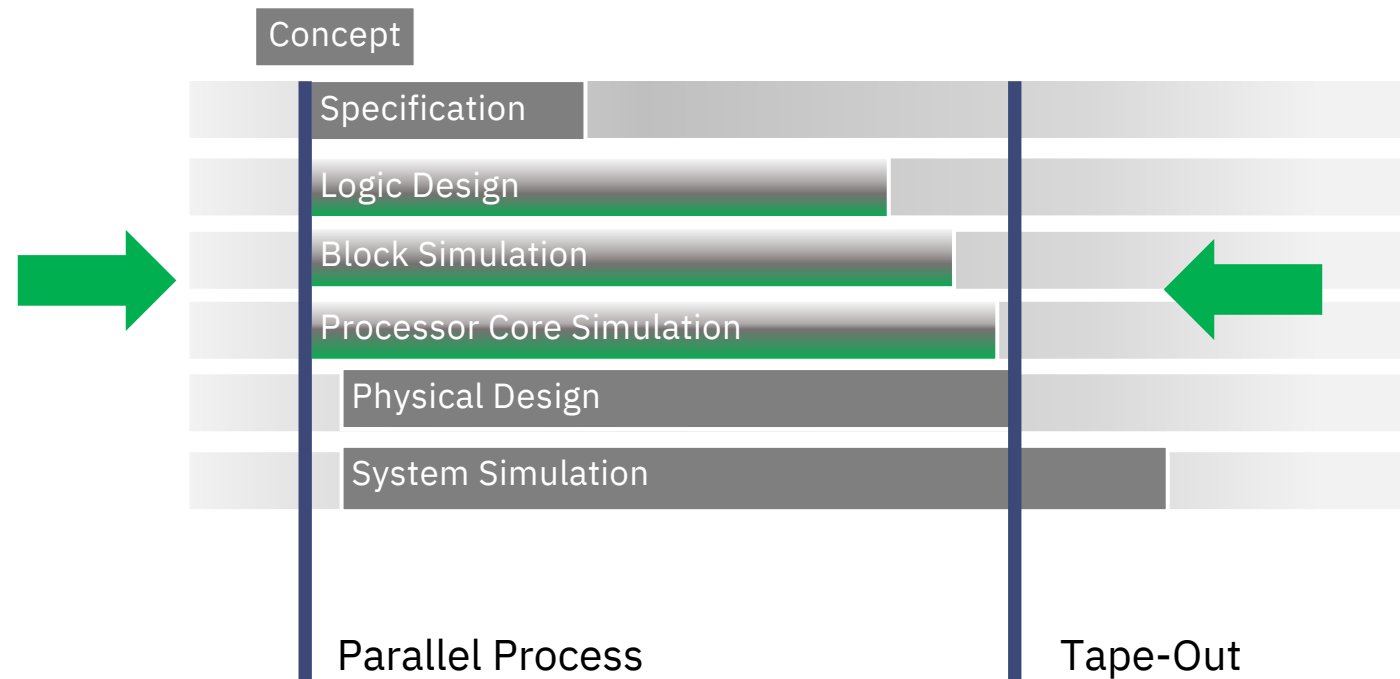


# Fast time to market



# Potential of Functional Coverage

- Faster time-to-market
- Higher Quality
- Less (Compute) Cost



# We use various functional coverage types



Functional Coverage  
Types

- ✓ Interface coverage
- ✓ (Micro-)Architectural cross product coverage
- ✓ Configuration coverage
- ✓ Discrete design events
- ✓ Testbench coverage

# We have (some) collaboration



Collaboration

- ✓ Mark as waived/deferred/impossible
- ✓ Analyze
- ✓ Prioritize
- ✓ Comment

# We have the technology



Automation

- ✓ Template Aware Coverage
- ✓ Coverage Driven Generation
- ✓ Finding unhittable events
- ✓ Coverage hole analysis
- ✓ Grading events & test templates
- ✓ Identifying aged out events

<https://research.ibm.com/publications/template-aware-coverage-taking-coverage-analysis-to-the-next-level>  
<https://research.ibm.com/publications/automatic-scalable-system-for-the-coverage-directed-generation-cdg-problem>

# But...

- Many months are still spent on coverage closure
  - In the critical path for tape-out
- We're still not seeing the forest because of all the trees
  - Missing potential bugs
- Still wasting compute cycles

Let's automate more ...

... and we can also ...

Functional Coverage  
Types

**The  
User**

Collaboration

Automation

Our tech and our tools can assist, but they  
cannot replace

How do we use the tools and tech we have in a way that will **enhance and augment** the user's abilities?



# Introducing... UX design!



**“Design a vase”**



**“Design a better way for someone to enjoy flowers”**



We look to these ways of questioning our problem spaces, to open up our creativity and scope, and to ask the Right Questions



# Enterprise design thinking: The loop

Observe

Reflect

Make



# UX design: An umbrella term

Observe

Reflect

Make

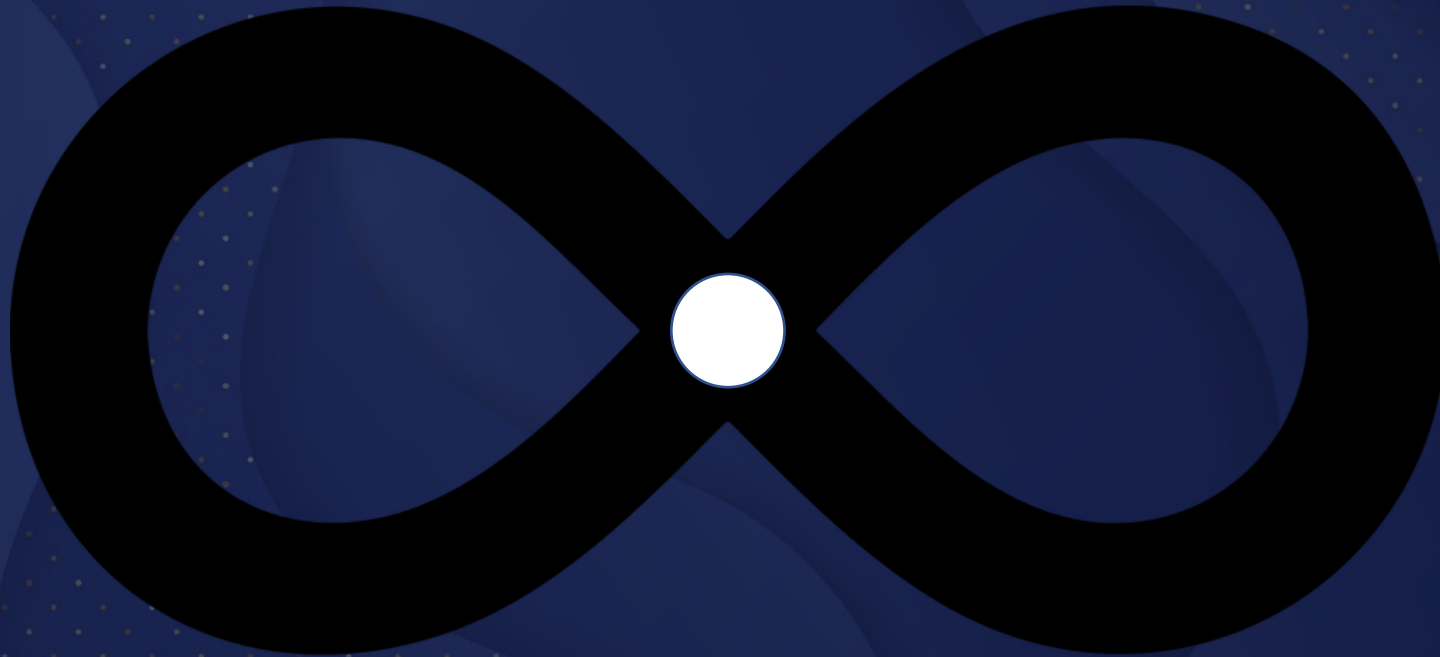
UX research

# UX design: An umbrella term

Observe

Reflect

Make



UX design  
Systems design  
Service design  
Product design

# UX design: An umbrella term

Observe

Reflect

Make



UI design  
Visual design  
Content design

# The original scope

- Improve the coverage data analysis experience
- Show user actions like waiving, deferring, marking impossible...

| Summary                |                |                 |                |                |  |  |  |  |  |
|------------------------|----------------|-----------------|----------------|----------------|--|--|--|--|--|
| Jun 27, 2022           |                |                 |                |                |  |  |  |  |  |
| Date                   | Test           | Core            | L3_ALL         | Total          |  |  |  |  |  |
| Jun 27, 2022           | 2 B            | 8 B             | 5 B            | 15 B           |  |  |  |  |  |
| Cycles                 | 18 K           | 106 K           | 61 K           | 185 K          |  |  |  |  |  |
| Testcases              | 165,534        | 147,979         | 17,585         |                |  |  |  |  |  |
| Raw Total Events       | 130,809        | 118,656         | 14,918         | 118,000        |  |  |  |  |  |
| Total Events           | 74,288 (56.8%) | 97,096 (81.8%)  | 10,120 (67.8%) | 73,830 (62.7%) |  |  |  |  |  |
| Covered                | 6,906 (5.3%)   | 11,230 (9.5%)   | 408 (2.7%)     | 6,819 (5.8%)   |  |  |  |  |  |
| Lightly Covered        | 81,194 (62.1%) | 108,326 (91.3%) | 10,528 (70.6%) | 80,749 (68.4%) |  |  |  |  |  |
| Covered+Lightly        | 48,615 (37.9%) | 10,330 (8.7%)   | 4,390 (28.4%)  | 37,251 (31.6%) |  |  |  |  |  |
| Zero Hit               | 48,221 (37.6%) | 7,255 (6.1%)    | 3,191 (21.4%)  | 8,948 (7.6%)   |  |  |  |  |  |
| Never Hit              | 394 (0.3%)     | 3,075 (2.6%)    | 1,199 (8.0%)   | 13 (0.0%)      |  |  |  |  |  |
| Aged Out               | 75             | 88              | 21             | 0              |  |  |  |  |  |
| Aged Out last day      | 394            | 1,100           | 54             | 2              |  |  |  |  |  |
| Aged Out last week     | 394            |                 |                |                |  |  |  |  |  |
| Aged Out last month    | 394            |                 |                |                |  |  |  |  |  |
| Defined last week      | 365            |                 |                |                |  |  |  |  |  |
| Recently Hit last week | 1,362          |                 |                |                |  |  |  |  |  |
| Impossible             | 34,710         |                 |                |                |  |  |  |  |  |
| Impossible Hit         | 15             |                 |                |                |  |  |  |  |  |
| Failed Hit             | 2              |                 |                |                |  |  |  |  |  |

| BugSpray Events   |       |                  |          |  |          |        |        |        |   |
|-------------------|-------|------------------|----------|--|----------|--------|--------|--------|---|
| zms1 / Core / CL3 |       |                  |          |  |          |        |        |        |   |
| All               |       |                  |          |  |          |        |        |        |   |
| Jun 27, 2022      |       |                  |          |  |          |        |        |        |   |
| Events            |       |                  |          |  |          |        |        |        |   |
| Waived            |       |                  |          |  |          |        |        |        |   |
| Hit Failures      |       |                  |          |  |          |        |        |        |   |
| Newly Hit         |       |                  |          |  |          |        |        |        |   |
| Aged Out          |       |                  |          |  |          |        |        |        |   |
| Zero Everywhere   |       |                  |          |  |          |        |        |        |   |
| Counts            |       |                  |          |  |          |        |        |        |   |
| Core              |       |                  |          |  |          |        |        |        |   |
| L3_ALL            |       |                  |          |  |          |        |        |        |   |
| Total             |       |                  |          |  |          |        |        |        |   |
| Owner             |       |                  |          |  |          |        |        |        |   |
| Updater           |       |                  |          |  |          |        |        |        |   |
| Comment           |       |                  |          |  |          |        |        |        |   |
| Harvest           |       |                  |          |  |          |        |        |        |   |
| Y                 |       |                  |          |  |          |        |        |        |   |
| Row               | Y     | Tag              | Entity   | Variables                              | Variable | Y      | Y      | Y      | Y |
| 1                 | notag | c_trctrl_comp    | trctrl   | max_inline_reached                     | 0        | 0      | Waived | 0      | 0 |
| 2                 | notag | c_trctrl_comp    | trctrl   | eff_bank_change                        | 0        | 0      | Waived | 0      | 0 |
| 3                 | notag | c_trctrl_comp    | trctrl   | scdm_active                            | 0        | 0      | Waived | 0      | 0 |
| 4                 | notag | c_trctrl_comp    | trctrl   | max_bigfsr_reached                     | 0        | 0      | Waived | 0      | 0 |
| 5                 | notag | c_trctrl_comp    | trctrl   | eff_extended_trig                      | 0        | 0      | Waived | 0      | 0 |
| 6                 | notag | c_trctrl_comp    | trctrl   | nonenh_store_on_trig                   | 0        | 0      | Waived | 0      | 0 |
| 7                 | notag | c_trctrl_comp    | trctrl   | enh_store_on_trig                      | 0        | 0      | Waived | 0      | 0 |
| 8                 | all   | c_direct_err_rpt | err_in   |  | Waived   | Waived | N/A    | Waived | 0 |
| 9                 | gold  | nx_grp_zenc      | compress | match_template_p0_g1_l12_p5_4_p7_1     | Waived   | 21 M   | N/A    | 21 M   | 0 |
| 10                | gold  | nx_grp_zenc      | compress | match_template_p0_g1_l12_p5_3_p7_2     | Waived   | 21 M   | N/A    | 21 M   | 0 |
| 11                | gold  | nx_grp_zenc      | compress | match_template_p1_g12_p5_4_p7_1        | Waived   | 22 M   | N/A    | 22 M   | 0 |
| 12                | gold  | nx_grp_zenc      | compress | match_template_p0_l1_p4_3_p5_p7_2      | Waived   | 24 M   | N/A    | 24 M   | 0 |
| 13                | gold  | nx_grp_zenc      | compress | match_template_p1_g12_p5_3_p7_3        | Waived   | 22 M   | N/A    | 22 M   | 0 |
| 14                | gold  | nx_grp_zenc      | compress | match_template_p1_g12_p5_4_p7_2        | Waived   | 22 M   | N/A    | 22 M   | 0 |
| 15                | rit   | nx_grp_zenc      | compress | current_byte7_match_generates_symbol_8 | Waived   | 267 K  | N/A    | 267 K  | 0 |
| 16                | rit   | nx_grp_zenc      | compress | current_byte7_match_generates_symbol_2 | Waived   | 115 K  | N/A    | 115 K  | 0 |
| 17                | rit   | nx_grp_zenc      | compress | current_byte7_match_generates_symbol_5 | Waived   | 81 K   | N/A    | 81 K   | 0 |
| 18                | rit   | nx_grp_zenc      | compress | current_byte6_match_generates_symbol_1 | Waived   | 204 K  | N/A    | 204 K  | 0 |
| 19                | gold  | nx_grp_zenc      | compress | match_template_p3_g14_4_5_p7_4         | Waived   | 21 M   | N/A    | 21 M   | 0 |
| 20                | gold  | nx_grp_zenc      | compress | match_template_p3_g14_4_5_p7_1         | Waived   | 21 M   | N/A    | 21 M   | 0 |
| 21                | rit   | nx_grp_zenc      | compress | current_byte6_match_generates_symbol_4 | Waived   | 204 K  | N/A    | 204 K  | 0 |
| 22                | rit   | nx_grp_zenc      | compress | current_byte4_match_generates_symbol_3 | Waived   | 234 K  | N/A    | 234 K  | 0 |
| 23                | rit   | nx_grp_zenc      | compress | current_byte4_match_generates_symbol_6 | Waived   | 123 K  | N/A    | 123 K  | 0 |
| 24                | gold  | nx_grp_zenc      | compress | match_template_p0_g1_l12_p5_p7_4       | Waived   | 21 M   | N/A    | 21 M   | 0 |
| 25                | rit   | nx_grp_zenc      | compress | current_byte3_match_generates_symbol_5 | Waived   | 131 K  | N/A    | 131 K  | 0 |
| 26                | rit   | nx_grp_zenc      | compress | current_byte2_match_generates_symbol_0 | Waived   | 195 K  | N/A    | 195 K  | 0 |
| 27                | rit   | nx_grp_zenc      | compress | current_byte2_match_generates_symbol_4 | Waived   | 141 K  | N/A    | 141 K  | 0 |
| 28                | gold  | nx_grp_zenc      | compress | match_template_p0_l1_l2_p7_5           | Waived   | 24 M   | N/A    | 24 M   | 0 |
| 29                | rit   | nx_grp_zenc      | compress | byte0_7_matches_convert_to_4_symbols   | Waived   | 455 K  | N/A    | 455 K  | 0 |
| 30                | gold  | nx_grp_zenc      | compress | lzenc_casum_h_pipeline_casum_8_byte    | Waived   | 2 M    | N/A    | 2 M    | 0 |
| 31                | gold  | nx_grp_zenc      | compress | match_template_p0_g1_p3_p4_3_17        | Waived   | 22 M   | N/A    | 22 M   | 0 |
| 32                | gold  | nx_grp_zenc      | compress | match_template_p5_g16_p7_2             | Waived   | 21 M   | N/A    | 21 M   | 0 |
| 33                | gold  | nx_grp_zenc      | compress | match_template_p0_g1_p5_5_16_17        | Waived   | 22 M   | N/A    | 22 M   | 0 |
| 34                | gold  | nx_grp_zenc      | compress | match_template_p2_g13_p5_3_16_17       | Waived   | 22 M   | N/A    | 22 M   | 0 |
| 35                | gold  | nx_grp_zenc      | compress | match_template_p6_7_17                 | Waived   | 23 M   | N/A    | 23 M   | 0 |
| 36                | gold  | nx_grp_zenc      | compress | match_template_p2_g13_p5_14_16_17      | Waived   | 22 M   | N/A    | 22 M   | 0 |
| 37                | gold  | nx_grp_zenc      | compress | match_template_p3_4_p6_3_p7_1          | Waived   | 23 M   | N/A    | 23 M   | 0 |
| 38                | gold  | nx_grp_zenc      | compress | match_template_p0_p6_6_17              | Waived   | 23 M   | N/A    | 23 M   | 0 |
| 39                | gold  | nx_grp_zenc      | compress | match_template_p2_g13_p7_5             | Waived   | 21 M   | N/A    | 21 M   | 0 |
| 40                | gold  | nx_grp_zenc      | compress | match_template_p0_g1_p3_3_14_16_17_1   | Waived   | 22 M   | N/A    | 22 M   | 0 |
| 41                | gold  | nx_grp_zenc      | compress | match_template_p2_g13_13_p7_4          | Waived   | 21 M   | N/A    | 21 M   | 0 |

IBM Functional Coverage Analysis

team\_name

Overview

Discrete events

Summary

Events

Cross-Product Events

Holes

Model

gap\_in0

Select a

Hole

97 /

45 /

20 /

18 /

15 /

15 /

15 /

14 /

8 / 1

Items per p

Hole summary

Overview

Discrete events

Summary

Events

Cross-Product Events

All events

All events

Flagged Events

Event

Event Name

Entity

Tag / Function

CORE

CORE\_HYDRA

CORE\_ALL

RAS

PERF

event\_name\_1

caa\_ist\_cam\_imb

tag\_here\_12

2345

34543

0

7578

466

event\_name\_2

entity2

tag\_here\_12

0

0

0

0

0

a\_really\_long\_name\_for\_this

entity3

tag\_here\_13

218 M

23 B

2 B

485 M

23 M

name

entity3

tag\_here\_2

25 B

45 B

1234

34 B

21 M

other\_name

entity3

tag\_here\_21

111,485

1 M

2 M

99

event\_name\_3

entity5

tag\_here\_1234

2,345

0

0

0

0

0

short\_name\_23

entity12

0

0

21 M

0

0

event\_name\_6

entity1

tag\_here\_53

2345

34543

0

7578

466

short\_name\_112

entity1

tag\_here\_22

0

0

123

0

0

a\_really\_long\_name\_for\_this\_33

entity2

tag\_here\_76

321 M

344 M

367 M

0

0

event\_name\_7

entity3

tag\_here\_03

111,234

114,987

125,677

0

0

other\_name\_10

entity4

tag\_here\_24

0

0

0

11 M

12 M

Items per page: 15

1 - 15 of 100 items

1 of 10 pages

“This is just a facelift”

“What’s the point?”

“We already have something similar”

What we were doing: **treating the symptom of functional coverage**

A quick reminder...

<https://scrolller.com/ui-vs-ux-3iy0tb43v4>



What we should've been doing:  
investigating the **underlying issue...**

***Why are there so many irrelevant and  
confusing events in the first place?***

**“Design a way to  
improve the  
coverage data  
analysis experience”**

**~~“Design a way to  
improve the  
coverage data  
analysis experience”~~**

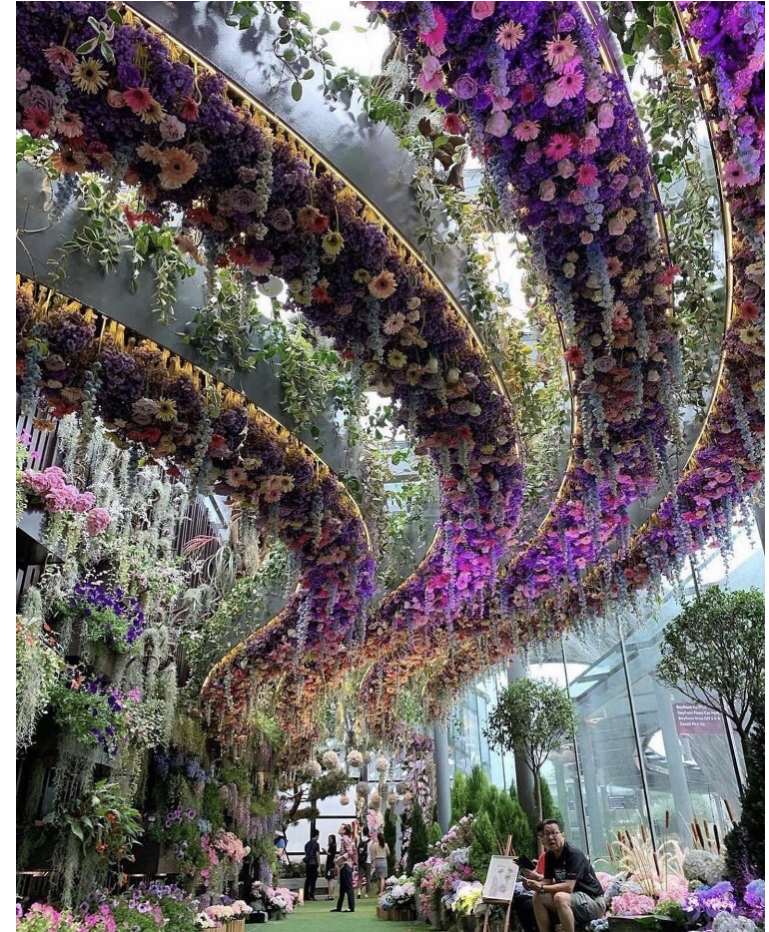
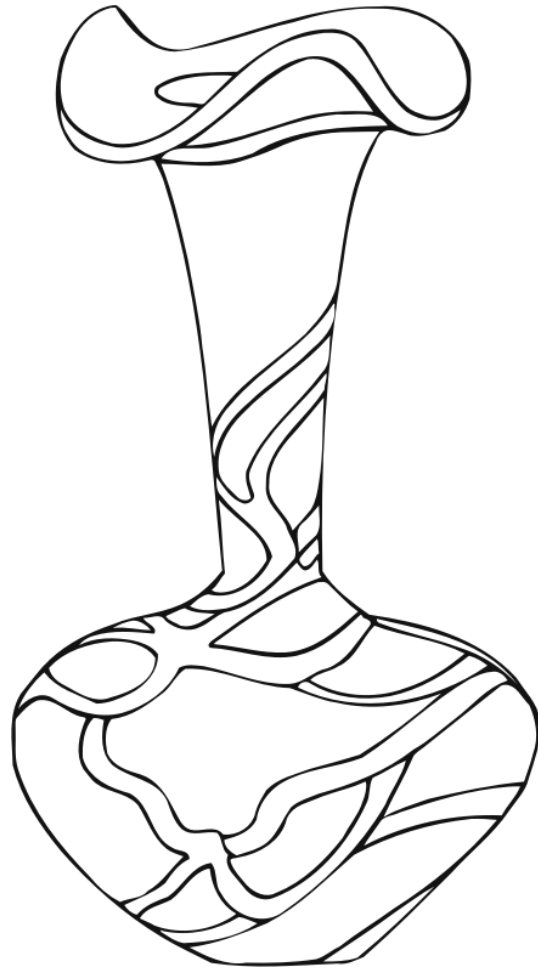
**“Design a way to  
close the design of  
the microprocessor  
faster”**

**Feature  
definition**

**Feature  
implementation**

**Coverage  
analysis**

**Coverage closure**



Floral fantasy at Gardens by the Bay, singapore  
by: @unique\_singapore [IG]

Observe

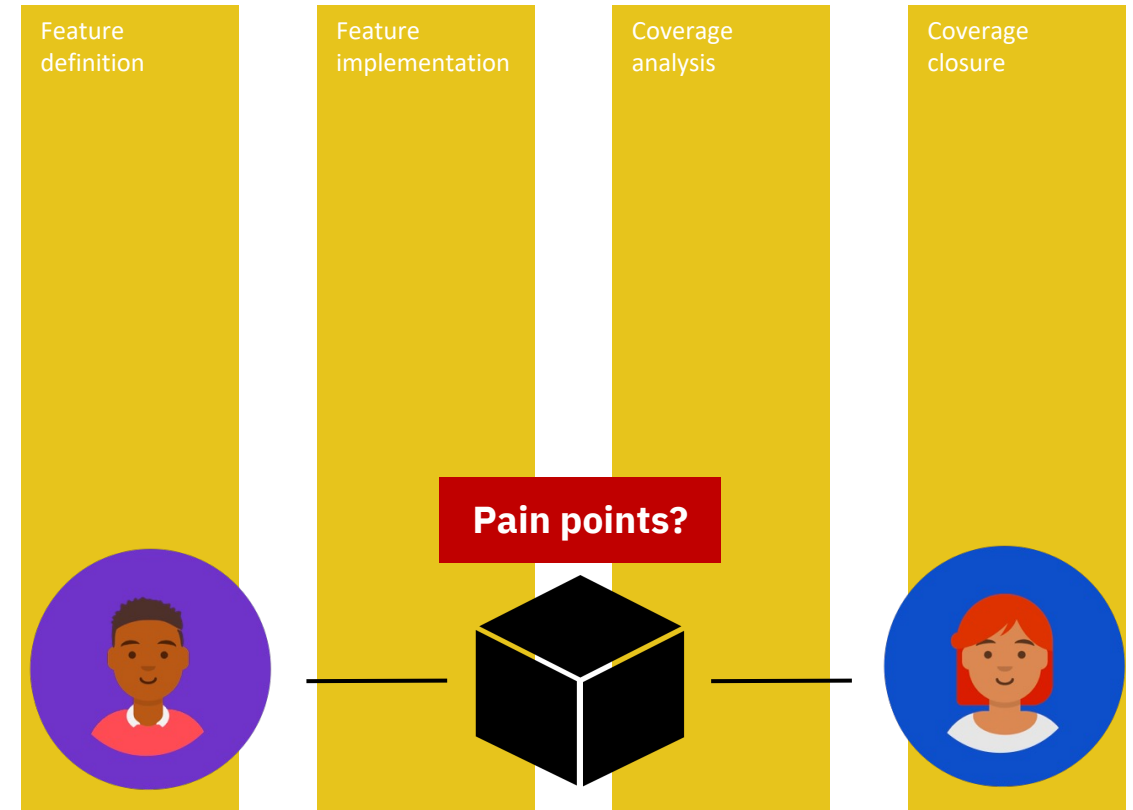
Reflect

Make



# User research questions

- What is the **overall process**, from feature definition to coverage closure?
- Where are the **collaboration touchpoints** between VE and LD?
- What are the **pain points** in this collaboration process?

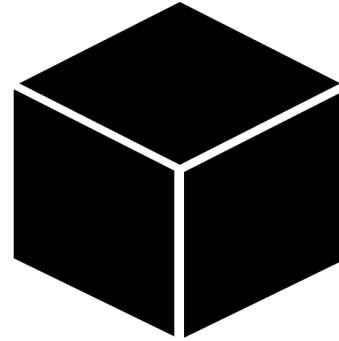


# Design toolbox: **Personas**



**Eddie**  
Logic Designer

Works with architects to define the new features of the chip  
Creates the logic design of the hardware  
Defines spaces that need verification, using things called “events”



Jobs to be done?  
Collaboration?  
Pain points?



**Vi**  
Verification Engineer

Creates test cases in C++ that stress the design of the chip  
Looking to improve their test bench to hit all important coverage events to find all bugs in the HW  
Sorts through all the events generated by the Verification Cockpit (VC) to look for the most interesting events

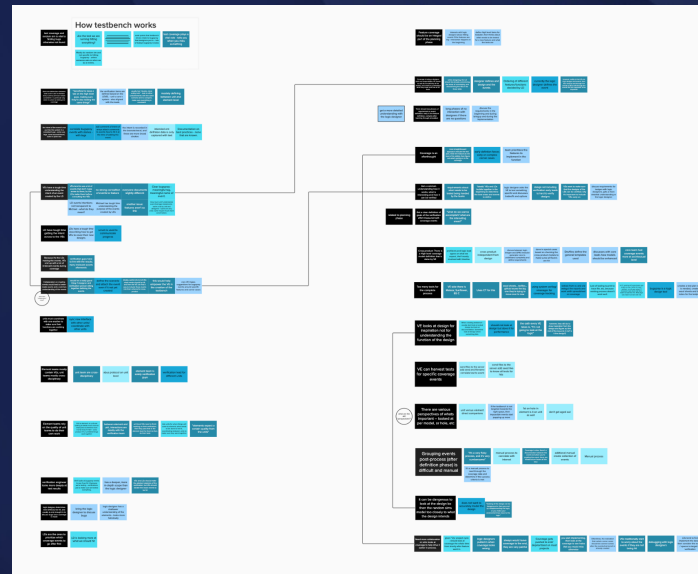
# Research

## Step 1: Observe



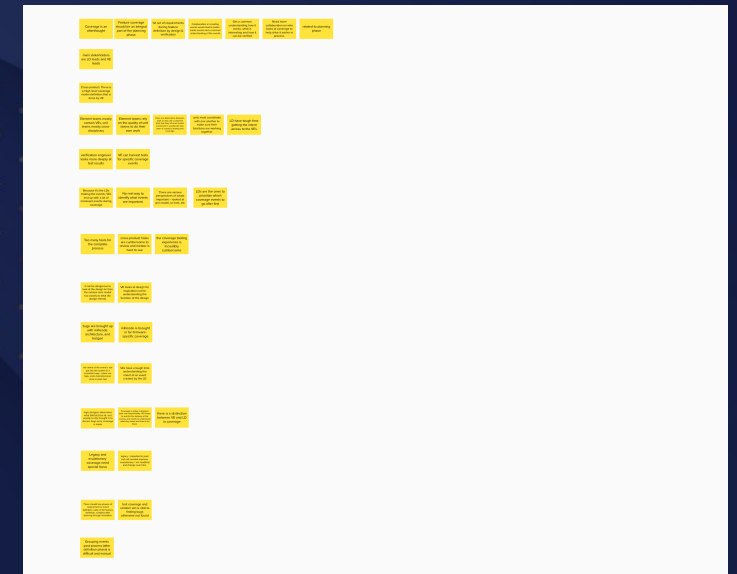
What does the user think/do?

## Step 2: Gather insights



What common attitudes and behaviors do our users collectively have?

## Step 3: Synthesize into big ideas



What are the main ideas we can gather from this?



# EDT toolkit: **As-is scenario**

# Designer toolkit: As-is scenario overview

## Phase 1

### Feature definition

- Main feature and design are defined here
- Eddie draws up the specs and designs with the architects
- Vi takes a back seat

## Phase 2

### Feature implementation Simulation bring-up

- Designs are created, simulation testing begins
- Eddie begins coding his designs
- Vi looks at the design specs in order to begin crafting her testbench scenarios

## Phase 3

### Coverage analysis

- Analysis of the testbench and discrete events begins
- Eddie and Vi collaborate to analyze the results.

## Phase 4

### Coverage closure

- Coverage must meet the expected quality requirements
- Vi writes special cases and continues to improve the testbench until the coverage percentage is high enough
- Eddie improves his designs

# Designer toolkit: As-is scenario overview

## Phase 1 Feature definition

- Main feature and design are defined here
- Eddie draws up the specs and designs with

Eddie is often asked to deliver both good design and good coverage

Vi does not participate in design scoping

## Phase 2 Feature implementation Simulation bring-up

- Designs are created, simulation testing begins
- Eddie begins design

Because Eddie must focus on his designs, this often results in the creation of improperly documented coverage

Vi is blocked from coverage until after the implementation of the designs by Eddie

## Phase 3 Coverage analysis

- Analysis of the testbench and discrete events begins
- Eddie and Vi collaborate

Vi, in turn, struggles with understanding the intent of events coded by Eddie

There is no central repository for proper collaboration

## Phase 4 Coverage closure

- Coverage must meet the expected quality requirements
- Vi writes spec and

Vi has no set definition of "done"

Eddie discovers bugs super late in the implementation phase because they were not caught by the testbench earlier

# Designer toolkit: As-is scenario overview

## Phase 1 Feature definition

- Main feature and design are defined here
- Eddie draws up the specs and designs with

Eddie is often asked to deliver both good design and good coverage

Vi does not participate in design scoping

## Phase 2 Feature implementation Simulation bring-up

- Designs are created, simulation testing begins
- Eddie begins design

Because Eddie must focus on his designs, this often results in the creation of improperly documented coverage

Vi is blocked from coverage until after the implementation of the designs by Eddie

## Phase 3 Coverage analysis

- Analysis of the testbench and discrete events begins
- Eddie and Vi collaborate

Vi, in turn, struggles with understanding the intent of events coded by Eddie

There is no central repository for proper collaboration

## Phase 4 Coverage closure

- Coverage must meet the expected quality requirements
- Vi writes spec

Vi has no set definition of "done"

Eddie discovers bugs super late in the implementation phase because they were not caught by the testbench

- Eddie discovers his designs

Observe

Reflect

Make





# EDT toolkit: To-be scenario

# How might we **activate** the users through **collaboration**?

## Pain points

- Eddie often asked to deliver both good design and good coverage
- Vi does not participate in design scoping

## To-be scenario

- Eddie defines the events **without implementation**, along with the scope of the stories
- Vi **collaborates earlier** to understand the scope and maps the events to the features created

# How might we **activate** the users through **collaboration**?

## Pain points

- Because Eddie must focus on his designs, this often results in the creation of improperly documented coverage
- Vi struggles to understand the coverage created by Eddie

## To-be scenario

- Eddie **provides the details** of the coverage space and the expected results to Vi
- Vi **implements the coverage** defined by Eddie in her testbench in order to create thorough and well-architected coverage

# How might we **activate** the users through **collaboration**?

## Pain points

- There is no central repository for proper collaboration

## To-be scenario

- All past tooling and features are integrated into **1 collaborative-centric platform**
- The experience and the views on this platform are **standardized** for easier access by both personas

# Design a prototype

Observe

Reflect

Make



# Overview

To-be scenario: All past tooling and features are integrated into 1 collaborative-centric platform

- Implemented with a **standardized design system**
- The user can see important metadata in order to provide the necessary context of the event
- Advanced filtering

IBM Functional Coverage

Overview

UVM Coverage

Discrete Events

Cross-product Coverage

Hierarchy1 / Hierarchy1 / UVM Coverage /

UVM Coverage

All coverageMy coverageNot implementedBugNo hitsLow hitsZeros everywhereAged out

Search input text

Name

Tags

Implementation status

Assignee

UNIT

▼

[cpoint1](#)

CORE +2

Implemented

@jamie.lai

0/1 NH

▼

[cpoint2](#)

CORE

Implemented

@jamie.lai

8 / 13

▼

[a\\_very\\_long\\_name](#)

ALU

Implemented

@jamie.lai

12/13

▼

cpoint3

ALU

Bug fix

@jamie.lai

8 / 13

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[cpoint4](#)

ALU

Bug fix

@jamie.lai

22/33

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cor\_cos\_fkt\_1948

ALU

Not implemented

@jamie.lai

4 / 21

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[cpoint5](#)

ILU

Bug fix

@jamie.lai

12/13

▼

[cpoint6](#)

ILU

Implemented

@jamie.lai

22/33

▼

[aid\\_sid\\_core\\_new\\_13](#)

ILU

Implemented

@jamie.lai

Waived

▼

cpoint7

ILU

Not implemented

@jamie.lai

22/33

# Coverage details

To-be scenario: Eddie provides the details of the coverage space and the expected results to Vi

- A new “more info” page gives more detailed info about the coverage point
- This is where Vi would find information about coverage, fleshed out by Eddie
- History/log of events and comments can be found here

IBM Functional Coverage

Overview  
UVM Coverage  
Discrete Events  
Cross-product Coverage

UVM Hierarchy3 / Hierarchy2 / Hierarchy1 / UVM coverage / cpoint1 / cpoint1

tag1 tag2 tag3

### Coverage information

Description

Lorem ipsum dolor sit amet, consectetur adipiscing elit, sed do eiusmod tempor incididunt ut labore et dolore magna aliqua.

Coverage intent

Lorem ipsum dolor sit amet, consectetur adipiscing elit, sed do eiusmod tempor incididunt ut labore et dolore magna aliqua. Ut enim ad minim veniam, quis nostrud exercitation ullamco laboris nisi ut aliquip ex ea commodo consequat. Duis aute irure dolor in reprehenderit in voluptate velit esse cillum dolore eu fugiat nulla pariatur. Excepteur sint occaecat cupidatat non proident, sunt in culpa qui officia deserunt mollit anim id est laborum.

How to hit

Lorem ipsum dolor sit amet, consectetur adipiscing elit, sed do eiusmod tempor incididunt ut labore et dolore magna aliqua. Ut enim ad minim veniam, quis nostrud exercitation ullamco laboris nisi ut aliquip ex ea commodo consequat.

Assignee  
jamie.lai

Author  
bruce.lee

User status  
Deferred Set status

### Bins

Search input text

|                          | Bin name | Status      | Header    | Header   | Header   | Header   | Header   | Header   |
|--------------------------|----------|-------------|-----------|----------|----------|----------|----------|----------|
| <input type="checkbox"/> | bin1     | Deferred    | In review | Add text | Add text | Add text | Add text | Add text |
| <input type="checkbox"/> | bin2     | Hard to hit |           | Add text | Add text | Add text | Add text | Add text |
| <input type="checkbox"/> | bin3     | Waived      |           | Add text | Add text | Add text | Add text | Add text |

### Coverage log

jamie.lai commented 8 days ago

I need someone to take a look at this @maya.eapen

# Request Coverage

To-be scenario: Eddie defines the events without implementation, along with the scope of the stories

- Eddie is able to request coverage and give a detailed blueprint of how it should be implemented
- Vi will take this blueprint to implement coverage into her testbench

IBM Functional Coverage

Overview UVM Hierarchy3 / Hierarchy2 / Hierarchy1 / UVM coverage / cpoint1 /

UVM Discr Cross

## Create coverage

Description goes here

- Coverage type
- Coverage information
- Implementation guideline
- Assignees

### Coverage information

Point name

Example: core\_new\_idea

Helper text

Event intent

This coverage should...

How to hit

The coverage can be hit by...

Code templates

Choose an option

Comments

Text area

Cancel Cancel Next

# Enabling Collaboration using Python

- Python is a common language
- Open Source Development
- System Verilog Constructs well proven over years

```
@vsc.covergroup
class my_weak_pht_cnt_cg(object):
    def __init__(self):
        self.with_sample(
            a = uint8_t(5)
            b = uint8_t(5)
        )
    self.cp1 = vsc.coverpoint(self.a, bins=dict(
        A = vsc.bin_array([],1,2,3,4)),
        illegal_bins=dict(
            illegal_Val = vsc.bin(5)
        )
    )
    self.cp2 = vsc.coverpoint(self.b, bins=dict(
        A = vsc.bin_array([],5,31))
    )
    self.cp1x2 = vsc.cross([self.cp1, self.cp2])
```



Credits to Matt Balance' PyVSC library:  
<https://pyvsc.readthedocs.io/en/latest/introduction.html>



# Implement a e2e prototype

Observe

Reflect

Make



# Develop an end-2-end prototype in 2 weeks

The screenshot shows the 'Create coverage' form in the cgotb application. The form is titled 'Create coverage' and has a subtitle 'Coverage profile'. It contains several sections: 'Coverage information' with a 'Name' field, 'Description' field, and 'Tags' field; 'Test results' with a 'Test results' field; and 'Test results' with a 'Test results' field. The form is divided into three tabs: 'Coverage information', 'Test results', and 'Test results'. The 'Coverage information' tab is currently selected.

Define



Implement



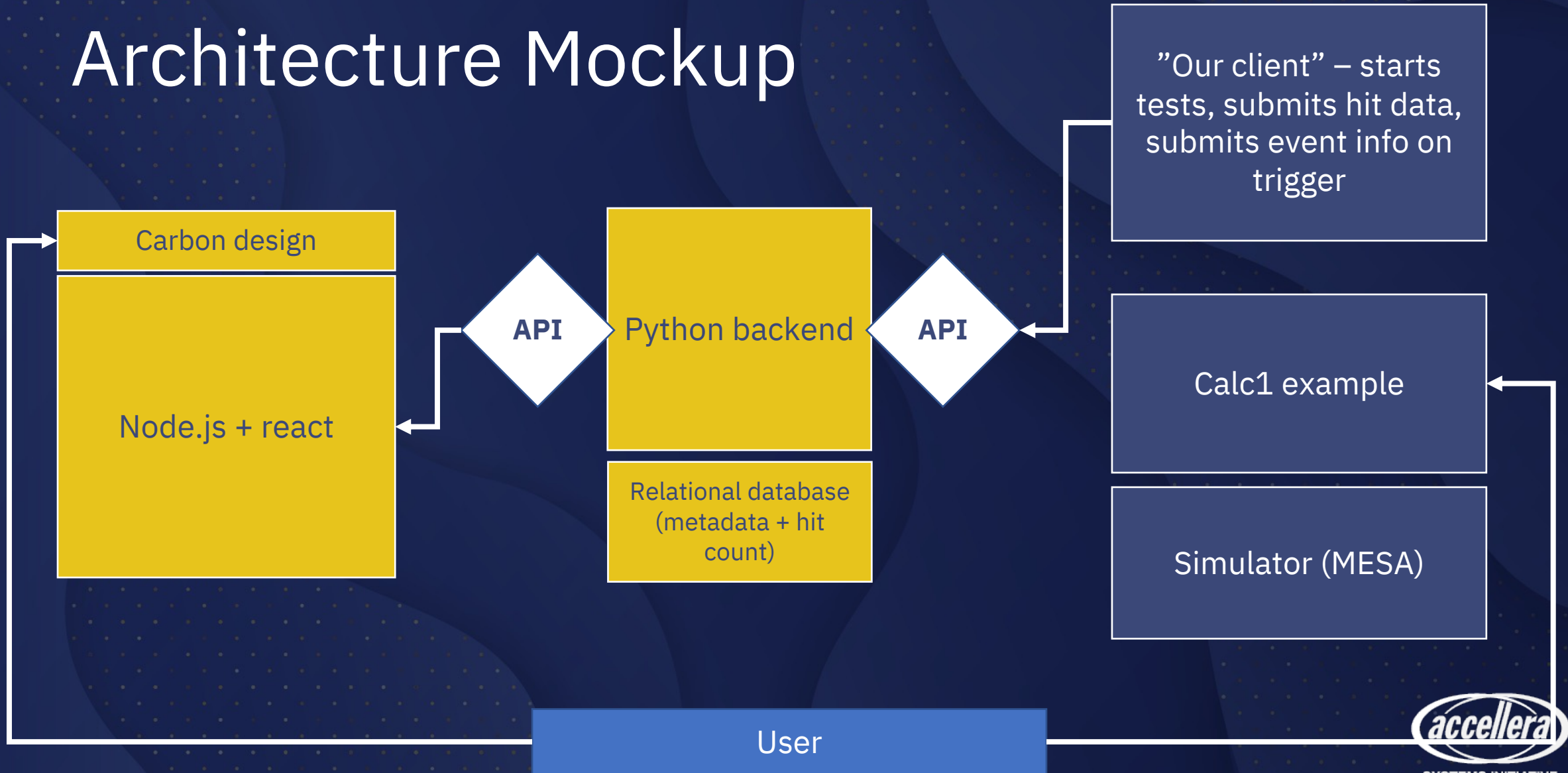
Collect

The screenshot shows the 'Coverage information' page in the cgotb application. The page is titled 'Coverage information' and has a subtitle 'Coverage profile'. It contains several sections: 'Coverage information' with a 'Name' field, 'Description' field, and 'Tags' field; 'Test results' with a 'Test results' field; and 'Test results' with a 'Test results' field. The page is divided into three tabs: 'Coverage information', 'Test results', and 'Test results'. The 'Coverage information' tab is currently selected.

| File name | Status | Header | Header | Header | Header | Header | Header |
|-----------|--------|--------|--------|--------|--------|--------|--------|
| 100       | 100%   | 100%   | 100%   | 100%   | 100%   | 100%   | 100%   |
| 100       | 100%   | 100%   | 100%   | 100%   | 100%   | 100%   | 100%   |
| 100       | 100%   | 100%   | 100%   | 100%   | 100%   | 100%   | 100%   |

Analyze

# Architecture Mockup



# Summary

## Enterprise Design Thinking is key

- ✓ With the user in the loop

## UX design is key to

- ✓ Deeply understand the developers' needs
- ✓ taking a holistic view at the process
- ✓ fast prototyping
- ✓ Drive usability testing

# Conclusions

- ✓ UX design and Prototyping allow fast iterations
- ✓ Can change the way how we work!
  - better
  - better together
- ✓ Allows the developer to take full advantage of the available technology
- ✓ Can significantly improve the overall development effort and schedule

# Questions?



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