UVM mixed signal extensions
Sharing Best Practice and Standardization Ideas

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2018 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

Agenda

- Introduction - 5 min
- UVM Mixed Signal Verification Experience Sharing sessions:
  - UVM-MS mixed signal extensions – 30 min
    - Joen Westendorp, NXP Semiconductors
  - A-UVM — A Transaction-Oriented UVM-Based Library for Verification of Analog Behavior – 30 min
    - Sebastian Simon, Infineon Technologies AG
- General discussion on outcome – 25 min

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Introduction

UVM is a SystemVerilog base class library that standardizes common functions like testbench class structure, testbench component communication and data automation features, like packaging, copy compare, debug

- 2009 Accellera voted to establish UVM standard based on OVM2.1.1 developed by Cadence Design Systems and Mentor Graphics.
- 2011 Accellera approved the 1.0 version of UVM
- 2014 Accellera released version 1.2 of UVM
- 2017 IEEE release of UVM LRM as IEEE 1800.2-2017

Introduction

- Goal of this tutorial
  - Show current best practices used by different companies
    - focus on advantages of practice
    - disadvantages/workarounds/future plans, best in light missing STDs/EDA tools
  - Discuss audience experience in AMS verification with UVM
  - Discuss if creation of an UVM-AMS Accellera working group is something that would be supported by the audience

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UVM-MS
mixed signal extensions

Joen Westendorp, NXP Semiconductors

Contents

- Introduction
- Layers of a verification environment
- Rationale
- UVM Mixed signal
- The analog mixed signal Verification Component
- Mixed signal UVC
- Required definitions
- Questions

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Introduction

- Mixed signal integration verification is about functional verification of analog and digital circuits together.
- Digital only verification is much more developed and methodical than analog verification
- Functional verification of mixed signal circuits is biased to use digital verification methodologies, like UVM
- UVM provides a structured and layered verification methodology, however UVM is not the only existing verification methodology
  - The UVM layers are not defined to deal with analog signals
- This is about **extending** digital verification environments into the AMS domain, to enable MS verification instead of simulation (use UVC's).

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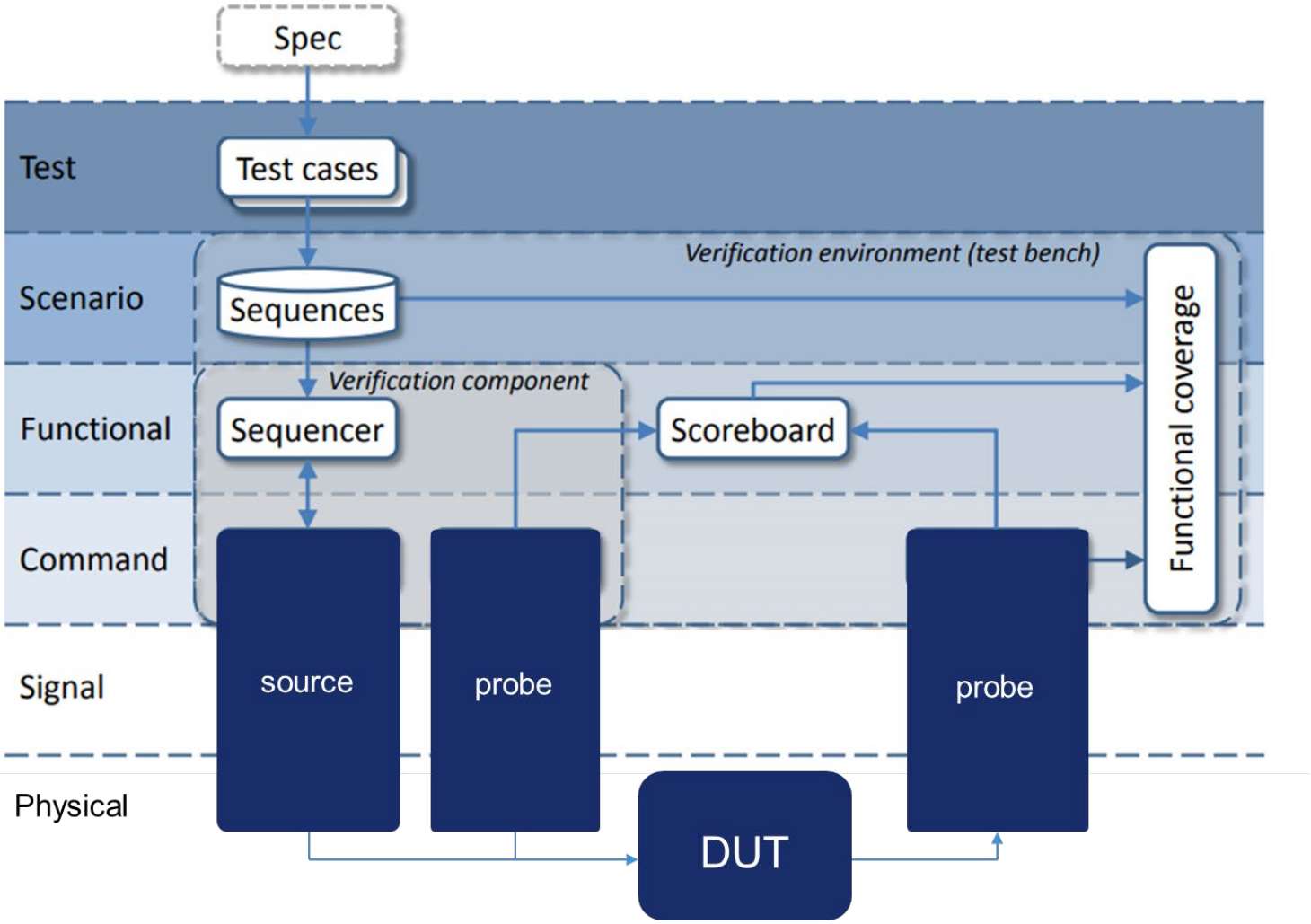
VE Layers



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Rationale

- Extendibility
  - New functionality can be added without changing existing functionality, a new component can be created by deriving it from an existing one
- Maintainability
  - The architecture is modular and everything is in a logic place, later changes will not affect already existing use models
- Configurability
  - Functionality can be selected and modified without changing the code, a test bench does not need to be changed when another signal is required

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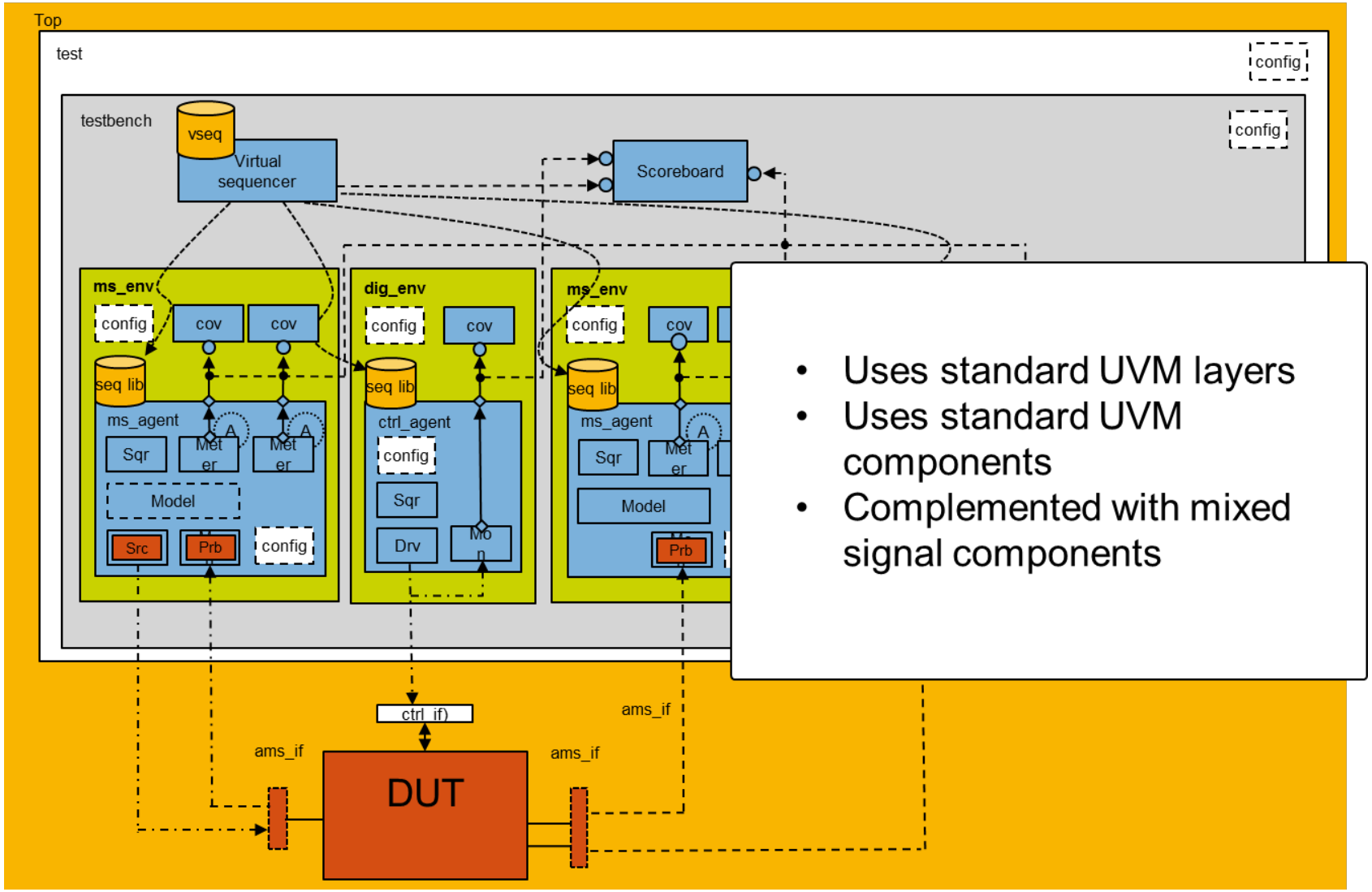
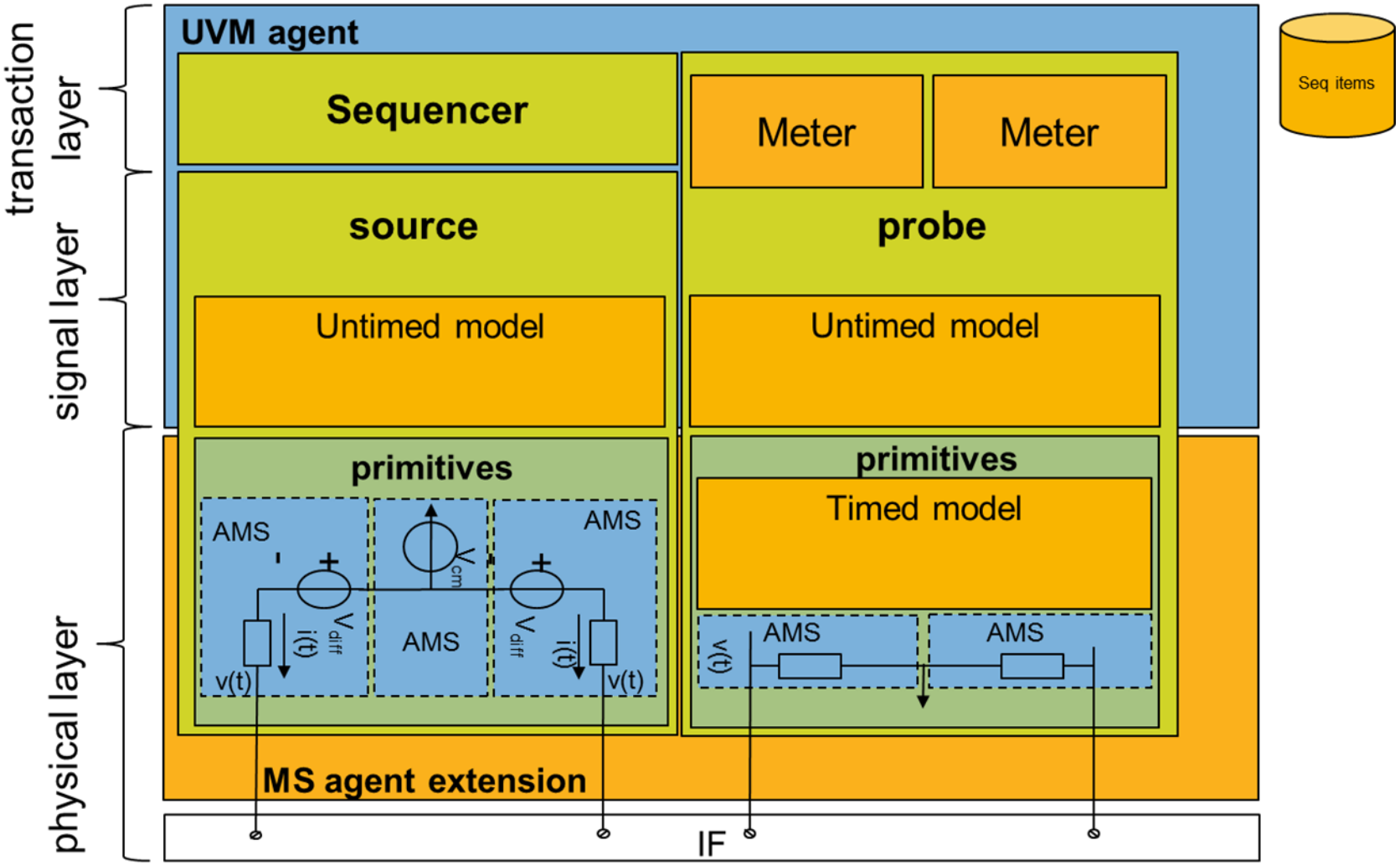
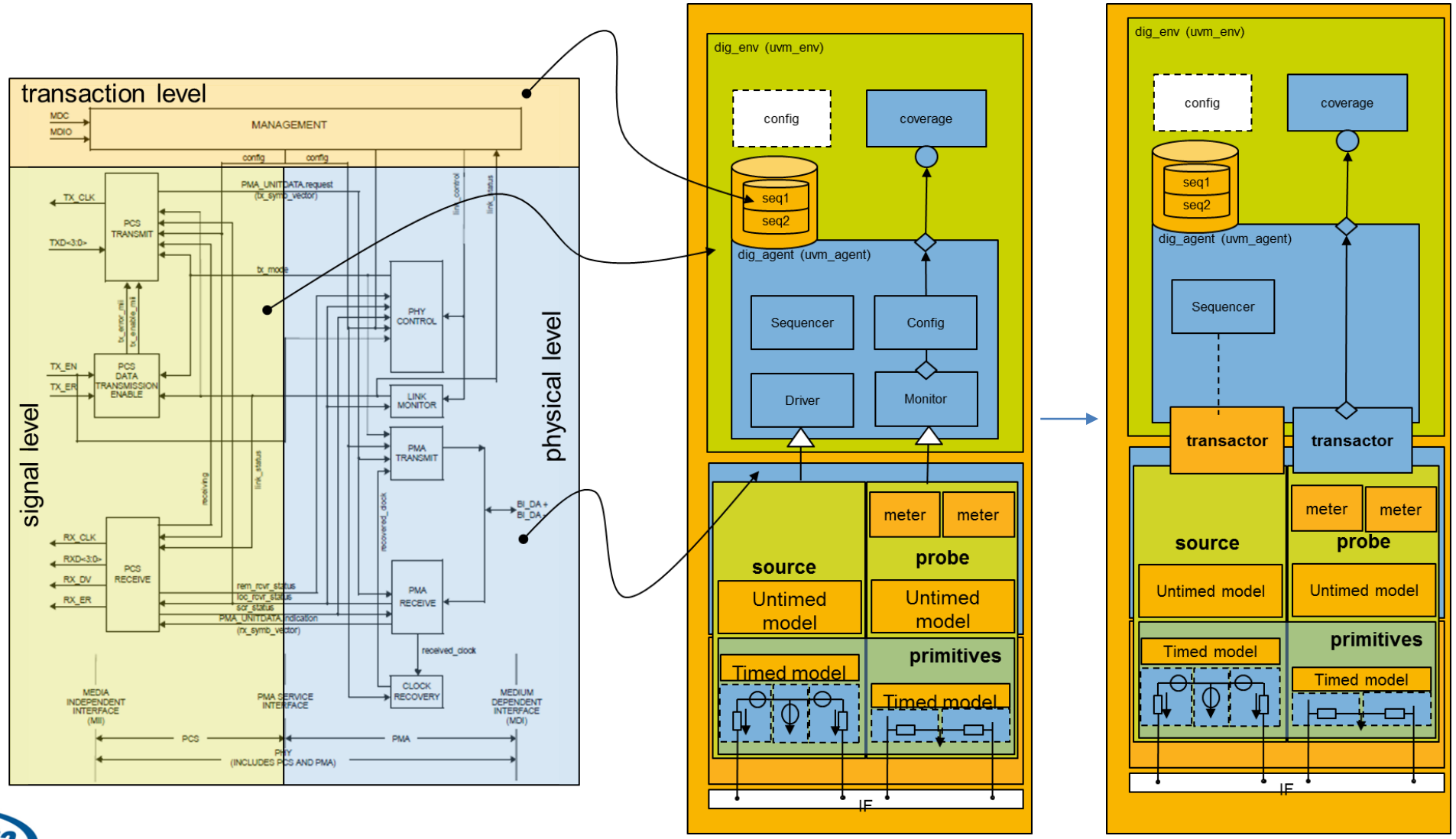
UVM-Mixed Signal



AMS Verification component



Mixes signal UVC



Advantages of Approach

- TBA

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Disadvantages/Workarounds/Future Plans
Definitions required

- Addition mixed signal verification components
  - Meters
  - Models
  - Primitives
  - Transactors
- Structure
  - Agent
  - Agent extension
- Interfaces between layers
  - Translation from transaction level to the signal layer is well defined through sequences
  - Definition of flexible API's between the physical and signal level layer still needed (also a common interface to connect to 3rd party VIP)

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Questions

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A-UVM — A Transaction-Oriented UVM-Based Library for Verification of Analog Behavior

Sebastian Simon
Infineon Technologies AG

Outline

1. Motivation
2. A-UVM: Analog extension to UVM
3. Application: IGBT driver
4. Summary

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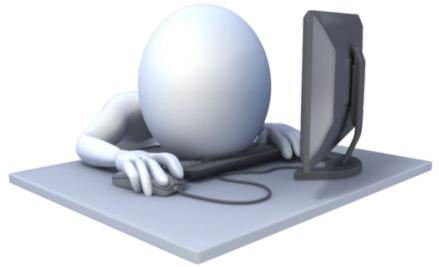
Traditional Analog/Mixed-signal Verification

- Mixed-signal top-level verification means …
  - … confirming functional correctness with respect to the specification
  - … analysing waveforms in the time domain

- Traditional analog verification approach has a couple of **limitations**:
  - Directed testing → Critical scenarios might be left out
  - No metrics for functional coverage → Are we done?
  - Waveforms are often manually inspected → Has to be repeated after each regression



→ Error-prone, inefficient and time-consuming!

→ **We need automation and reusability!**

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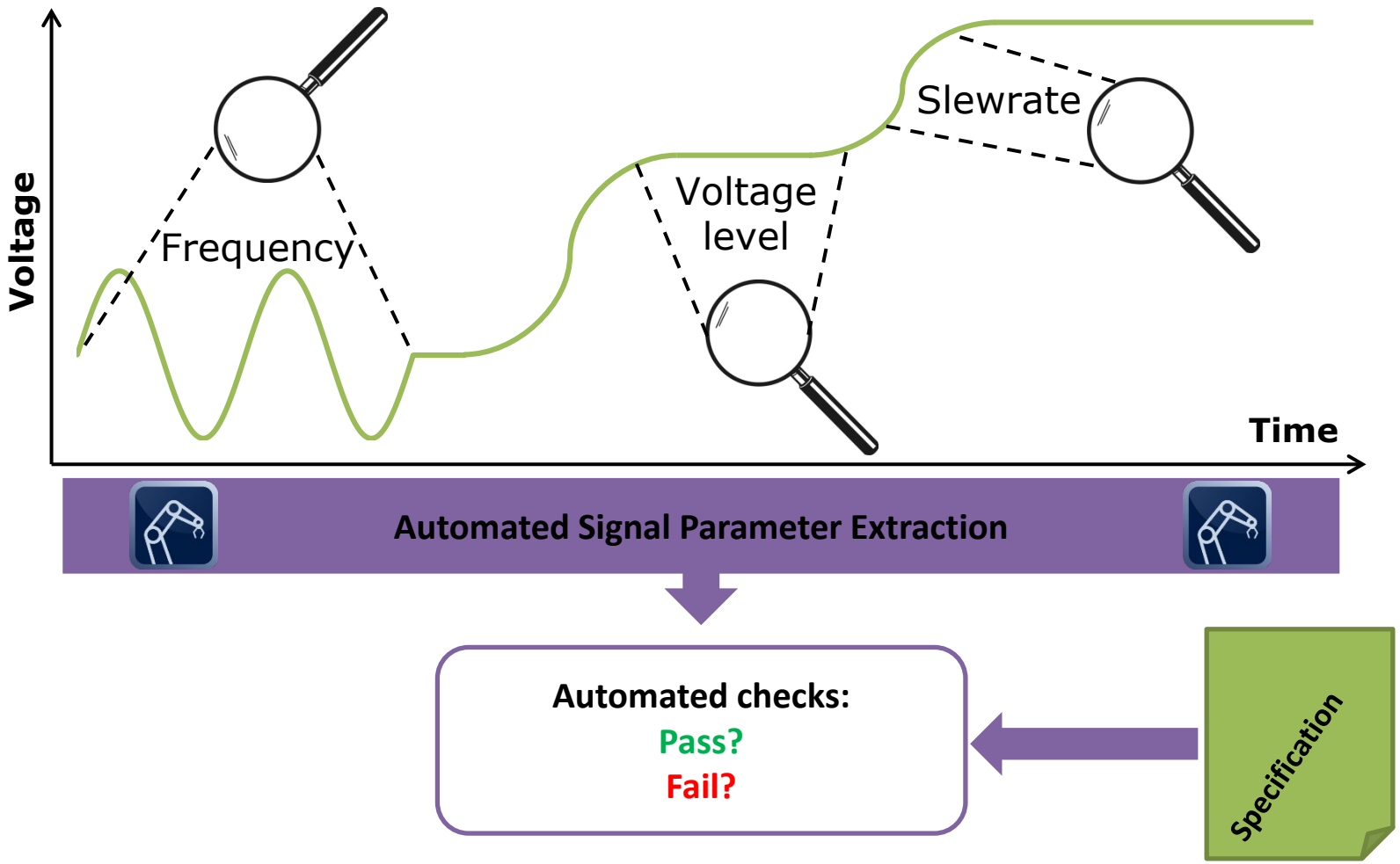
Automation in the Analog Domain



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Outline

1. Motivation
2. **A-UVM: Analog extension to UVM**
3. Application: IGBT driver
4. Conclusion

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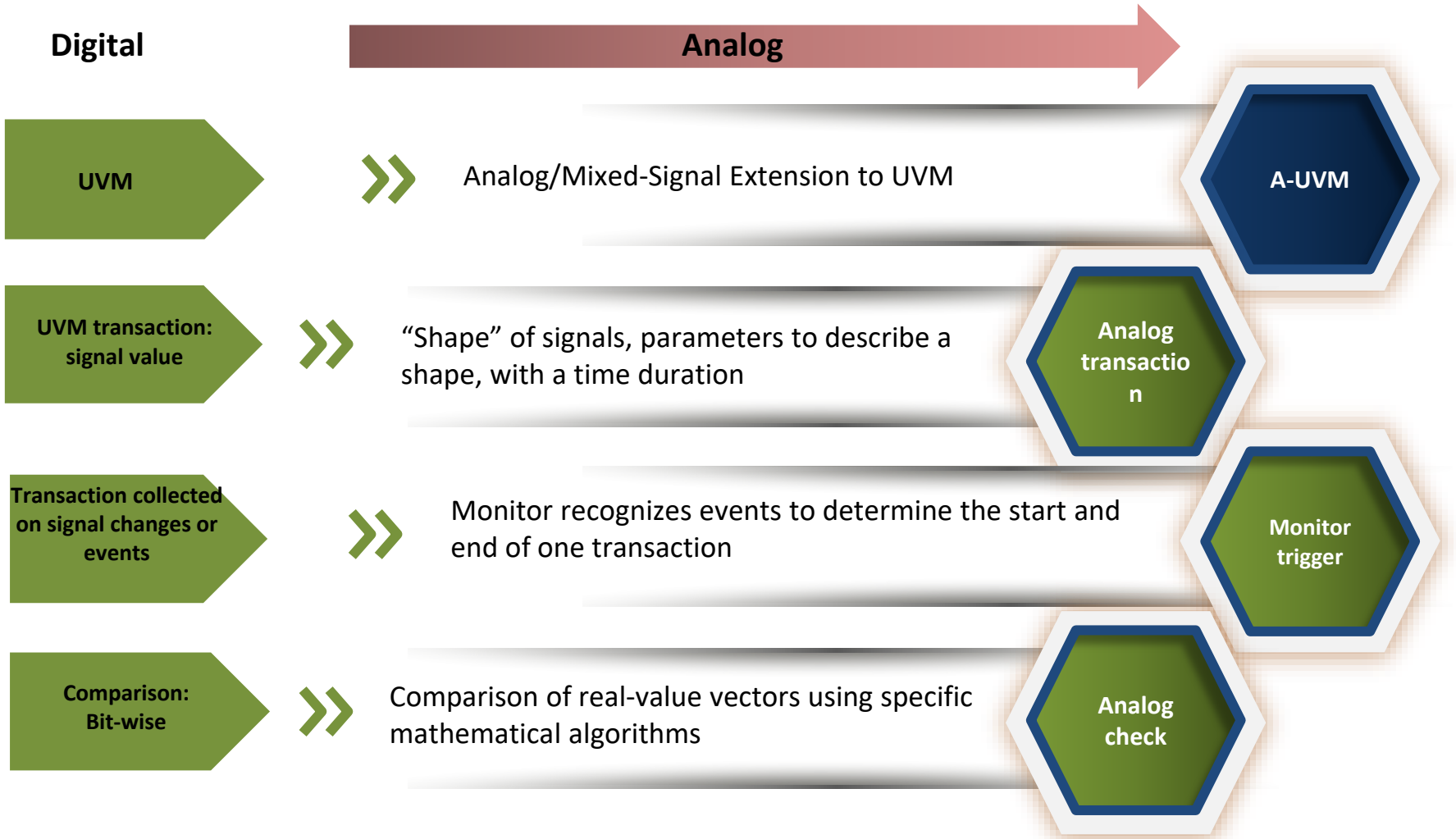
A-UVM (Analog-UVM)



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A-UVM: Transaction

UVM Transaction

```
Input_a =1'b1;
Input_b =1'b0;
```

A-UVM Transaction

```
Name: sine
Freq: 200kHz
Ampl: 5V
Dur: 5us
Phase: 10°
```

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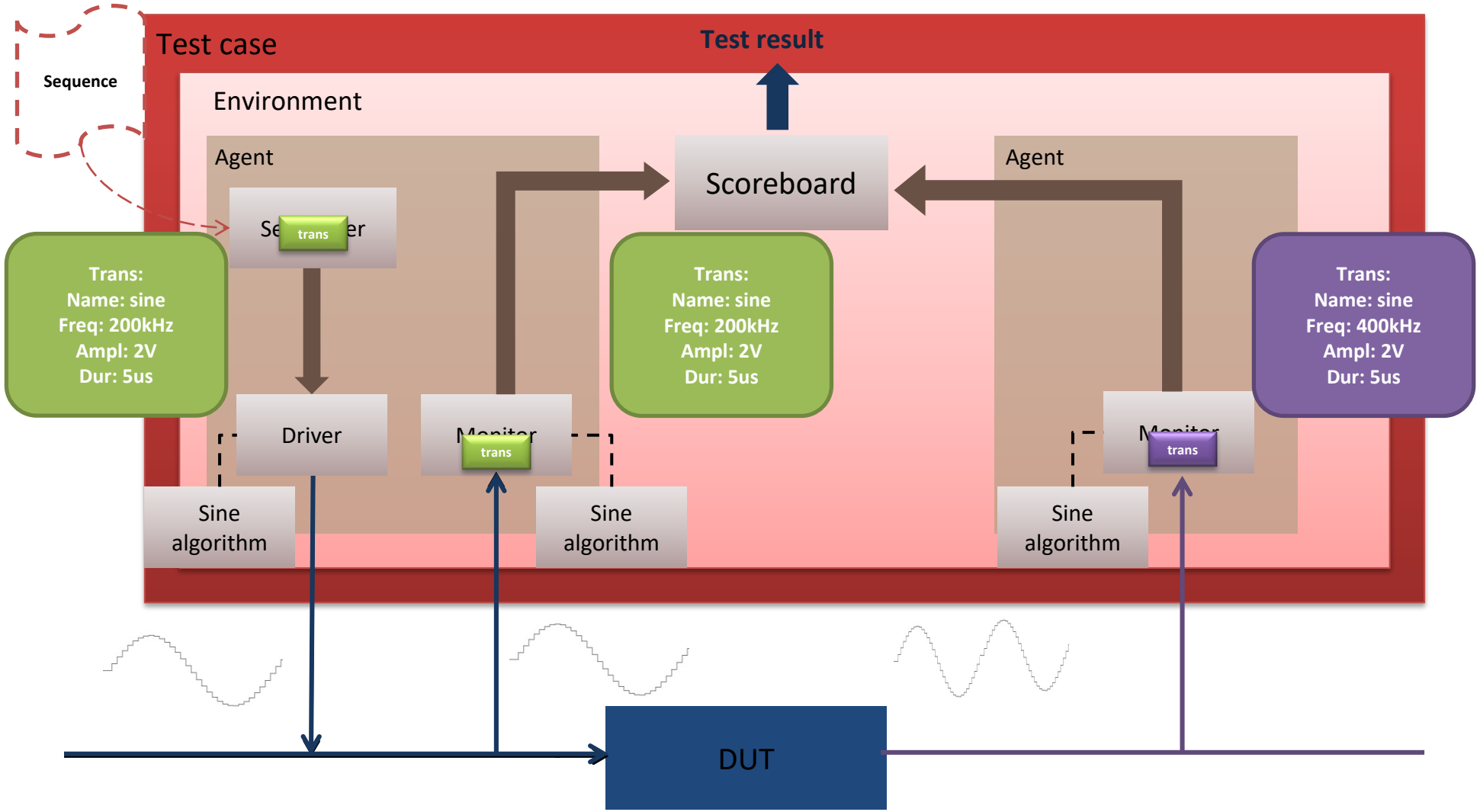
A-UVM (Analog-UVM)



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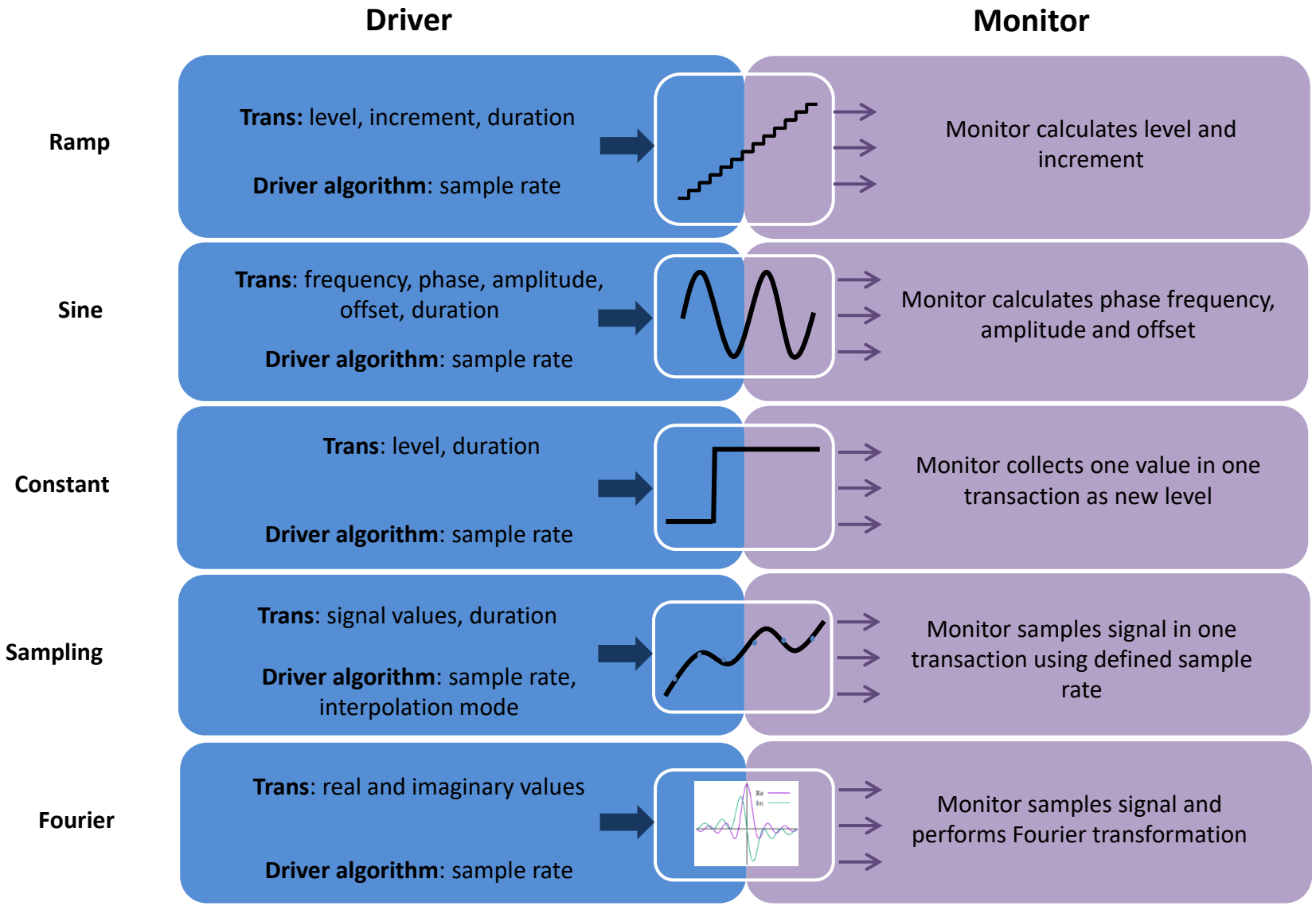
A-UVM: Driver & Monitor Algorithms



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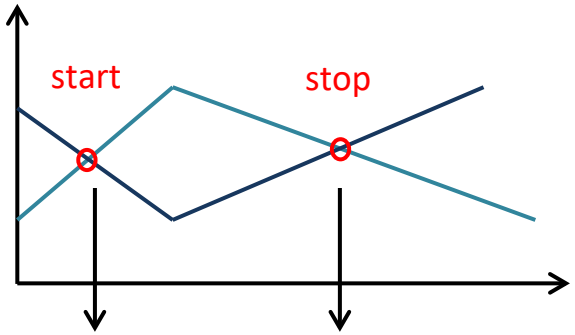
A-UVM: Trigger Mechanism

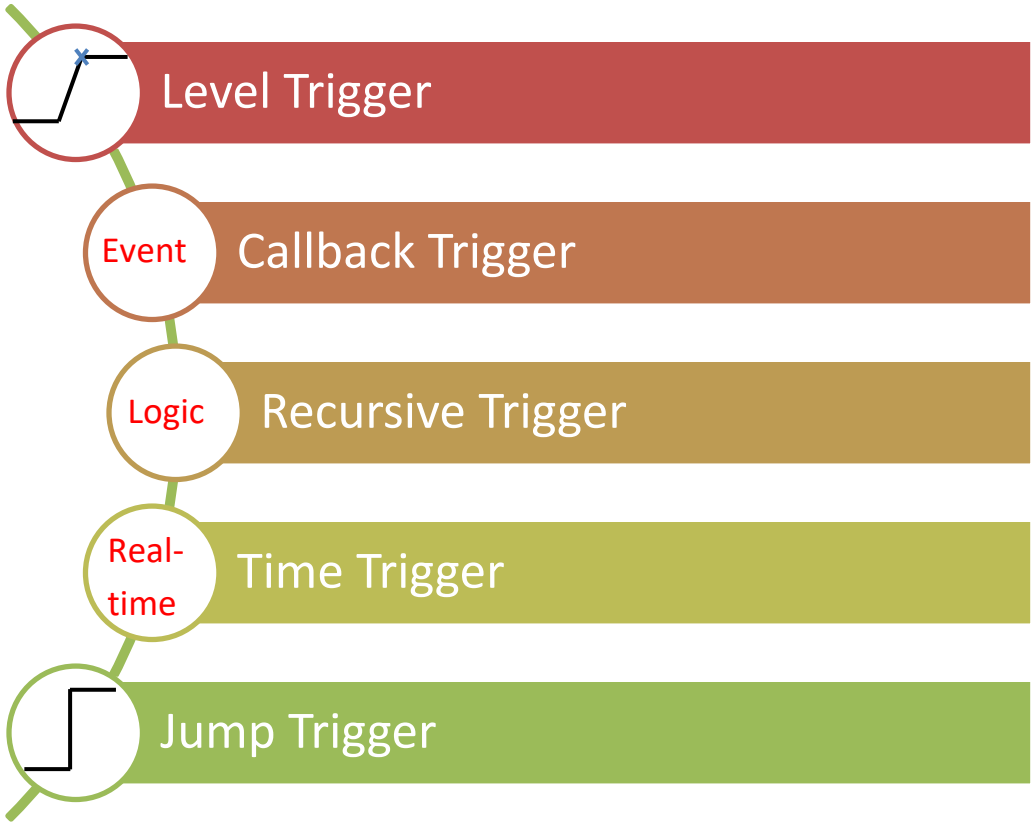
Start Trigger

Stop Trigger

Cancel Trigger

Example: using crossing of two signals as trigger condition





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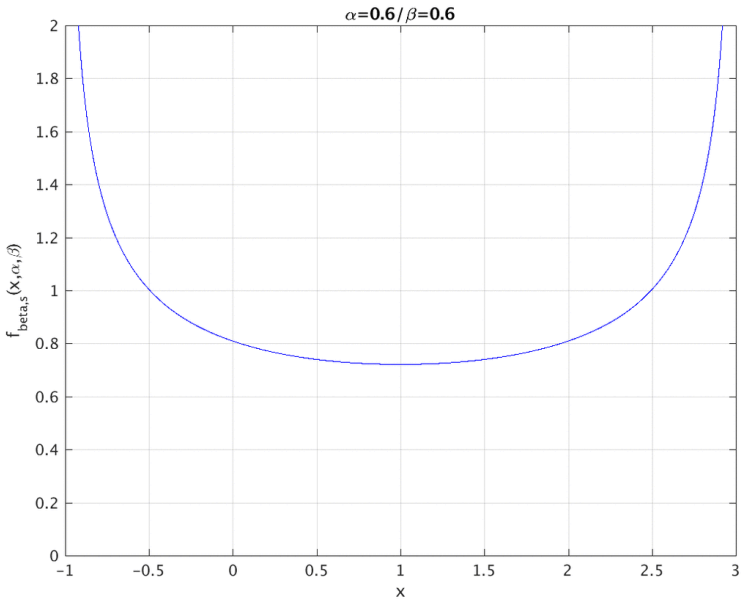
A-UVM: Stimulus generation

Analog Constrained Random Stimulus

- Signal features can randomized based on distributions
  - Uniform distribution
  - Gaussian distribution
  - Beta distribution

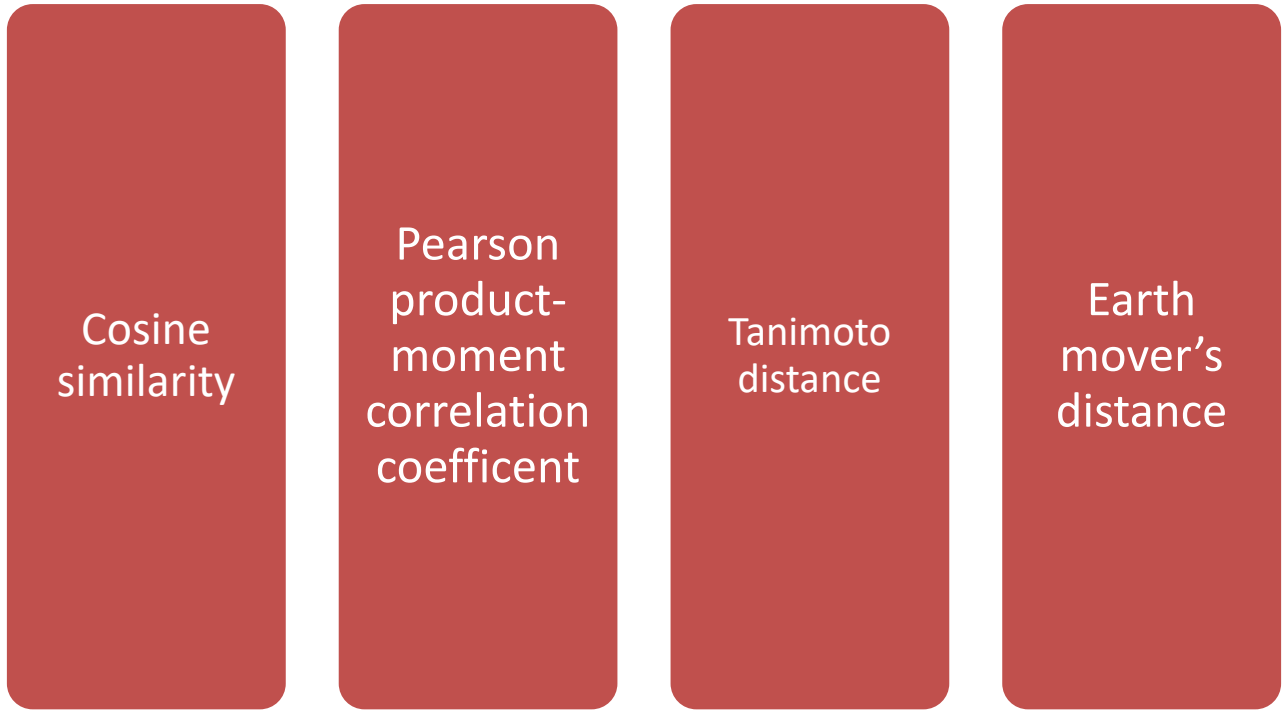
$$f_{\text{beta}}(x,\alpha,\beta) = \begin{cases} \frac{\Gamma(\alpha+\beta)}{\Gamma(\alpha)\Gamma(\beta)} \cdot \frac{x^{\alpha-1}}{(1-x)^{1-\beta}} & x \in (0,1) \\ 0 & \text{otherwise} \end{cases}$$

Beta distribution can be used for constrained-random stimulus:



- Symmetric vs. asymmetric
- Unimodal vs. bimodal
- Concave vs. convex

A-UVM: Comparison of Analog Signals



- Comparison of analog waveforms can be performed using different metrics
- Provides real value between 0.0 and 1.0 representing degree of similarity
- Waveform checks assume lower limit for similarity result → pass/fail

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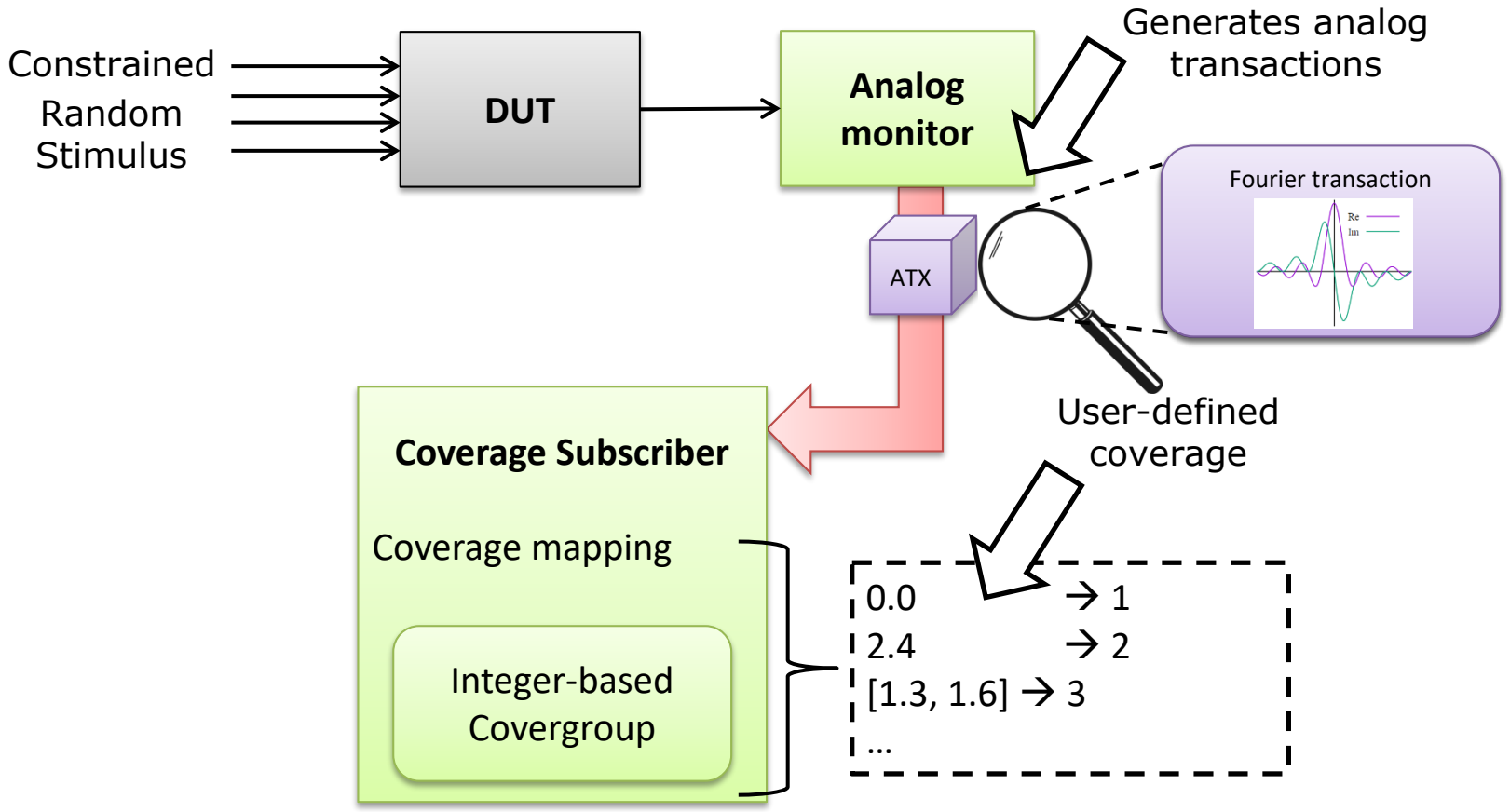
A-UVM: Analog Coverage Collection

- Basic concept of analog coverage collection:



A-UVM: Other Features

Sanity check: is applied on the interface to check whether signals exceed a allowed value

Plotter/scanner: stores/reads signal information in/from separate files

More user/project-specific features can be added

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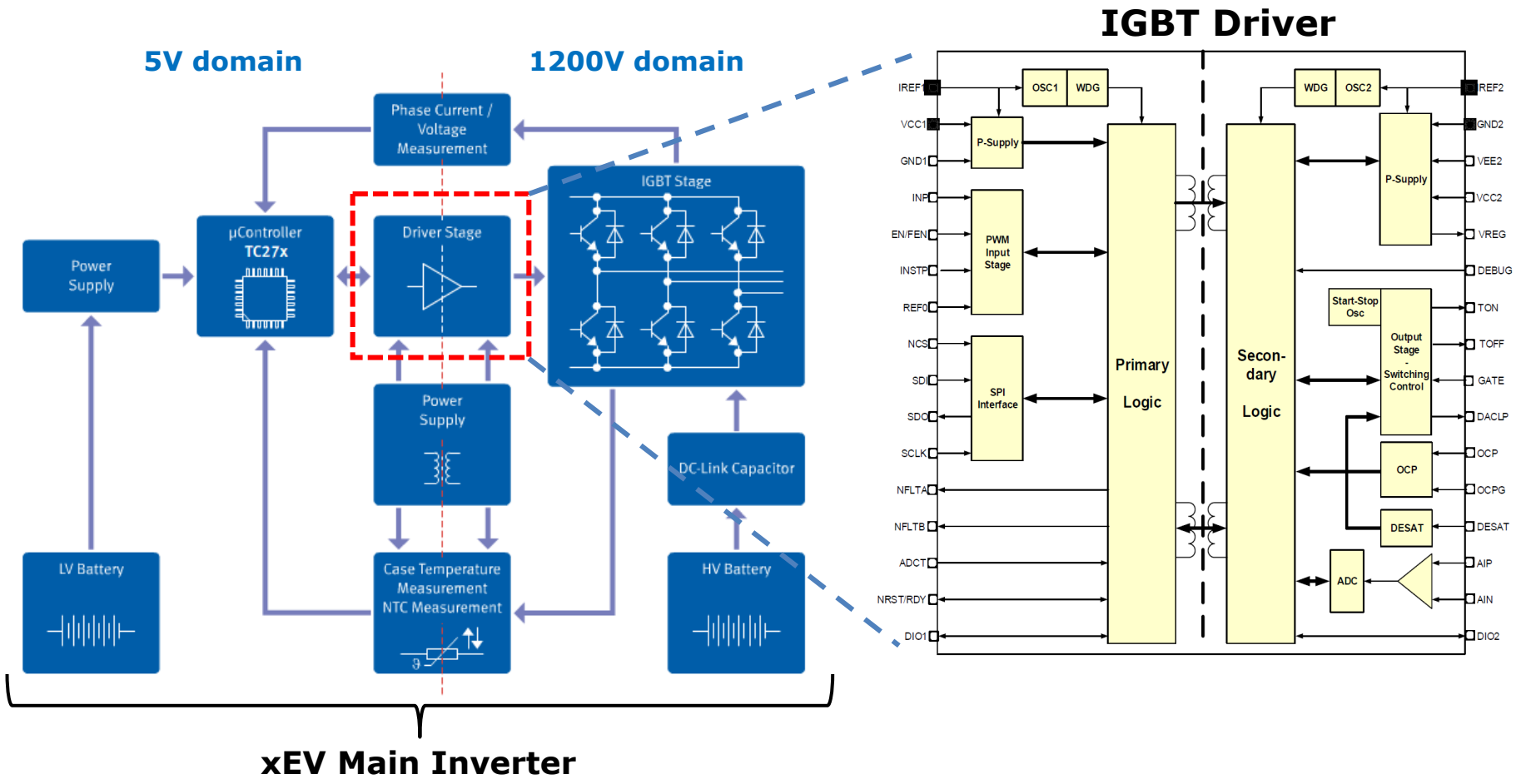
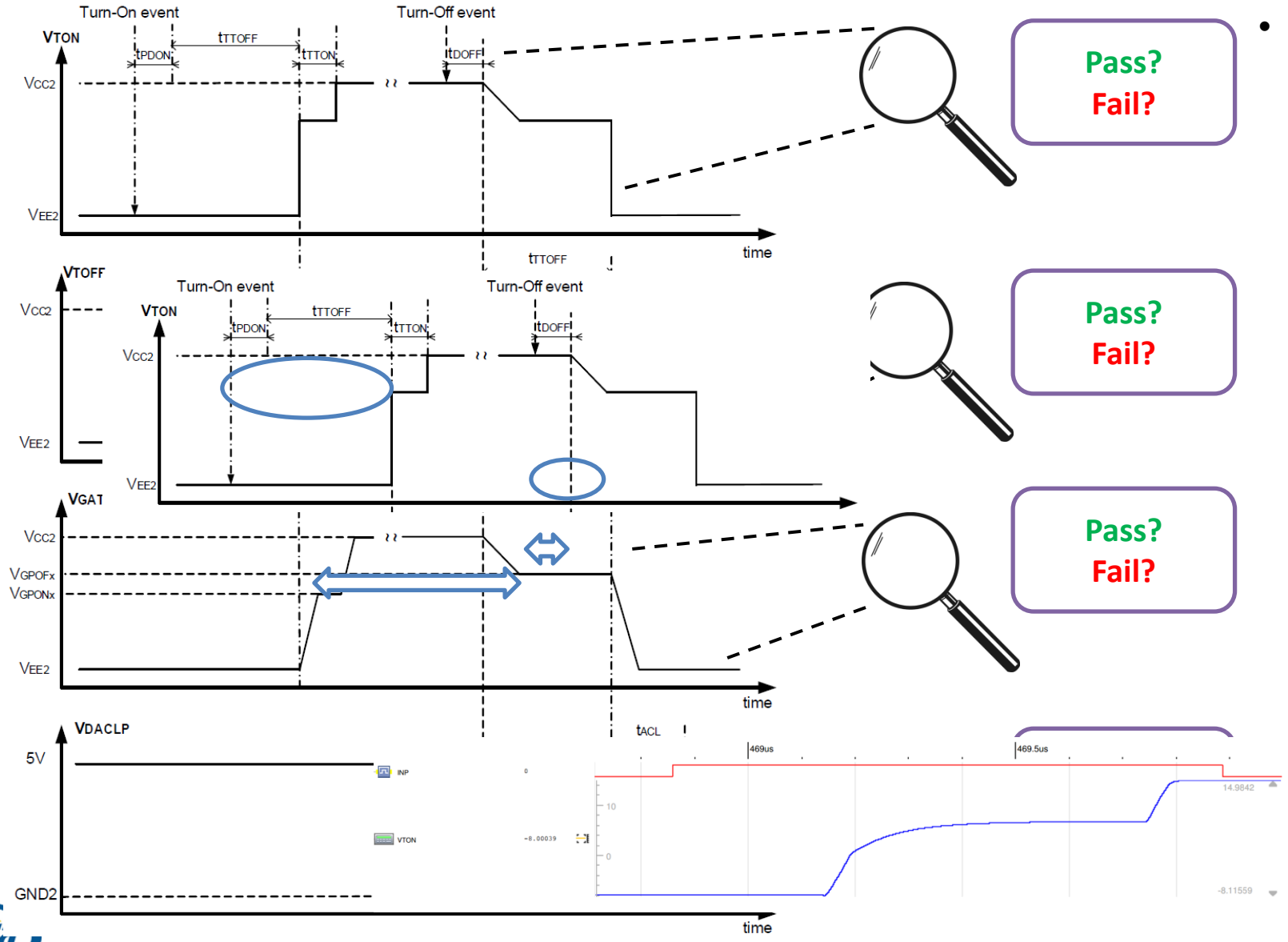
Application: IGBT Gate Driver

- High-voltage IGBT gate driver designed for motor drives above 5kW (e.g. xEV)
- On-chip galvanic insulation via coreless transformer



Application: Specification

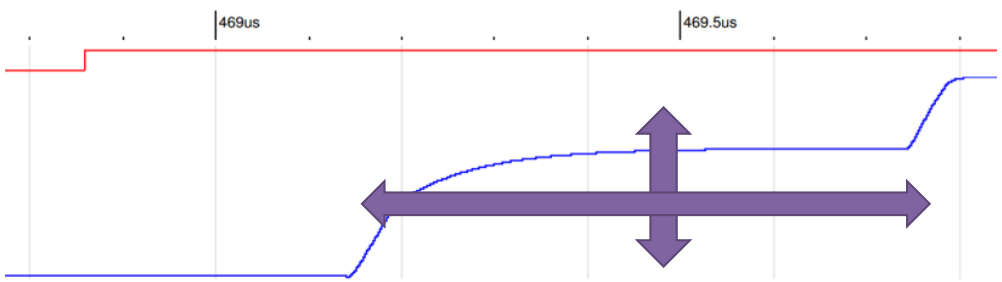


- Extracting signal features for two-level turn-on
  - Start-trigger for monitoring: posedge of digital input signal
  - Algorithm to extract time and voltage parameters based on stable level regions
  - Stop-trigger for monitoring: VCC2 level is reached

› Two-level turn-on during simulation:

Application: Configurations

- Why spending so much effort on automated feature extraction and automated checking?
  - Plateau level and plateau length can be configured via SPI in register fields



  - Possible configurations just for turn-on: 7·246 = 1722
  - Narrowed down to interesting scenarios (e.g. extreme cfgs):
    - 42 conf's · 5 seeds · 5 turn-on events/conf/seed = **1050 turn-on waveforms** (to be checked after each regression)
    - Not realizable without automated extraction and checking!

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Advantages of Approach

A-UVM Features	Available?
Analog (real-valued) transactions	✓
Driving analog constrained-random stimulus	✓
Monitoring analog signal features	✓
Automated analog checks with pass/fail criteria	✓
Similarity analysis of analog signal features	✓
Analog Functional Coverage	✓

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Disadvantages/Workarounds/Future Plans

- TBA

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General Discussion on Outcome

- To be filled

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