

USF-based FMEDA-driven Functional Safety Verification

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Outline

- Session 1
 - Introduction
 - Functional Safety Analysis Overview
 - Deep Dive
 - Architectural FMEDA
 - Detailed FMEDA
 - Safety Metrics Verification
- [Break]
- Session 2
 - Fault Campaign Management
- Summary



EDA as an Ecosystem of International and Industry Standards

1800 - IEEE Standard for SystemVerilog Unified Hardware Design, Specification, and Verification Language

1364 - IEEE Standard for Verilog Hardware Description Language

1076 - IEEE Standard for VHDL Language Reference Manual

Library Exchange Format (LEF)/Design Exchange Format (DEF)

1801 - IEEE Standard for Design and Verification of Low-Power, Energy-Aware Electronic Systems

Timing Constraints – SDC

1497 IEEE Standard for Standard Delay Format (SDF) for the Electronic Design Process

Liberty™ library format

GDSII - Graphic Design System
OASIS® – Open Artwork System Interchange Standard

1685 - IEEE Standard for IP-XACT, Standard Structure for Packaging, Integrating, and Reusing IP within Tool Flows

Why not for safety?

Describe safety features, targets (intent) and exchange safety-related information



Motivations & Mission

- Lack of formalism, standards ambiguity, differentiated assessors scenario, lead to customer-specific methodologies + widespread usage of Spreadsheets
 - «consulting-driven» market side-effects:
 - 'keep it obscure'
 - 'this is my (certified) methodology'
 - '(only) We will tell you what you have to do'...etc...

To develop a modular safety analysis platform to exchange safety-related information and to enable Design For Safety with Cadence® Tools



Cadence Approach

- Modularity
 - A solution that can be adapted and scaled to different scenarios
- Defined scope
 - A set of kernel functionalities Rooted by safety analysis capabilies
- Not enforcing a «methodology»
- EDA 'friendly'



Current Status

- Accellera Functional Safety Working Group (FSWG)
 - Second White Paper Published December 2023
 - Cadence was part of the WG formation and kick-off in 2019
 - Being the collaborative work of entities the final Accelera proposal will be different from USF
- IEEE Std 2851[™]- 2023 "Standard for Functional Safety Data Format for Interoperability within the Dependability Lifecycle"
 - "dot standards" will follow
 - IEEE to adopt the Accelera FSWG work on FMEDA

Cadence is committed to adopt and support the IEEE 2851 family of standards

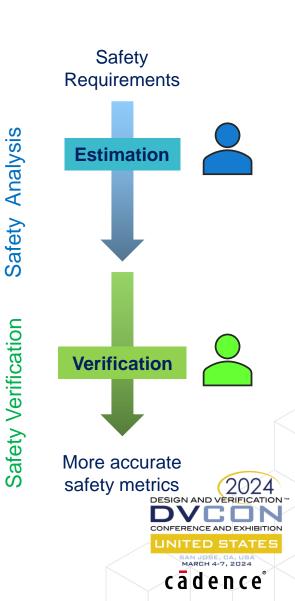
- Where we are going:
 - Safety Analysis: an international standard to share safety information
 - Safety Implementation: adding a new variable to PPA





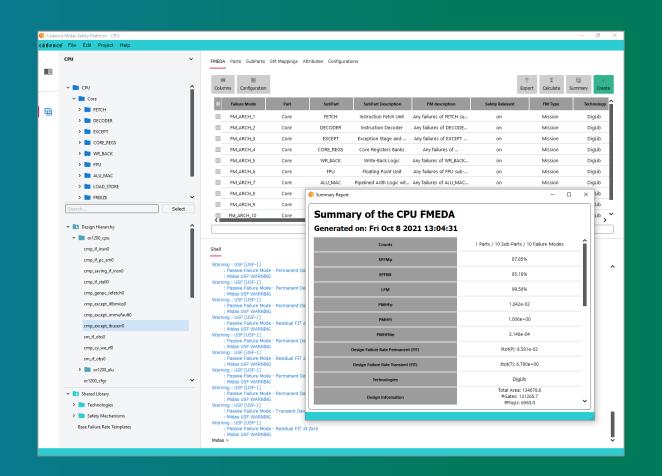
Closing the Gap between FMEDA and Safety Verification

		Abstraction	Safety Step	User
	Functional Safety Concept	Functional	FMEA	Safety Architect (System level)
	Technical Safety Concept SoC	Block Diagram	FMEDA (architectural)	Safety Architect (SoC level)
	SoC Design	RTL/netlist	FMEDA (detailed)	Safety Engineer (RTL/gate level)
	SoC Safety Verification	Netlist	Safety Verification (Formal/Fault Injection)	Safety Verification Engineer
	Safety Metrics	Verification Result	FMEDA backannotation	Safety Verification Engineer



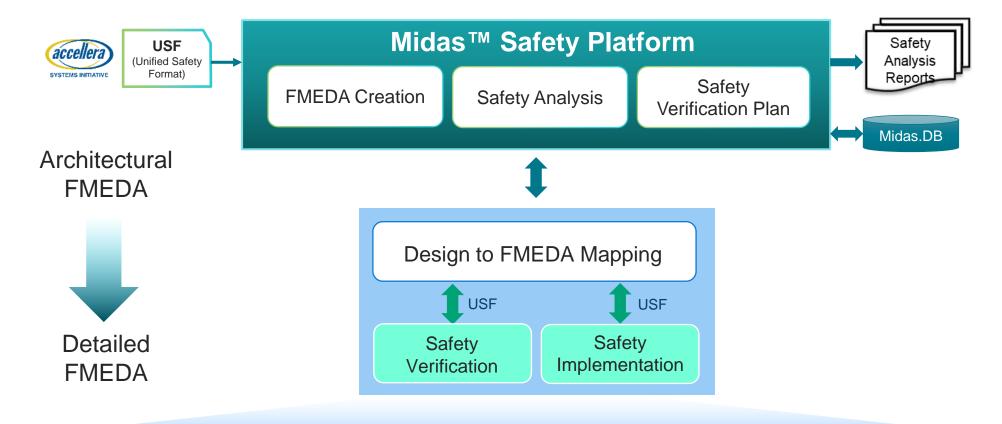
Midas Safety Platform for FMEDA-driven Functional Safety

- Midas[™] Safety Platform driving analog and digital flows for FMEDAbased functional safety
- Early phase safety analysis and architecture exploration
- Automated safety mechanism insertion and verification
- Native chip design data for accuracy and detailed safety analysis
- Unified Safety Format (USF) support





Cadence Functional Safety Full Flow











Digital Safety Verification

Fault campaign management, analysis, simulation and emulation

Fault Campaign Management – Verisium Safety

Unified campaign management across all engines

Backannotation of DC results into Midas FMEDA

Provides requirements traceability and reporting

Fault Analysis – Jasper FSV App

Structural analysis to reduce the fault list

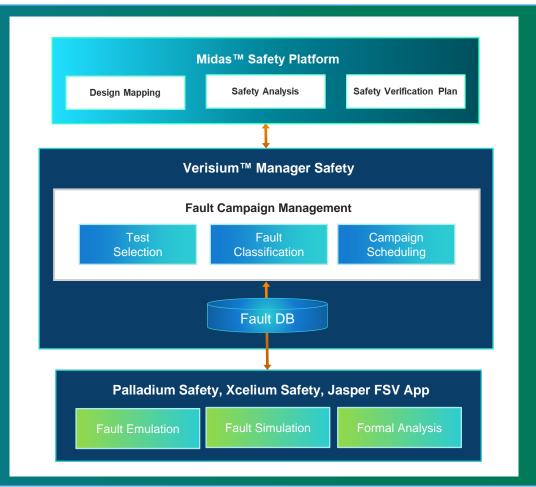
Formal analysis for accurate fault classification

Fault Simulation – Xcelium Safety

Native serial and concurrent fault verification

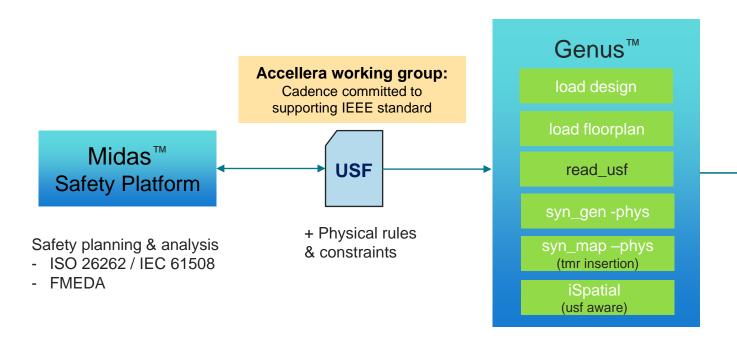
Same simulator for functional verification (GOOD machine) and fault simulation (BAD machine)

Fault Emulation – Palladium Safety Run full SoC with SW or STLs





Cadence Automotive Safety / USF-Driven Flow



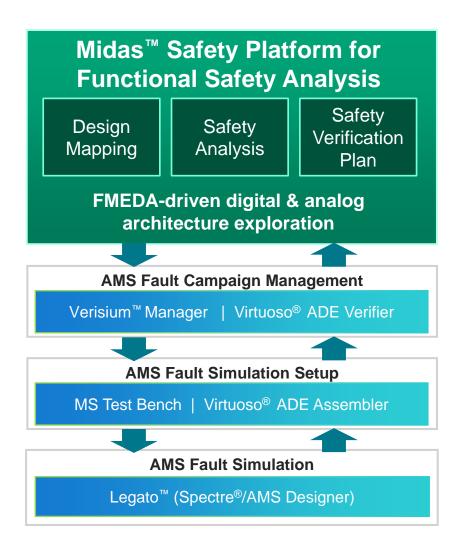
- USF from Midas augmented with physical information (spacing rules, ...)
- USF-driven safety mechanism flow:
 - Insertion in Genus during synthesis
 - Physical implementation & verification (spacing, keepout, ...) in Innovus
 - Logical verification in Conformal







Midas AMS Functional Safety Flow Overview



- Connect FMEDA data to design data
 - Import schematic/RTL hierarchy into Midas (DHE)
 - Direct mapping of Safety objects to Design objects
 - Generate fault campaigns inside Midas for various failure modes
- Clean hand-off from FuSa lead to IC design teams
 - Digital-centric or analog-centric AMS flows
 - Automated fault campaign management: ADE® Verifier and Assembler (analog-centric) or Verisium Manager (digital-centric)
 - Run fault campaigns with Virtuoso, Verisium Manager, and Legato
- Improve the accuracy & traceability of safety metrics
 - Back-annotate key safety metrics back to Midas



Midas Safety Platform Modularity

- The Midas backend is the 'functional safety engine'
 - Support for Midas command line interface
 - ISO26262; IEC61508
 - BFR
- Same backend is integrated into Genus and Innovus
- Core features can be made easily available in different contexts

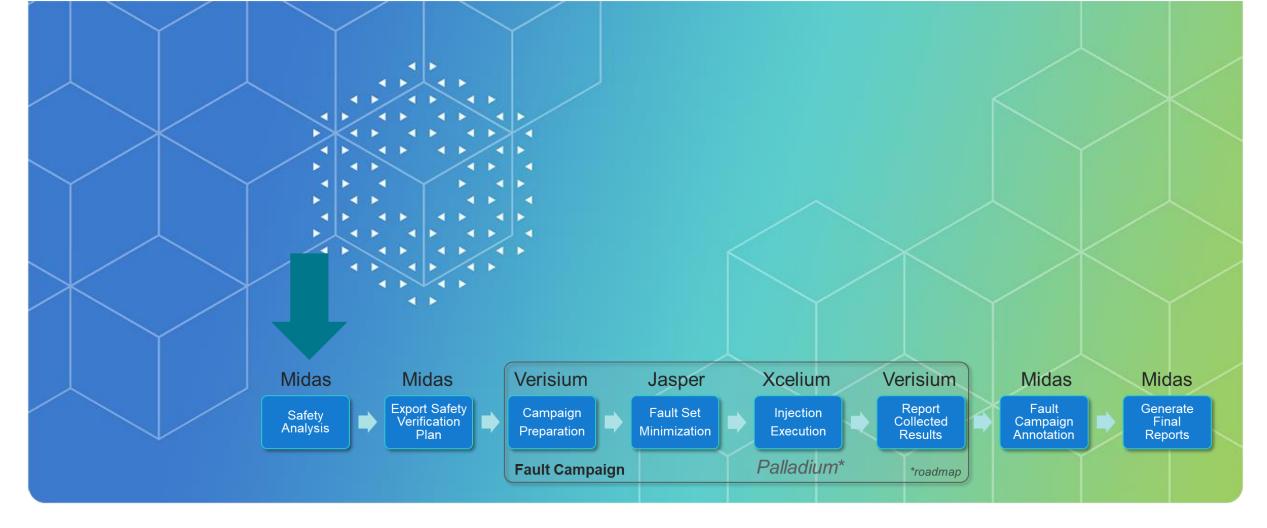
Midas Application



Genus

Innovus





Functional Safety Analysis Overview



Functional Safety Analysis

Architectural FMEDA

- Device Safety (IP/SoC) architectures
- No direct access to design information

Detailed FMEDA



Using real design information

FMEDA Project (IP and SoC)

BFR calculation engine (IEC TR 62380)

Technologies (Digital, Analog, ...)

Safety Hierarchy (Parts/Subparts)

Failure Modes

Mapping Safety Mechanisms

Mapping Safety Hierarchy to Design Hierarchy

Metrics & Reports

Queries

Rules check

IP FMEDA, FMEDAs grouping and SGs definition

DC on FM-SM, different DC heuristics for combining from multiple SM

Only for a detailed FMEDA: direct (with – exclude support) or extraction-based (COI)

Custom attributes, What-if analysis, flexiblecustomizable template

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Architectural FMEDA

USF

FMEDA Project (IP and SoC)

set fmeda myFMEDA -ASIL B -t -p -arch

BFR calculation engine (IEC TR 62380)

Technologies (Digital, Analog, ...)

Safety Hierarchy (Parts/Subparts)

Failure Modes

Mapping Safety Mechanisms

Mapping Safety Hierarchy to Design Hierarchy

Metrics & Reports

Queries

create technology DigLib -type Digital -fitperm 1.07e-6 fittrans gate 1.64e-6 -fitbit 1.64e-6 -refarea 1.026

create part "OpenRISC Core" -fmeda myFMEDA create subpart FETCH -desc "Instruction Fetch Unit" -part "OpenRISC Core" -fmeda myFMEDA

create failure mode FM ARCH 1 -desc "Any failures of FETCH subblock" -type Mission -technology DigLib -subpart FETCH -gates 2500 -flops 100 -safe_perm 1 -safe_trans 0 -fmeda myFMEDA

create safety mechanism SM-IF -desc "Instruction Fetch redundancy" -type Custom -class HW apply safety mechanism SM-IF -to FM ARCH 1 -fmeda myFMEDA dcperm 95 -dctrans 0 -dclat 100

report safety -fmeda myFMEDA permanent html Permanent.html report safety -fmeda myFMEDA transient csv Transient.csv query usf myFMEDA -obj type failure mode -obj id FM ARCH 1

Detailed FMEDA

USF

FMEDA Project (IP and SoC)

set_fmeda myFMEDA -ASIL B -t -p -detailed

BFR calculation engine (IEC TR 62380)

Technologies (Digital, Analog, ...)

Safety Hierarchy (Parts/Subparts)

Failure Modes

Mapping Safety Mechanisms

Mapping Safety Hierarchy to Design Hierarchy

Metrics & Reports

Queries

```
create_technology DigLib -type Digital -fitperm 1.07e-6 -
fittrans_gate 1.64e-6 -fitbit 1.64e-6 -refarea 1.026
```

```
create_part "OpenRISC Core" -fmeda myFMEDA -instances
{hinst:or1200_cpu/or1200_if hinst:or1200_cpu/or1200_genpc}
create_subpart FETCH -desc "Instruction Fetch Unit" -part
"OpenRISC Core" -fmeda myFMEDA -instances
{hinst:or1200_cpu/or1200_if}
```

create_failure_mode FM_ARCH_1 -desc "Any failures of FETCH subblock" -type Mission -technology DigLib -subpart FETCH safe_perm 1 -safe_trans 0 -fmeda myFMEDA -instances {hinst:or1200_cpu/or1200_if}

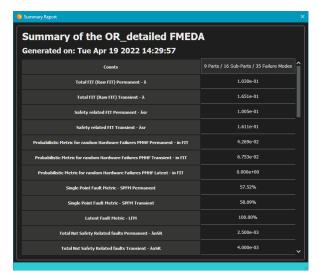
create_safety_mechanism SM-IF -desc "Instruction Fetch
redundancy" -type Custom -class HW
apply_safety_mechanism SM-IF -to FM_ARCH_1 -fmeda myFMEDA dcperm 95 -dctrans 0 -dclat 100

report_safety -fmeda myFMEDA permanent html Permanent.html
report_safety -fmeda myFMEDA transient csv Transient.csv
query_usf myFMEDA -obj_type failure_mode -obj_id FM_ARCH_1



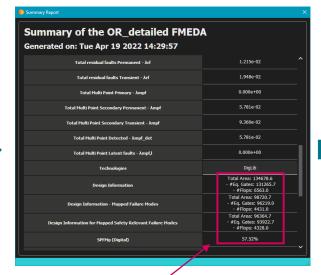
Refine FMEDA Data for Optimized Safety Design

Architectural FMEDA



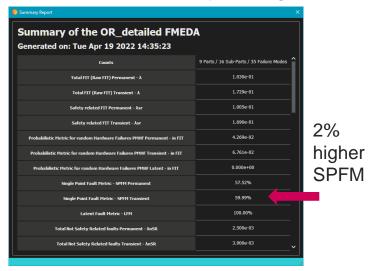
- No design data available
- FMEDA hierarchy only
- Failure rates and distribution solely based on early estimations





- With design data
- Design to FMEDA hierarchy mapping
- HW safety metric based on design data

Optimized Safety Design



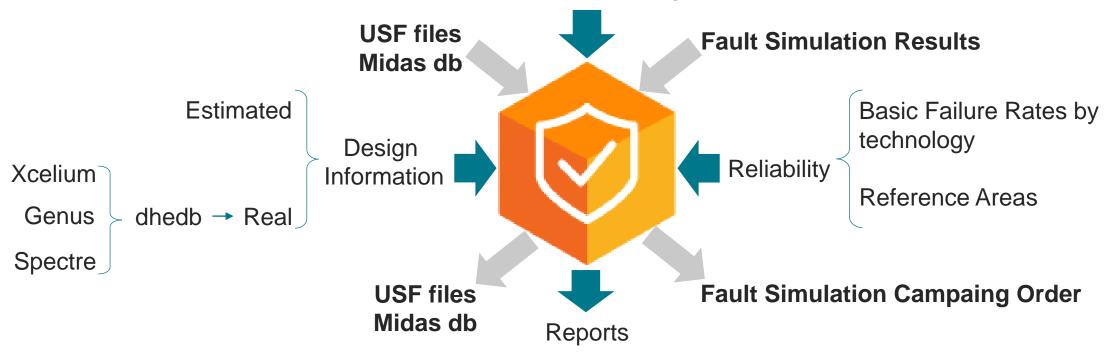
- With design & simulation data
- Design to FMEDA hierarchy mapping
- HW safety metric based on design & simulation data

Optimized FMEDA metric by using design & simulation-based data

Inputs / Outputs

- Definition of the FMEDA Project
- Parts, Subparts, Failure Modes, Safety Mechanism
- Design Mapping (for a Detailed FMEDA)
- Excel files

FMEDA Authoring



- FMEDA (Permanent+Transient)
- Summary
- SoC Summary
- Safety Goal Report

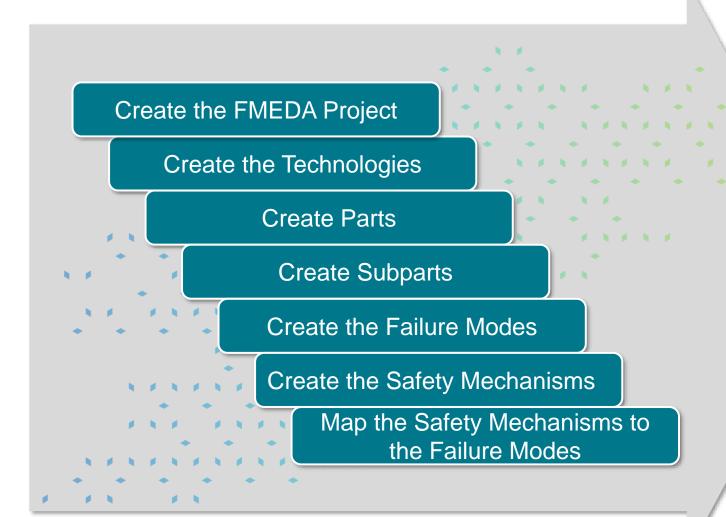




Architectural FMEDA



Architectural FMEDA Authoring Steps



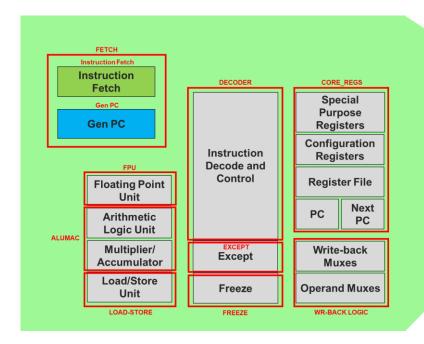
Queries

Generate Reports

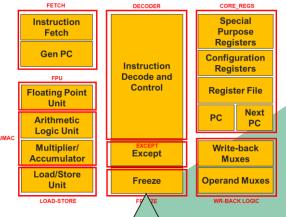


Design Decomposition

 Safety analysis are typically performed with a reduced number of hierarchical levels compared with the design hierarchy



FMEDA Project



Parts

First level of hierarchical decomposition

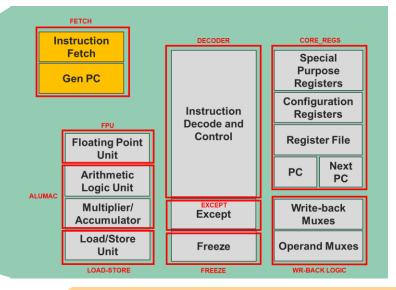
Subparts

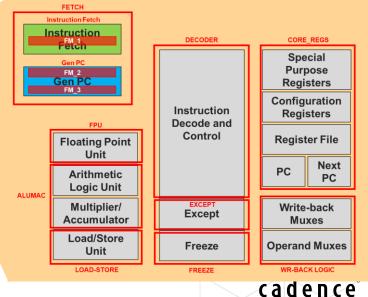
Second or greater level of hierarchical decomposition

Failure Modes

Manner in which an element or an item fails to provide the intended behavior

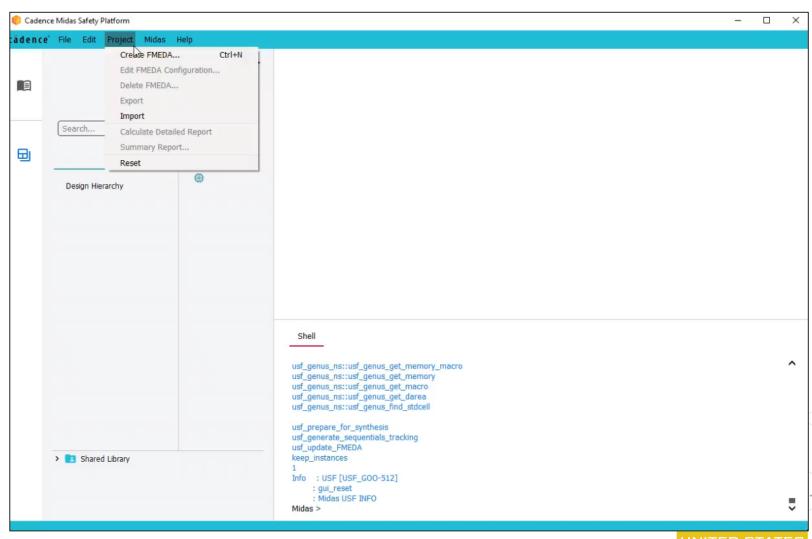
 The target is to define the failure modes, not to describe the circuit functionalities





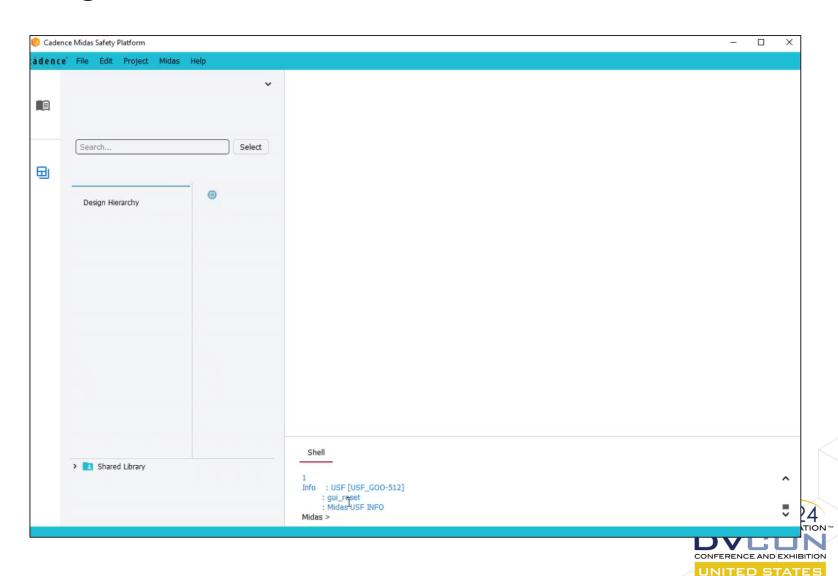
Functional Safety Authoring

- The GUI provides an user-friendly FMEDA authoring environment
- Safety objects can also be created with USF commands



Functional Safety Authoring

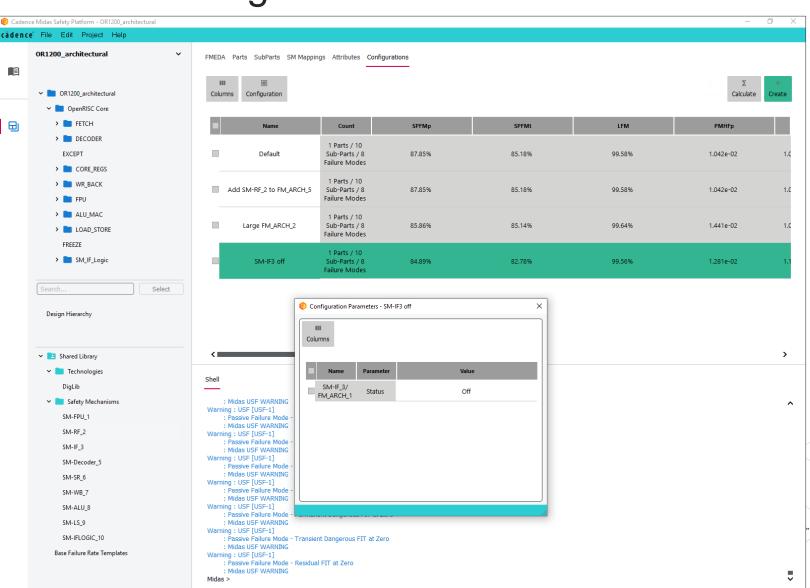
- The solution is fully scriptable
- Mixing GUI and scripted-automations is further possibile



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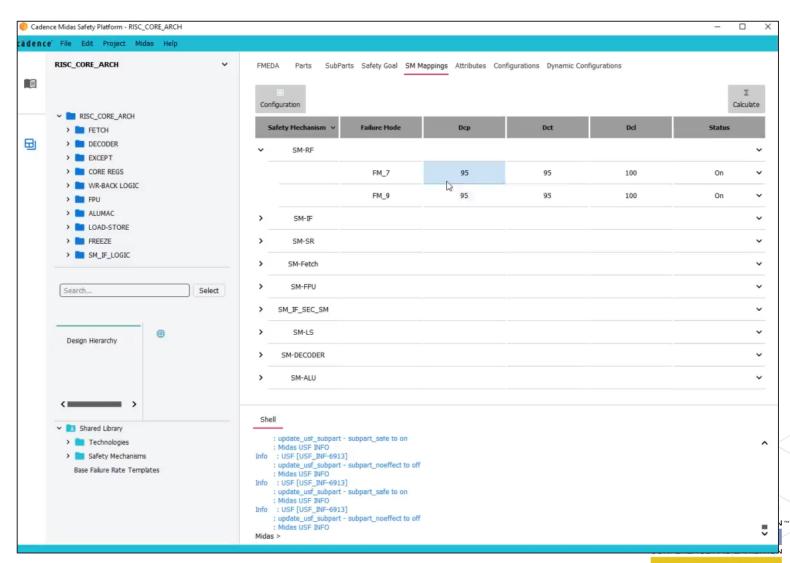
What-if Analysis: FMEDA Static Configurations

- Create configurations changing values in the FMEDA (e.g., design info., SM DCs)
- Each configuration generates safety metrics to be compared
- The configurations can be saved and restored



What-if Analysis: FMEDA Dynamic Configurations

- It is possibile to select one parameter (e.g, DC), define the interval and an output metric to be reported
- By leveraging the USF backend Midas provides the result of the simulation
- Graphs, and values, can be saved and restored





Detailed FMEDA



Detailed FMEDA Authoring Steps

Get Design Information (DHE)

Import Design Information

Create the FMEDA Project

Create the Technologies (Base Failure Rates)

Create Parts

Define Parts Mapping to Design

Create Subparts

Define Subparts Mapping to Design

Create the Failure Modes

Define Failure Mode Mapping to Design

Create the Safety Mechanisms

Map the Safety Mechanisms to the Failure Modes

Detailed-FMEDA Specific

Steps

Queries

Generate Reports

Safety Metric Verification



Design Hierarchy Extraction - Genus

```
usf genus ns::usf genus dhe
      [designInstance]
      {dheFileName}
      {ffFileName}
      [-bbox bboxFileName]
      [-seq leaf {instances name list}
       -comb leaf {instances name list} [-stopathier]]
                                                                          Hierarchical design instance to collect design information. If no instance is
designInstance
                                                                          passed, the current design is assumed to be extracted
dheFileName
                                                                          Filename to store design Hierarchy Information
ffFileName
                                                                          Filename to store the information for each hierarchical instance
                                                                          If this option is used, the command will try to find all the memories and the
-bbox bboxFileName
                                                                          macros in the design and to generate automatically a description file
[-seq leaf {instances name list}
                                                                          Support the extraction of leaf instances
 -comb leaf {instances name list} [-stopathier]]
```

- The generated database can be parsed with the usf_dhe_parser command
- A Midas database can be generated by using the save usf -db command

Design Hierarchy Extraction - Xcelium

```
xrun -elaborate
      -fault mdb gen
      [-fault top <top instance | top module>]
      [-fault mdb file
                                    <dheDB filename>]
      [-fault mdb ff]
      [-fault lib mfile
                            <lib list file>]
      [-fault mdb overwrite]
      [other options]
     <source files>
-fault top
                             Specifies the top_instance or top_module for design information extraction.
                             Enables design extraction and generates a Midas database file.
-fault mdb gen
-fault mdb file
                             Name of the Midas database file
-fault mdb ff
                             Includes sequential element extraction (pinout and flip-flop information) in the generated Midas database file.
-fault lib mfile
                             Specifies a liberty file list for gate-level design.
-fault mdb overwrite
                             Overwrites a previously generated Midas database file, if it exists
```

- For macros, read the liberty files into the Xcelium elaboration
 - $_{\circ}$ Area is extracted if the <code>-macro_cell</code> option is used when reading the relevant <code>.lib</code> files and the macro are elaborated as a library using $_{\rm V}$

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 Import the generated database into Midas or parse using the usf dhe parser -db command

Design Hierarchy Extraction - Spectre

- Spectre Circuit Information (info)
 - New keyword: what=dhe
- DHE Options

Parameter	Description		
dheminarea	Lower bound of area value for device to be considered during design hierarchy extraction		
dhesubckt	dhesubckt Design hierarchy is generated for all instances of the specified sub-circuits		
dheinst	Design hierarchy is generated for the specified sub-circuit instances		
dhexsubckt	All instances of the specified sub-circuits are excluded from the design hierarchy		
dhexinst	The specified sub-circuit instances are excluded from the design hierarchy		
dheparams	Name of the file that provides the rules to calculate area for subcircuits when what=dhe. Area are calculated on instance parameters		

 Import the generated database into Midas or parse using the usf_dhe_parser -db command



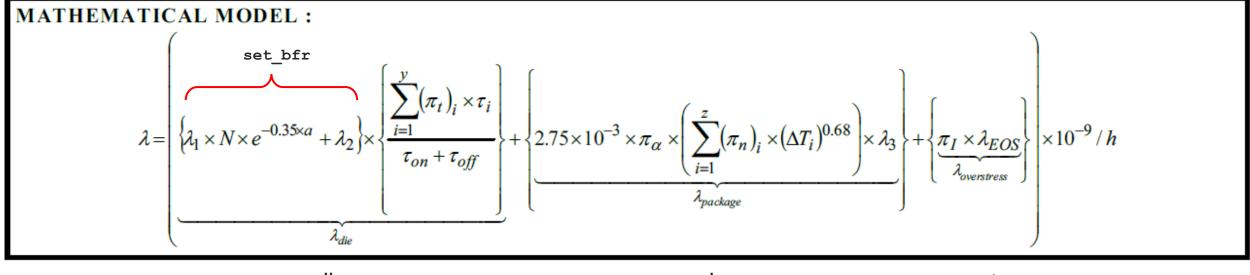




Basic Failure Rate (BFR) Support



IEC TR 62380: USF Commands



die package overstress

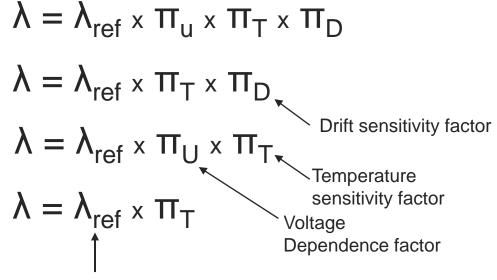
set_IEC62380_1DIE set_IEC62380_1Package set_IEC62380_1overstress

Customizations:

- Mission Profile: set_Mission_Profile; get_Mission_Profile
- Safe/Dangerous Ratio: set_safeness; get_safeness
- Confidence Level: set_Confidence; get_confidence
- Conservative (ISO26262-11) temperature derating
- Package customizations: set_IEC62380_cpackage; get_IEC62380_cpackage



SN29500: USF Command



Analog integrated circuits with extended range of operating voltages

Analog integrated circuits with fixed operating voltages

Digital CMOS-B

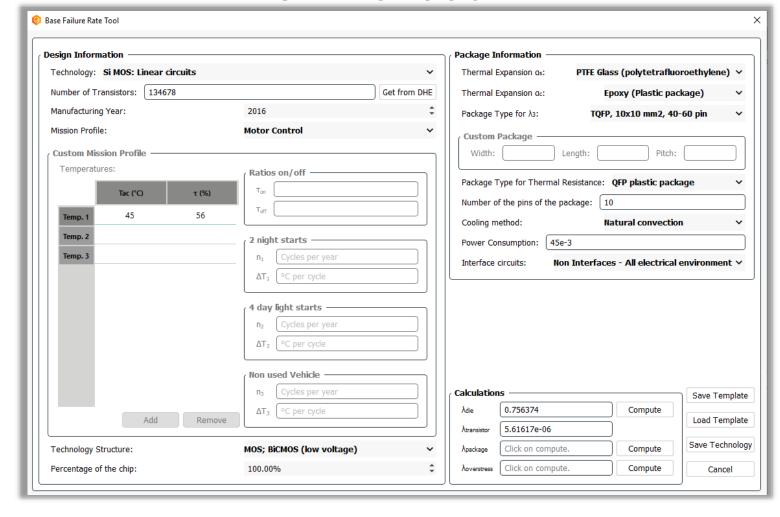
For all other integrated circuits



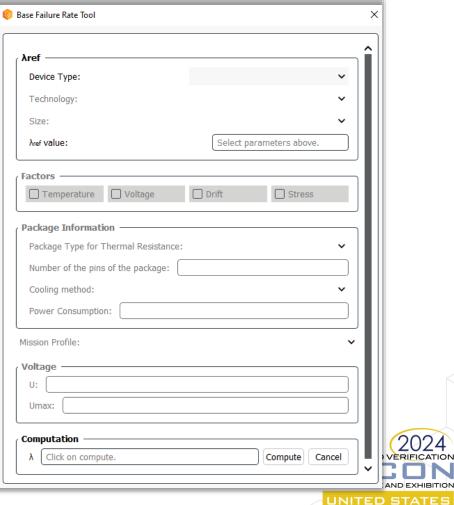


Midas GUI BFR Tools

IECTR 62380

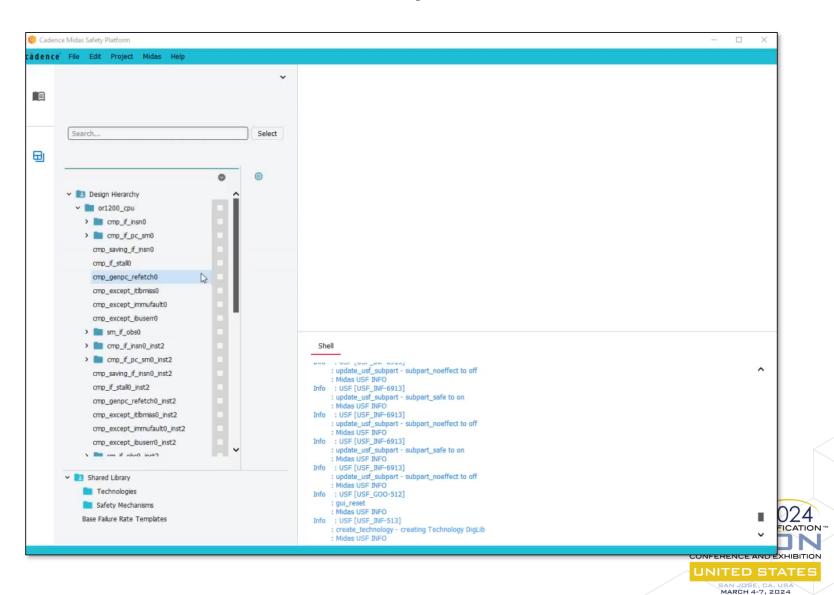


SN29500



Leverage Design Information in the BFR Computation

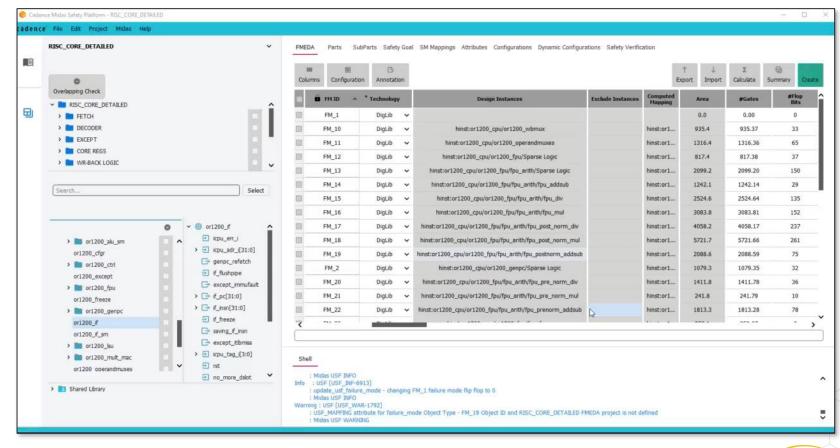
- Create a Technology by using the IEC 62380 BFR tool with automatic computation of the number of transistors
- The technology is saved in the shared library, available for all FMEDA projects



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Design Information Mapping

- Drag & drop Design information to Parts, Subparts and Failure Modes
- Area, equivalent number of gates and number of sequential elements are automatically computed







Safety Checks



USF check usf Command

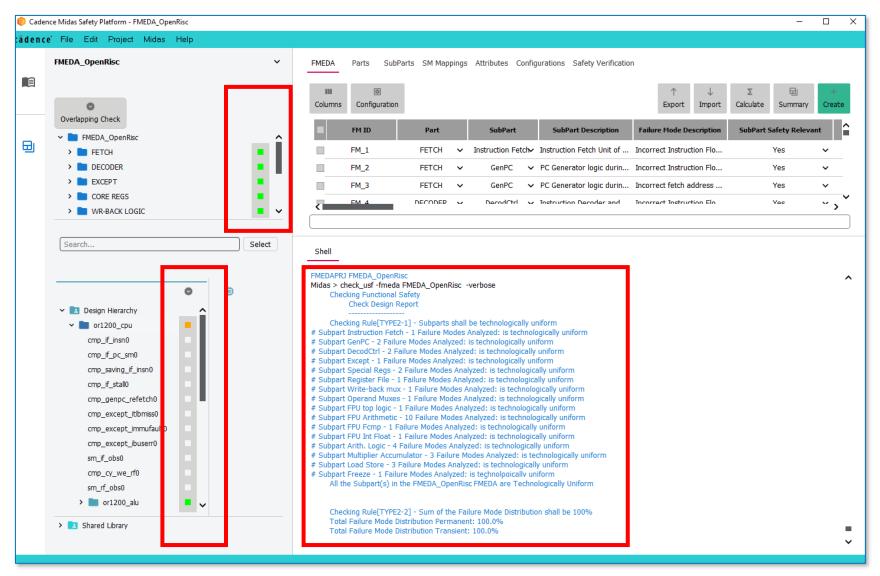
- check_usf -fmeda FMEDA_OpenRisc
- Rule Examples:

```
TYPE2-1: Subparts shall be technologically uniform
TYPE2-2: Sum of the Failure Mode Distribution shall be 100%
TYPE2-3: One safety mechanism should be defined for each failure mode
TYPE2-5: All the design logic has been mapped to a Subpart
TYPE2-6: All the design logic has been mapped to a Failure mode
TYPE2-7: All the design logic has not been mapped to more than one Part
```



- To report more information:
 - check_usf -fmeda FMEDA OpenRisc -verbose
- Adding custom specific rules:

Safety Checks on GUI



- Safety hierarchy overlapping checks
- The instances mapped to the given safety object (part, subpart, or failure mode) do not have any hierarchical dependency with other safety objects of the same type (part, subpart, or failure modes)
- The instances mapped to the given safety object (part, subpart, or failure mode) have one or more hierarchical dependency with other safety objects of the same type (part, subpart, or failure modes)
- Failure modes mapping checks
- Design instance is not mapped to any failure mode
- Design instance is mapped to one failure mode
- Design instance is mapped to more than one failure mode



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USF Query & Reporting



query usf USF Relational Queries

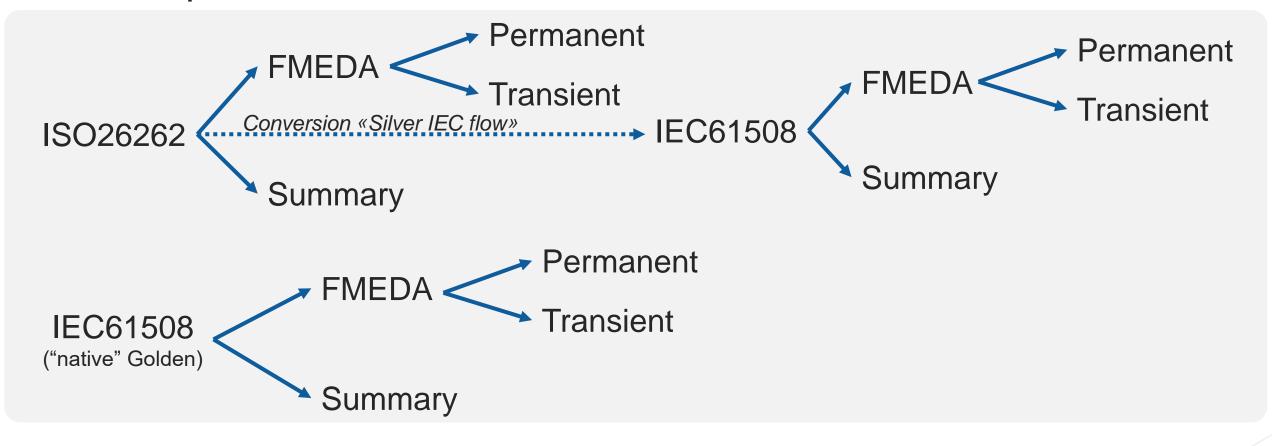
The query_usf command reports in a 'TCL friendly' format the information to create safety automations

LEVEL 0	query_usf *	Listing available information
LEVEL 1	<pre>query_usf {fmeda} {-obj_id id} {-obj_type type}</pre>	Direct query
LEVEL 2	<pre>query_usf {fmeda} {-obj_id id} {-obj_type type} [-ref_type RefType] [-ref_id refid]</pre>	By referencing another object

- How many FMEDA projects do we have?
 - query_usf *
 - FMEDAPRJ FMEDA OpenRisc
- How many Failure Modes have been defined for this project?
 - query_usf FMEDA_OpenRisc -obj_type failure mode -obj id *
 - FAILUREMODES FM_1 FM_2 FM_3 FM_4 FM_5 FM_6 FM_7 FM_8 FM_9 FM_10 FM_11 FM_12 FM_13 FM_14 FM_15 FM_16 FM_16 FM_17 FM_18 FM_20 FM_21 FM_22 FM_23 FM_24 FM_25 FM_26 FM_27 FM_28 FM_29 FM_30 FM_31 FM_32 FM_33 FM_34 FM_35
- Report the metrics for a specific FMEDA project
 - query_usf FMEDA_OpenRisc -obj_type fmeda -obj_id metrics
 - FMEDAPRJ FMEDA_OpenRisc off on on B off on {9 16 35} {57.5% 58.1% 100.0%} {4.269e-02 6.753e-02 0.000e+00 1.005e-01 1.611e-01} DigLib {{134678.6 131265.7 6563.0} {98720.7 96219.0 4431.0} {96364.7 93922.7 4328.0}} {57.52% -- -- -- } {100.00% -- -- -- }



USF Reports: ISO26262 and IEC61508



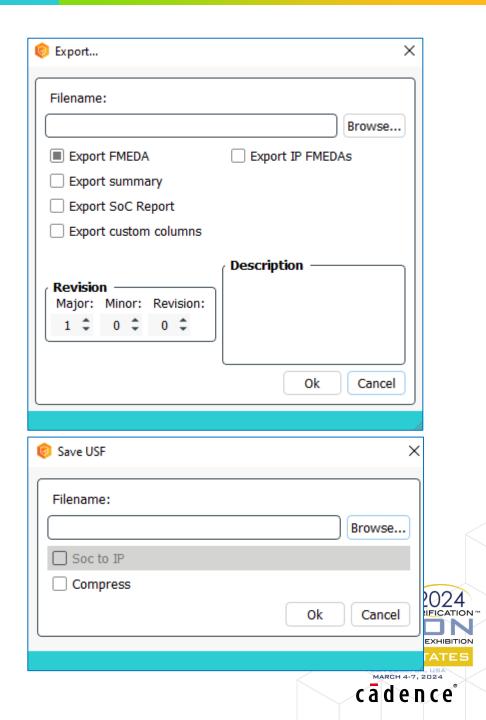
```
report_safety -standard iso26262 -fmeda myFMEDA permanent html "reports/ISO_PERMANENT.html"
report_safety -standard iso26262 -fmeda myFMEDA transient html "reports/ISO_TRANSIENT.html"
report_safety -standard iso26262 -fmeda myFMEDA report html "reports/ISO_SUMMARY.html"

report_safety -standard iec61508 -fmeda myFMEDA permanent html "reports/IEC_PERMANENT.html"
report_safety -standard iec61508 -fmeda myFMEDA transient html "reports/IEC_TRANSIENT.html"
report_safety -standard iec61508 -fmeda myFMEDA report html "reports/IEC_SUMMARY.html"
```



Midas Application Import-Export

- Microsoft Excel import/export is supported
- Rationales
 - Use USF (text file) for exchange/integration
 - Use MS Excel for final reporting and auditing



FMEDA Compression

Reduce the number of safety objects, preserving the metrics

```
set fmeda "IP1" -permanent -transient -ASIL B -architectural
create technology "Tech1" -type Digital -fitperm 1.070e-006 -fittrans_gate 1.640e-006 -fitbit 1.640e-006 -refarea 1.026
create technology "Tech5" -type Flash -fitperm 9.759e-004 -fittrans gate 0.000e+000 -fitbit 9.759e-002 -refarea 1.026
              "IP1/P1" -fmeda "IP1"
create part
create part
             "IP1/P2" -fmeda "IP1"
create subpart "IP1/P1/SP1" -part "IP1/P1" -fmeda "IP1"
create subpart
                        "IP1/P2/SP2" -part "IP1/P2" -fmeda "IP1"
create failure mode
                        "IP1/P1/SP1+Tech1:FM1" -type Active -technology "Tech1" -subpart "IP1/P1/SP1" -gates 1234 -flops 567 -safe perm 10 -fmeda "IP1"
create failure mode
                        "IP1/P1/SP1+Tech1:FM2" -type Passive -technology "Tech1" -subpart "IP1/P1/SP1" -gates 7654 -flops 321 -safe trans 40 -fmeda "IP1"
create failure mode
                        "IP1/P2/SP2+Tech5:FM1" -type Mission -technology "Tech5" -subpart "IP1/P2/SP2" -membits 890 -safe trans 70 -fmeda "IP1"
create failure mode
                        "IP1/P2/SP2+Tech5:FM2" -type Active -technology "Tech5" -subpart "IP1/P2/SP2" -membits 123 -safe perm 5 -fmeda "IP1"
create safety mechanism "SM:IP1/P1" -type Custom -class HW
apply safety mechanism "SM:IP1/P1" -to "IP1/P1/SP1+Tech1:FM1" -dcperm 80 -dctrans 90 -dclat 60 -fmeda "IP1"
save usf saved IPs compress.usf -compress
```

```
set_fmeda "IP1" -permanent -transient -ASIL B -architectural
create_technology "Tech1" -type Digital -fitperm 1.070e-006 -fittrans_gate 1.640e-006 -fitbit 1.640e-006 -refarea 1.026
create_part part_IP1_Tech1 -fmeda IP1
create_subpart subpart_IP1_Tech1 -fmeda IP1 -part part_IP1_Tech1
create_failure_mode fm_IP1_Tech1_Active_on -type Active -technology Tech1 -fmeda IP1 -subpart subpart_IP1_Tech1 -gates 4936 -flops 2268 -safe_perm 10 -
safe_trans 0
create_safety_mechanism sm_IP1_Tech1_Active -type Custom -class HW
apply_safety_mechanism sm_IP1_Tech1_Active -to fm_IP1_Tech1_Active_on -fmeda IP1 -deperm 80 -detrans 90 -delat 60
create_failure_mode fm_IP1_Tech1_Passive_on -type Passive -technology Tech1 -fmeda IP1 -subpart subpart_IP1_Tech1 -gates 30616 -flops 1284 -safe_perm 0 -
safe_trans 40
create_safety_mechanism sm_IP1_Tech1_Passive -type Custom -class HW
apply_safety_mechanism sm_IP1_Tech1_Passive -to fm_IP1_Tech1_Passive_on -fmeda IP1 -delat 60
```

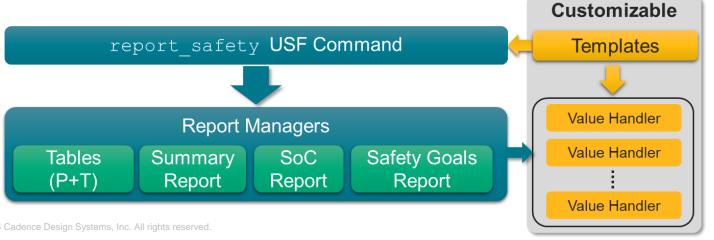
Report Customizations

- Report Managers
 - Organize the report information by rows and columns
 - Each report has its own template that defines the values handlers

а	b	С
1	2	3
-a1	b2	с3

Templates

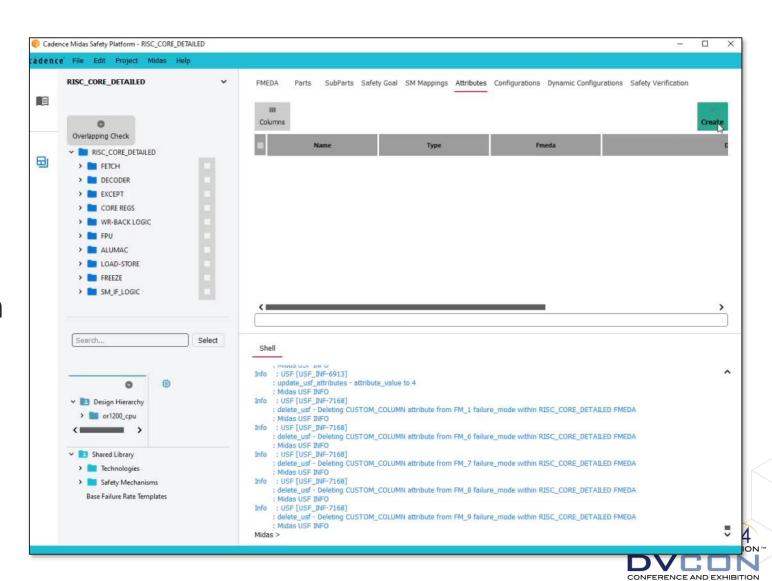
- Stored in the usf report safety templates directory
 - They can be replaced and customized by TCL procedures that have to follow a formalism defined in the USF command reference
- Customizations examples
 - Remove a column/row; Change the columns/row order
 - Adding a custom column/row by providing the TCL value handlers





Custom FMEDA Columns

- It is possibile to add custom columns to the FMEDA
- The custom FMEDA columns are leveraging USF attributes
- An attribute tagged to a failure mode can be a custom column
 - Select the «Create FMEDA custom column»
- Custom columns can be exported in the Excel reports



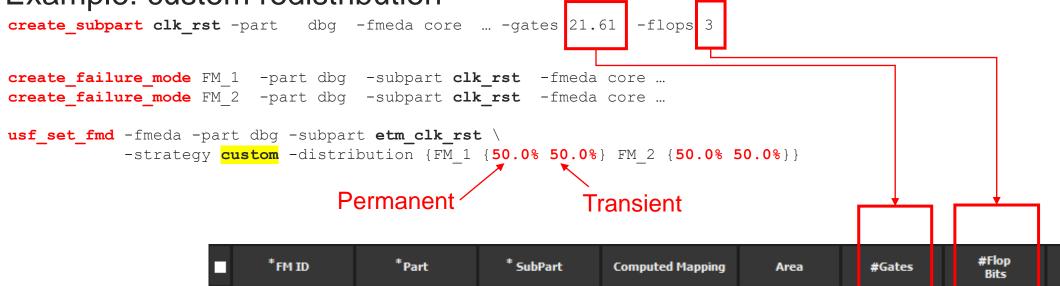
cādence

Failure Mode Distribution (FMD) Post-processing

Post-process the failure mode distribution

```
{-fmeda fmendaprj}
usf set fmd
             [-part part name]
             [-subpart subpart name]
             [-permanent]
             [-transient]
             [-strategy {area uniform | fit constant | custom} |
              -fm fm name [-value {0-100}]
             [-distribution {distributions}]
             [-rounding cost {default | cascade | sum of dist diffs}]
```

Example: custom redistribution



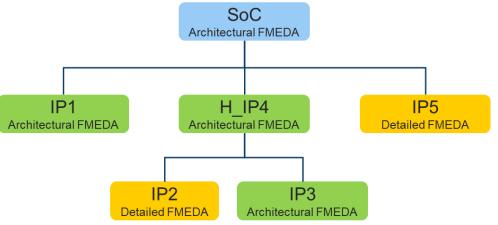


SoC Safety Analysis



SoC Safety Analysis Integration

- SoC metrics are calculated combining (grouping) IP FMEDAs
- IP FMEDA work is partitioned, the owner of the overall safety analysis is grouping the IP FMEDAs into a SoC FMEDA
- Multiple levels of hierarchy are supported
- Combination of detailed and architectural FMEDA is possible
- Keep the details in the IP FMEDAs but keep SoC FMEDA as simple as possible
- Propagation and combination of Safety Goals (aka Failure Mode Effect)
- Ability to support weights of Failure Modes to different Safety Goals



```
# FMEDA 1
usf reset
set troot1 {...}
load usf [file join $troot1 "arm cortex m7 fmeda.usf"]
save usf [file join $troot1 IP USF "fmeda 1.usf"] -compress
set fmeda1 [lreplace [query usf *] 0 0]
# FMEDA 2
usf reset
set troot2 {..}
load usf [file join $troot2 "dtmf.usf"]
save usf [file join $troot2 IP USF "fmeda 2.usf"] -compress
set fmeda2 [lreplace [query usf *] 0 0]
# FMEDA ...
# Create SoC and group IP FMEDA
usf reset
set fmeda SOC -soc -ASIL B -permanent -transient -architectural
group fmeda -fmeda list [list $fmeda1 $fmeda2] \
            -fmeda file [list [file join $troot1 IP USF "fmeda 1.usf"]
                        [file join $troot2 IP USF "fmeda_2.usf"]] -to SOC
```

Grouping IP FMEDAs into a SoC FMEDA: USF Command

```
      group_fmeda {-fmeda_list} {-fmeda_file} {-fmeda_file} {-to fmeda_soc} {-linkonly}

      Specify a list of FMEDA to link to a SoC FMEDA.

      —fmeda_list FMEDA_tags_list
      Specify a list of FMEDA to link to a SoC FMEDA.

      —fmeda_file FMEDA_files_list
      Optional. Specify a list of FMEDA project files to link to an SoC FMEDA.

      —to fmeda_soc
      Optional. Specify that the SoC FMEDA is used as a reference for the FMEDA project. The SoC FMEDA must be previously created with the set_fmeda_command using the _soc_option.

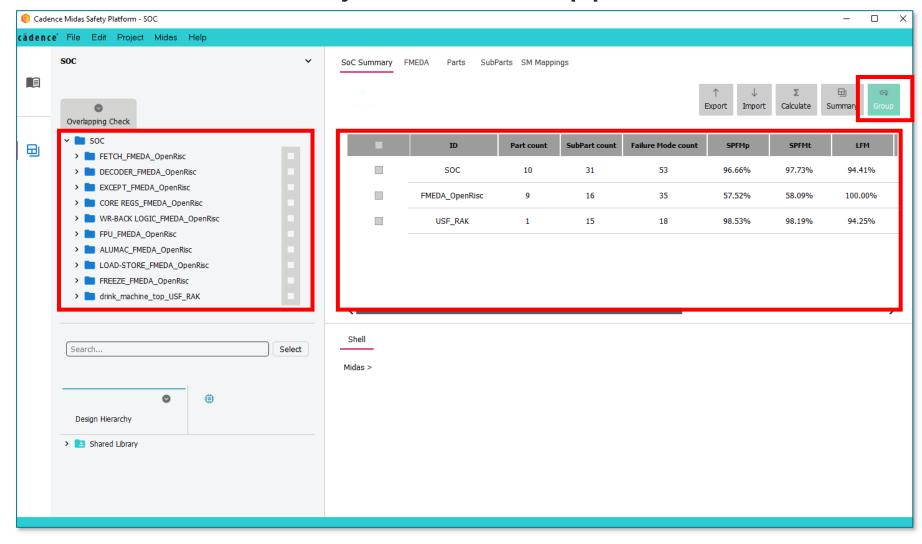
      —linkonly
      Optional. Link an IP FMEDA to the SoC FMEDA without copying parts, subparts, and failure modes
```

Examples

```
• group_fmeda -fmeda_list {myFMEDA1 myFMEDA2} -fmeda_file {myFMEDA1.usf myFMEDA2.usf} -to mySOCFMEDA
• group fmeda -fmeda list {myFMEDA1 myFMEDA2} -to mySOCFMEDA
```



SoC FMEDA Project: Midas Application



Grouping IP FMEDAs into a SoC FMEDA

- Safety Hierarchy
- SoC Summary



SoC Reports – USF Examples

- SoC Table
 - report_safety -fmeda SoC soc html SoC_soc.html

SoC	Summary
-----	---------

	FMEDA	SPFMp	SPFMt	LFM	PMHFp	PMHFt	PMHFlfm	Design Failure Rate Permanent (FIT)	Design Failure Rate Transient (FIT)	
	SoC	99.00%	99.00%	100.00%	1.426e-003	3.190e-003	0.000e+000	1.426e-001	3.190e-001	
Γ	>H_IP4	99.00%	99.00%	100.00%	9.507e-004	2.127e-003	0.000e+000	9.507e-002	2.127e-001	
ı	>IP1	99.00%	99.00%	100.00%	4.753e-004	1.063e-003	0.000e+000	4.753e-002	1.063e-001	

IPs Summary

- SoC Safety Goal table
 - report_safety -fmeda SoC safety_goal html SoC_sg.html

SG ID	FMEDA	Safety Goal Violations	SPFMp	SPFMt	LFM	PMHFp	РМНГр%	PMHFt	PMHFt%	Design Failure Rate Permanent (FIT)	Design FITp%	Design Failure Rate Transient (FIT)	Design FITt%	SG_H_IP4:P2	SG_IP1/P1
SG_SOC	SoC	SG_SOC violation	99.00%	99.00%	100.00%	9.111e- 004	100.0%	2.038e- 003	100.0%	9.111e-002	100.0%	2.038e-001	100.0%	x	X



Safety Goals (aka Failure Mode Effects, High Level Failure Modes)

Can be used to track the metrics of a list of failure modes of a given IP FMEDA

ID	Part	SubPart	Failure Mode	Safety Releva	FM Type	Techno	Area	#Gates	#Flop Bits	#bit	Raw Permanent	Total Safety	F _{SAFE} (p)	Fail rate Safe Fault	Fail rate	λ(p) %	K _{RF} (p) %	Single Point	SG_1	SG_2
FM_ROM	TOP	MYRO	ROMFM	Yes	Mission		0	0	0	0	0.00E+00	0.00E+00	0.00%	0.00E+00	0.00E+00		0.00%	0.00E+00		
FM_RAM	TOP	MYRAM	RAMFM	Yes	Mission	RAMLi	210487	0	0	8192	6.55E-02	6.55E-02	0.00%	0.00E+00	6.55E-02	98.83%	0.00%	6.55E-02		
FM_TDSP	TOP	TDSP	TDSP_CORE_INST FM	Yes	Mission	DigLib	6488.5	6488.53	256	0	4.54E-04	4.54E-04	0.00%	0.00E+00	4.54E-04	0.68%	0.00%	4.54E-04	Х	
FM_CONV_INST	TOP	CONV_	RESULTS_CONV_INST	Yes	Mission	DigLib	3716.2	3716.17	199	0	2.60E-04	2.60E-04	0.00%	0.00E+00	2.60E-04	0.39%	0.00%	2.60E-04		Χ
FM_GROUPED	TOP	GROUP	BASKET FM	Yes	Mission	DigLib	924.4	924.43	62	0	6.47E-05	6.47E-05	0.00%	0.00E+00	6.47E-05	0.10%	0.00%	6.47E-05		Χ

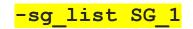
It is possibile to export the Safety Goals metrics into a report

report_safety -fmeda FMEDA_DTFM safety_goal html "fmeda_sg.html"

SG ID	FMEDA	Safety Goal Violations	SPFMp	SPFMt	LFM	РМНГр	PMHFp%	PMHFt	PMHFt%	Design Failure Rate Permanent (FIT)	Design FITp%	Design Failure Rate Transient (FIT)	Design FITt%
SG_1	FMEDA_DTFM	My safety goal 1	0.00%	0.00%		4.542e-04	58.3%	1.106e-02	57.9%	4.542e-04	58.3%	1.106e-02	57.9%
SG_2	FMEDA_DTFM	My safety goal 2	0.00%	0.00%		3.248e-04	41.7%	8.039e-03	42.1%	3.248e-04	41.7%	8.039e-03	42.1%

• It is possible to create SoC Safety Goals linked to IPs Safety Goals

```
create safety goal SGTOP -description "My new safety goal" -fmeda FMEDA SOC \
```





Safety Goals (aka Failure Mode Effects, High Level Failure Modes)

• In case the same failure mode is distributed across different safety goals, it is possible to specify a list of weights (sum of the weights must be 100%)

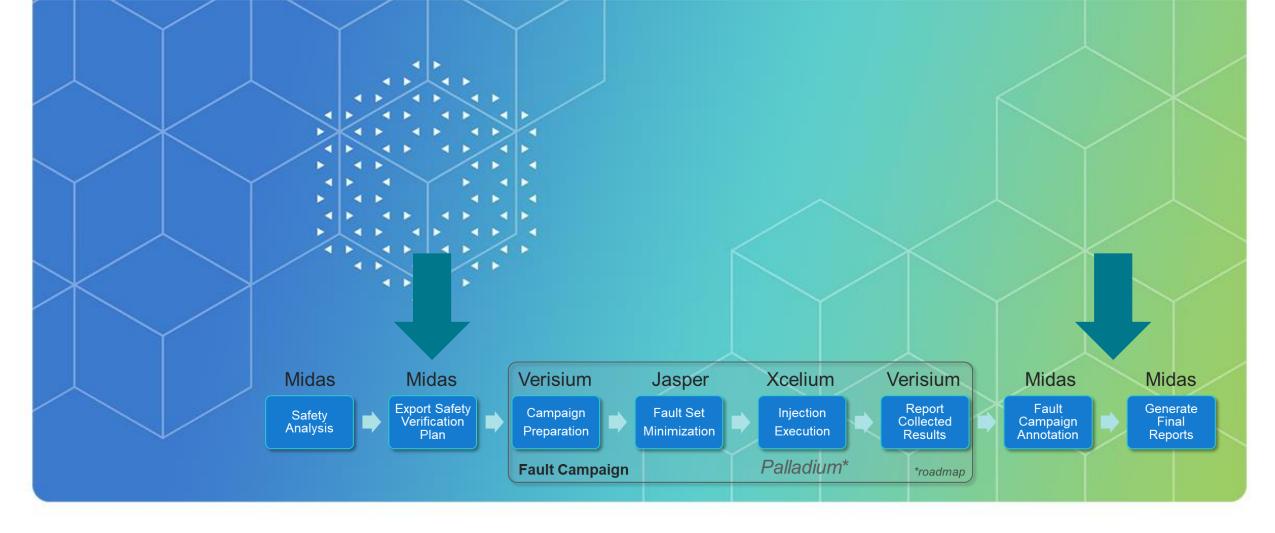
ID	Part	SubPart	Failure Mode	Techn ology	Area	#Gates	#Flop Bits	#bit	Raw Permanent faults FIT	Total Safety Related	SG_1	SG_2	SG_1 (W)	SG_2 (W)	SG_1 (Res%)	SG_2 (Res%)
FM_ROM	TOP	MYROM	ROMFM	ROMLi	0	0	0	0	0.00E+00	0.00E+00			0.00%	0.00%	0.00%	0.00%
FM_RAM	TOP	MYRAM	RAMFM	RAMLi	210487.2	0	0	8192	6.55E-02	6.55E-02			n nn%	0.00%	0.00%	0.00%
FM_TDSP	TOP	TDSP	TDSP_CORE_INST FM	DigLib	6488.5	6488.53	256	0	4.54E-04	4.54E-04	Х	Χ	20.00%	80.00%	100.00%	52.80%
FM_CONV_INS	TOP	CONV_INST	RESULTS_CONV_INST	DigLib	3716.2	3716.17	199	0	2.60E-04	2.60E-04		Х	0.00%		0.00%	
FM_GROUPED	TOP	GROUPED	BASKET FM	DigLib	924.4	924.43	62	0	6.47E-05	6.47E-05		X	0.00%		0.00%	

Example use case

Safety Goals

	Deadlock	Data Corruption	Exceptions	Performance
FM_1	 80%	20%		
FM_2	 	100%		
FM_3	 		50%	50%

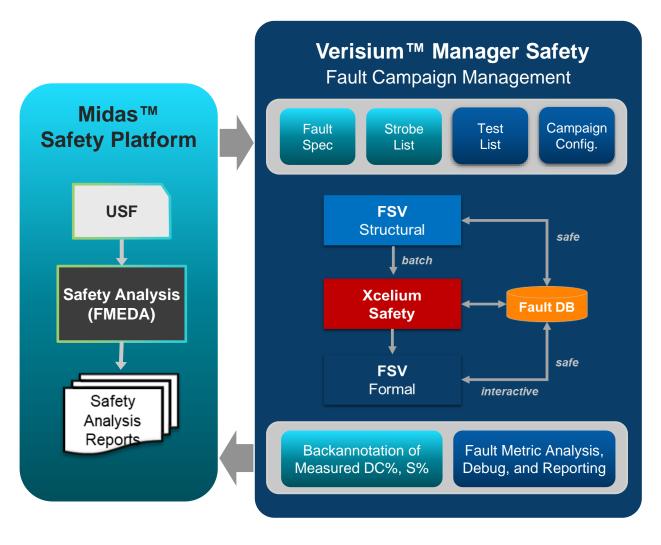




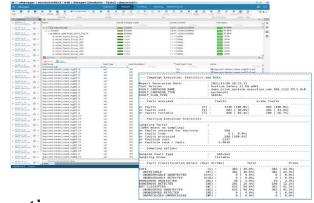
Safety Metrics Verification



Fault Campaign Management – Automation & Optimization



- Test selection and ranking
 - Coverage-based test selection
 - Customizable ranking criteria
- Fault list reduction
 - Fault sampling
 - Fault collapsing
 - Testability analysis
 - Test Dropping



- Fault campaigns execution
 - Measured Diagnostic Coverage and Safeness
 - Backannotation of results to FMEDA
 - Generate reports and analyze fault metric
 - FMEDA, fault classification, campaign summary,...

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Safety Metrics Verification



MidasTM

Definition of the observation and detection points

Generation of the Fault Injection Campaign Order Verisium™ Manager Safety Fault Campaign Management Expert Judgment

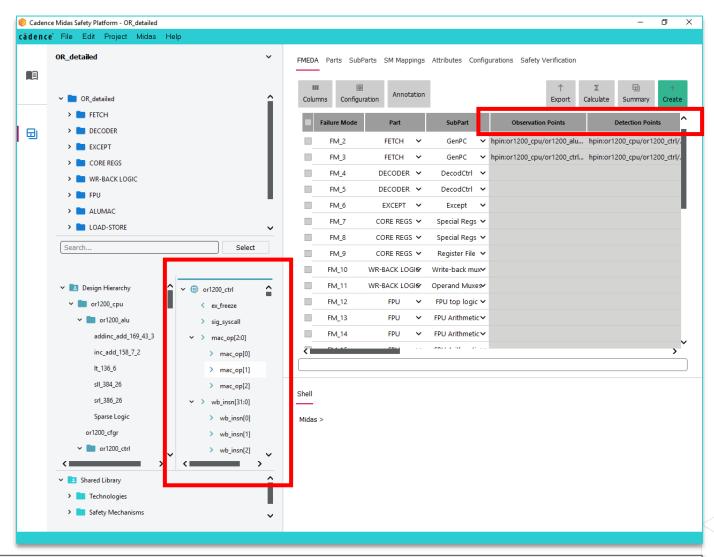
Annotation of the fault simulation Results

Final Reports



Strobing Points Definition

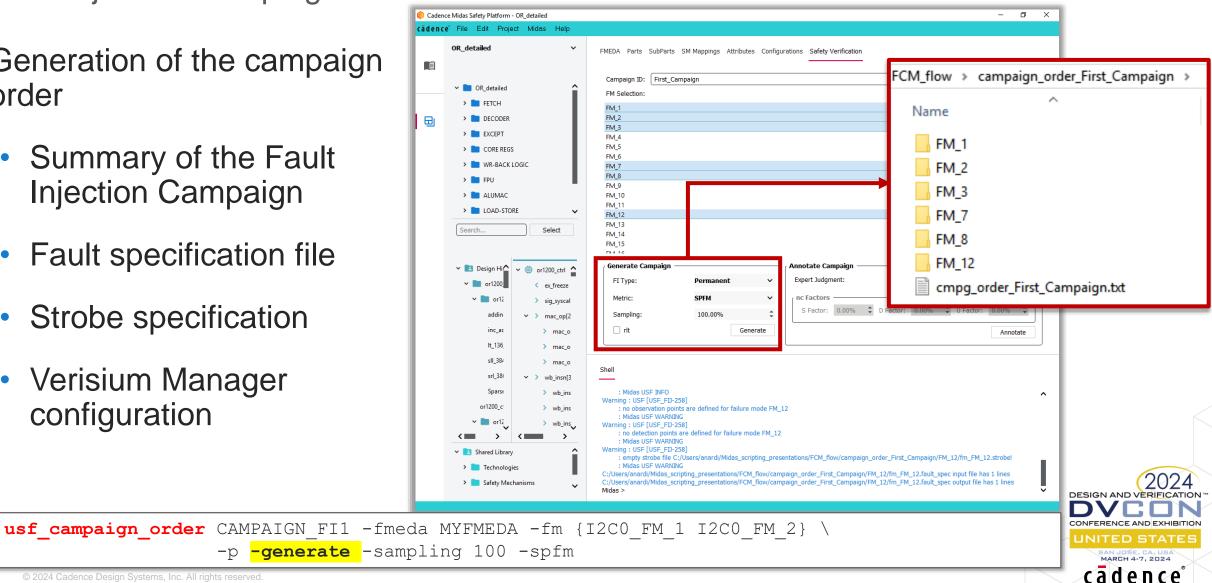
- Strobing points can be dragged & dropped from the design hierarchy into the related fields of the FMEDA
- The operation can be scripted



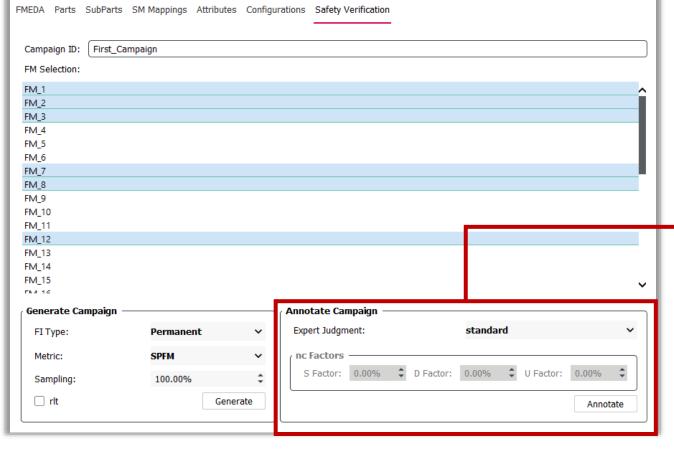
Driving Fault Simulation Campaign for DC Validation

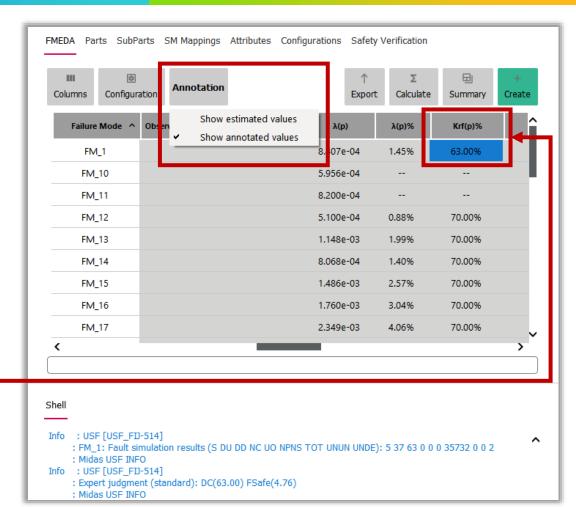
Fault Injection Campaign Order Generation

- Generation of the campaign order
 - Summary of the Fault Injection Campaign
 - Fault specification file
 - Strobe specification
 - Verisium Manager configuration



Back-annotation of the Fault Injection Campaign Results





usf_campaign_order CAMPAIGN_FI1 -fmeda MYFMEDA -fm {I2C0_FM_1 I2C0_FM_2 I2C0_FM_3 I2C0_FM_4} -p -annotate
-expert standard

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Supported Expert Judgment Methods

standard (Default)

$$F_{safe} = \frac{S_{measured}}{S_{measured} + NC_{measured} + DD_{measured} + DU_{measured}}$$

$$DC = \frac{DD_{measured}}{DD_{measured} + DU_{measured}}$$

progressive

$$Rate = \frac{DD_{measured} + DU_{measured} + S_{measured}}{S_{measured} + NC_{measured} + DD_{measured} + DU_{measured}}$$

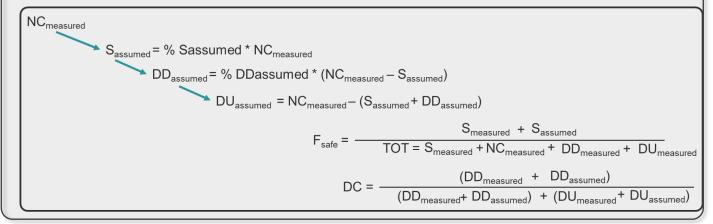
- F_{safe} is computed with NC_{measured}
- Rate is evaluating the % of NC_{measured}
 - Inversely: NC High → Rate Low

Automatically and conservatively moves a given percentage of NC faults to detected - The higher NC are, the less they are moved

Rate	DC calculation
> 75%	$DC_{75\%} = \frac{DD_{measured}}{DD_{measured} + DU_{measured}}$
>= 50% && <= 75%	$DD_{rate} = NC_{measured} * 0.5 * DC_{75\%}$ $DC = \frac{DD_{measured} + DD_{rate}}{DD_{measured} + NC_{measured} + DU_{measured}}$
< 50%	$DD_{rate} = NC_{measured} * 0.25 * DC_{75\%}$ $DC = \frac{DD_{measured} + DD_{rate}}{DD_{measured} + NC_{measured} + DU_{measured}}$ Design Systems, Inc. All rights reserved.

ncshare (two factors expert judgment)

Distribution of the Not Classified (NC) faults according to configurable percentages. DUassumed% + DDassumed% + Sassumed% = 100%



ncjudge

Redistribute percentages of faults to a given basket, with the only limitation that the total number of redistributed faults cannot be higher than the total

$\begin{array}{c} NC. \\ NC = \text{NOT CLASSIFIED} \\ Sfactor\$ \rightarrow Sassumed = NC \times Sfactor\$ \\ Dfactor\$ \rightarrow DDassumed = NC \times Dfactor\$ \\ Ufactor\$ \rightarrow DUassumed = NC \times Ufactor\$ \\ Sfactor\$ + Dfactor\$ + Ufactor\$ <= 100\$ \\ \end{array}$ $\begin{array}{c} F_{safe} = \frac{S_{measured} + S_{assumed}}{TOT = S_{measured} + NC_{measured} + DD_{measured} + DU_{measured}} \\ DC = \frac{(DD_{measured} + DD_{assumed})}{(DD_{measured} + DD_{assumed})} \\ \end{array}$

direct

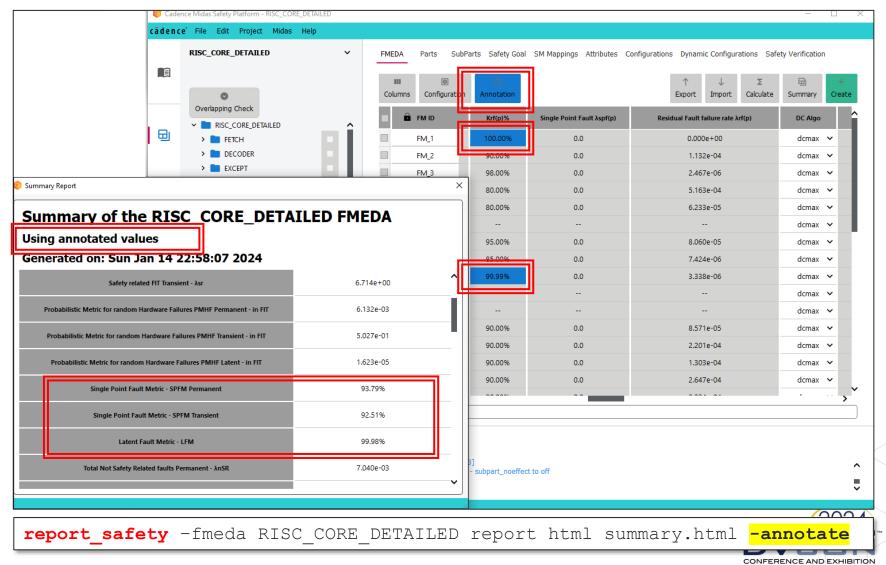


Enable external, not supported expert judgment algorithms. Use it to directly annotate DC or safe values based on users evaluation. The provided DC and safe values are annotated to the target failure modes.

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Generate Final Reports

- Once annotated, both estimated and measured values are available
- Switch between the two modes and generate reports
- Save and restore



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USF-based FMEDA-driven Functional Safety Verification

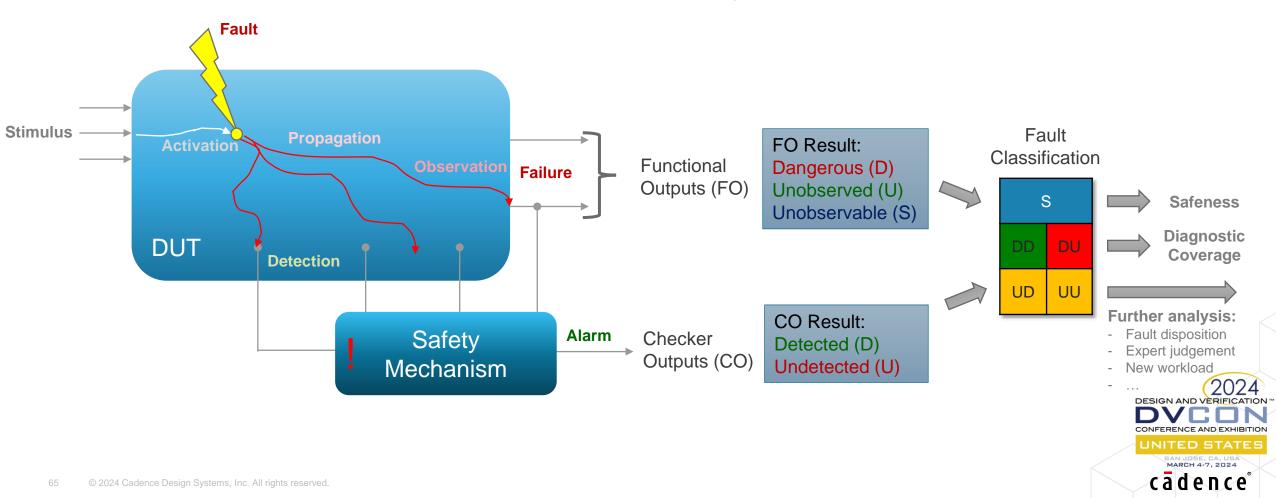
Fault Campaign Management (Verisium Manager Safety + Xcelium Safety + Jasper Safety)

Mangesh Mukundrao Pande

cadence

Automotive / Functional Safety / Random Faults / ...

- Goal: prevent or mitigate the effect of a hazardous event due to (operational) random faults
- Requirement: deliver diagnostic coverage according to ASIL (Automotive Safety Integrity Level)
- Method: integrate safety mechanisms across the system architecture
- Validation: show evidence and assess robustness via <u>fault injection</u>



Digital Safety Verification

FMEDA-driven safety verification

Campaign Automation – Verisium [™] Manager Safety
Unified front-end to manage all engines and analyze results
Validation and FMEDA back-annotation of diagnostic coverage

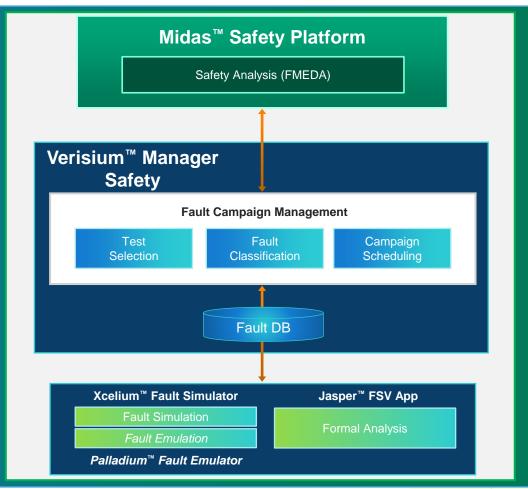
Complexity Reduction — Jasper™ FSV App

Applies industry-leading formal techniques to fault analysis

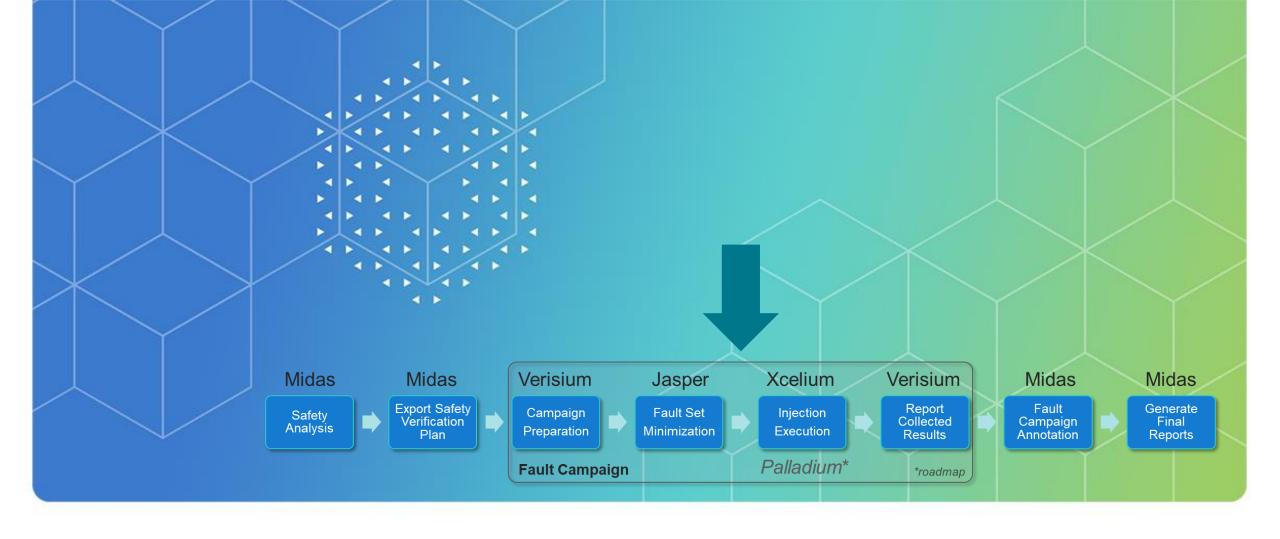
Increases safety verification performance

Injection Engine – Xcelium[™] Fault Simulator Native serial and concurrent fault simulation engine

Acceleration – Palladium™ Fault Emulator







VerisiumTM Manager Safety Fault Campaign Manager – FCM



Fault Campaign <u>Automation</u> and <u>Analysis</u>

1. Prepare Data

- Single front-end campaign configuration
- Expand fault targets & instrument design
- Translate strobe definition

4. Generate Reports

- Campaign summary report
- Diagnostic Coverage / Safeness
- FMEDA validated results

Verisium Manager Safety Fault Campaign Manager - FCM Minimite Automation **Analysis**

Fault Metric Analysis

- Merge fault results across different campaigns
- Disposition of not-classified faults
- Offer insights towards analysis closure

2. Minimize Fault Set

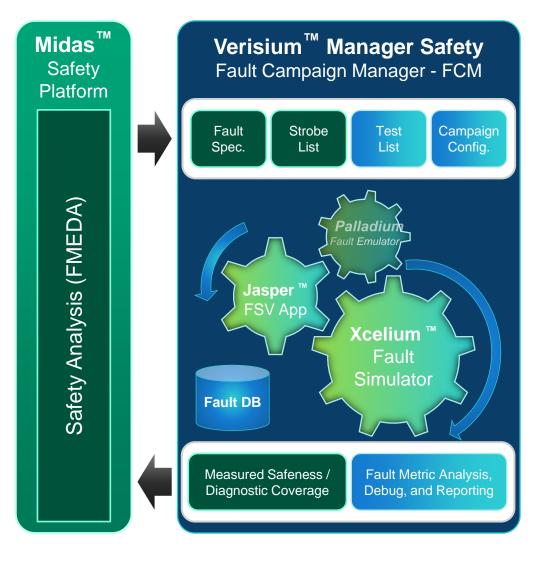
- Collapse redundant faults
- Identify unobservable/safe faults
- Test-based fault pruning

3. Execute Campaign

- Create runs per fault groups
- Verisium Manager state-of-the-art DRM
- Drop exhausted faults/tests



FMEDA-driven Fault Campaign



Inputs

- Safety Engineer
 - Fault Targets (derived from FMEDA ⇔ design mapping)
 - Strobe List (observation and detection points)
- Verification Engineer
 - Test List (selected for fault analysis)
 - Campaign Configuration
 - Optimizations, runs distribution, customization, etc.

Outputs

- Summary Report
 - Measured Fault/Diagnostic Coverage, Safeness
- Fault Annotation
 - Fault Metric Analysis, annotated fault list, ...



Fault Classification

Safeness (S%)

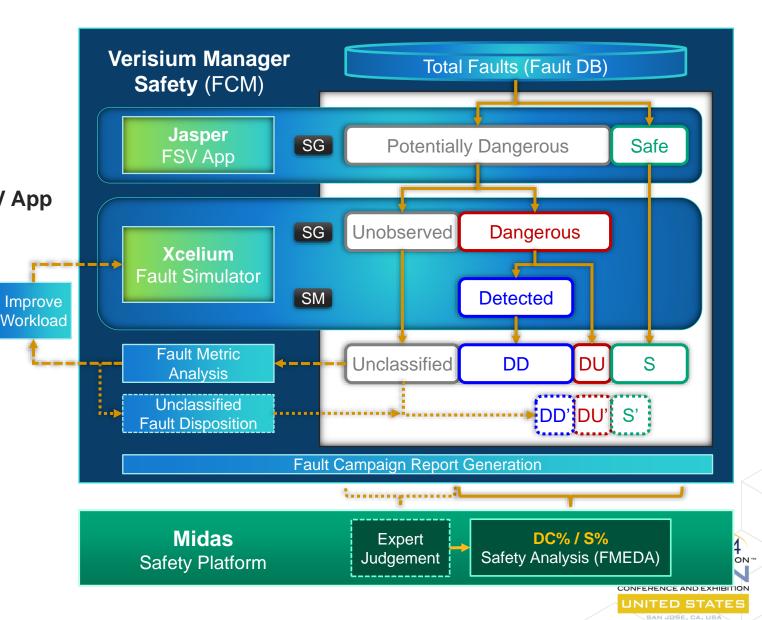
- Unable to violate Safety Goal (SG)
- Exhaustive fault analysis with Jasper FSV App

Diagnostic Coverage (DC%)

- Safety Mechanism (SM) performance
- Simulation evidence with Xcelium Safety
 - <u>Dangerous</u> faults <u>Detection</u> (DD)

Closure

- Dedicated fault metric analysis
- Insight for Workload/SM improvements
- Disposition of the Not Classified faults

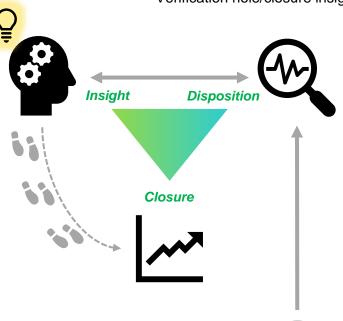


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Features / Optimizations

Dedicated Fault Metric Analysis

- Merge results across different campaigns
- Disposition of not-classified faults
- Verification hole/closure insight



Unified Fault Database

- · Scalable to multi-millions of fault results
- Cross-engine data exchange

1. Test Ranking & Pruning

Custom ranking criteria

3.

a. FST

b. Good

Simulation

Fault

Pruning

Design Elaboration

Fault

Analysis

Fault

DB

Fault Simulation

Test Selection

Report

Generation

Verisium Manager™

Safety

2. Fault Instrumentation

- Expand user fault specification
- Collapsing and design-based testability

3.a. Structural Fault Reduction

- Strobe-based testability (safe faults)
- Advanced fault collapsing

3.b. Fault-free Simulation

- Required for serial engine and pruning
- Test-based activatability analysis

4. Test-based Fault Reduction

- · Strobe-based propagability analysis
- Constant propagation analysis

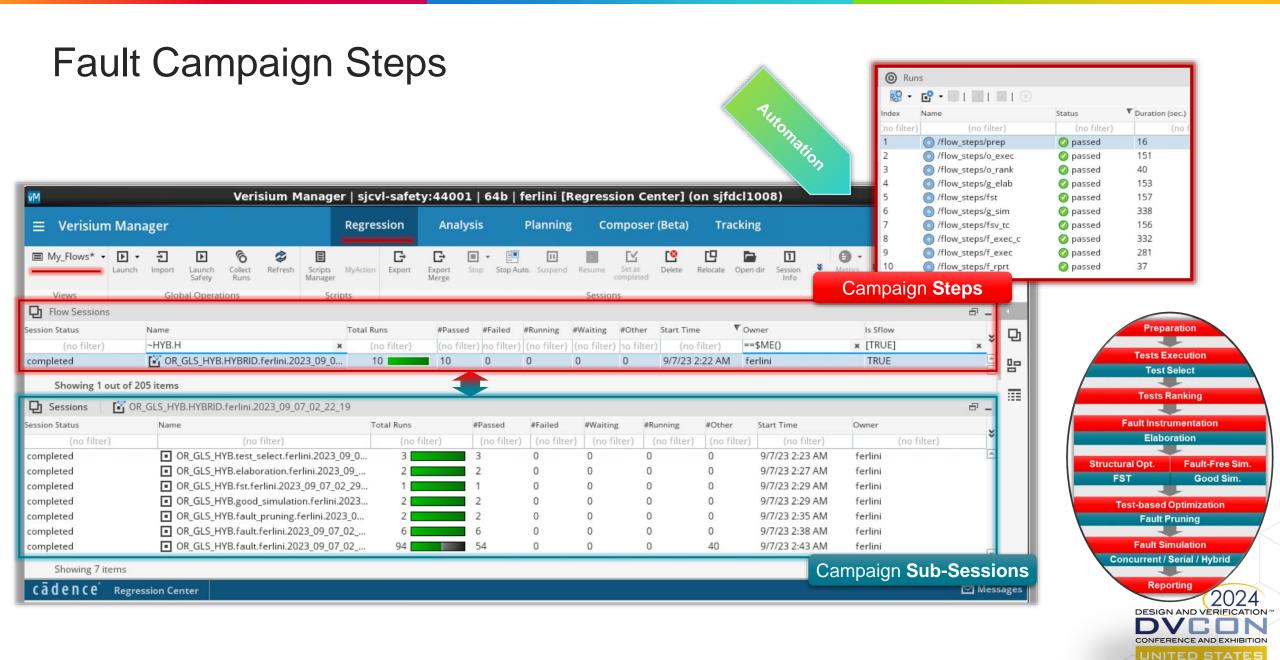
5. Dynamic Fault Simulation Control

- State-of-the-art run distribution manager
- Fault/Test Dropping, Timeout
- Skip pre-injection simulation

6. Reports Generation

- Campaign summary, annotated fault list
 - FMEDA back-annotation results

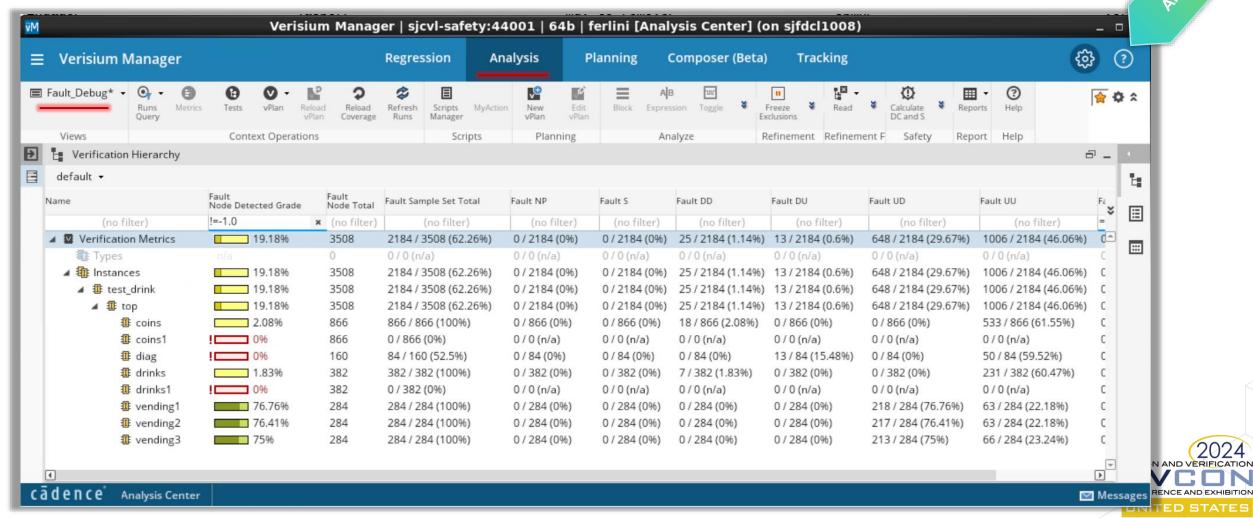




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Dedicated Fault Analysis

Hierarchical Data



Campaign Summary Report

Date, tool version, fault types, sampling, ...

Static instrumentation fault results

Overall campaign(s) merged results

Fault Disposition (user refinement)

Applicable client configuration

Report Date : 2023/02/13 02:49:17 Tool Version : Xcelium 22.09-s005 , Verisium Manager 22.09-s002 Fault Types : SA0+SA1 Sampling : 50.00% of testable faults Total Faults Total Prime Sample Faults 2546 Faults 2626 465 Safe 1658 63.14 1658 65.12 0.00 Not Injected 479 18.24 458 17.99 7.53 Injected 489 18.62 430 16.89 Fault Annotations 2626 2546 484 465 SAFE 1666 63.44 1666 65.44 1.65 1.72 362 13.79 65.16 DANGEROUS DETECTED 11.90 DANGEROUS UNDETECTED 4.68 123 4.83 123 25.41 123 26.45 475 18.09 454 17.83 6.67 Not Classified UNOBSERVED DETECTED UD 0.00 0.00 0.00 0.00 6.67 UNOBSERVED UNDETECTED 8.04 199 NOT SIMULATABLE 0.00 0.00 0.00 INJECTION FAILED IF 0.00 0.00 0.00 0.00 NOT PROCESSED 101 3.85 3.61 0.00 0.00 163 To S From UU From DU Fault Coverage 16.83 71.08 Test Coverage Fault Coverage : 100 * (DD + D) / (DD + DU + S + D + U + P + U+U + U+D) : 100 * (DD + D) / (DD + DU + D + U + P)Test Coverage Merge File Refinement : /vols/vmanager t2b/ferlini/activities/2022/FCM tech up 22.09/refine2.vRefine

---- CAMPAIGN : new rprt sample , permanent , CONCURRENT

Sampled fault scope

Fault and Test Coverage results and formulas







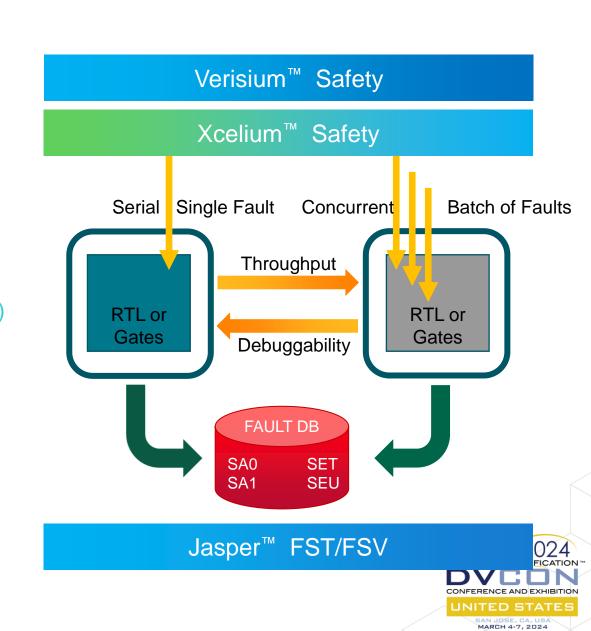


Fault Campaign Management – Safety Engines



Xcelium Safety App

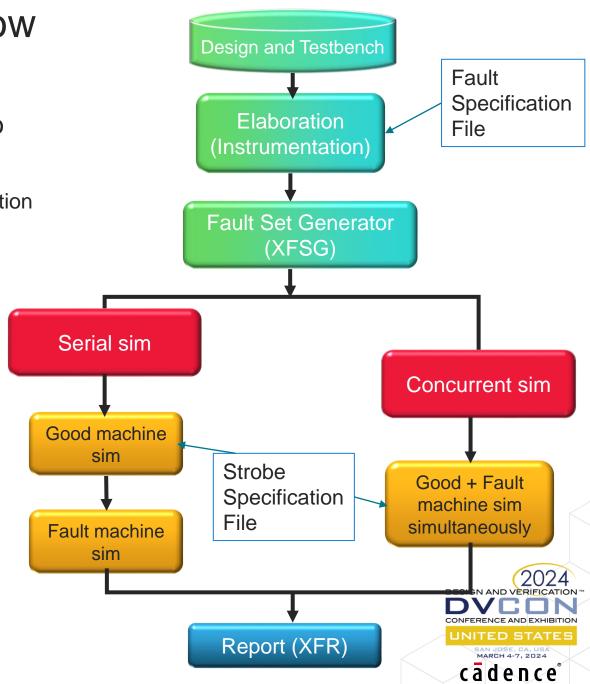
- The Xcelium Safety App provides native fault simulation by integrating Functional & Safety Engines
- Supports existing Xcelium Methodologies
 - · Capture Replay, DSS (Dual Snapshot), Save Restore
- The Xcelium Safety App operates in 2 modes:
 - Serial mode: Flow setup and Debug
 - Concurrent mode:
 - Higher throughput
 - 5-100x faster than serial
 - Handles 2K to 20K faults in a single run (Single CPU Core)
- Supports Random Sampling as Sampling Percentage, Sampling Number
- Support Dual Strobe, Single Strobe Fault Classification
- Interoperable serial and concurrent fault simulation engines
- Both modes have identical flow and can easily switch back and forth
- The Xcelium Safety App simulates & annotates all faults in the fault DB
- Supports Fault Boundary to limit CoPF (Cone of Fault Propagation)



cadence

Xcelium Safety Overview – User Flow

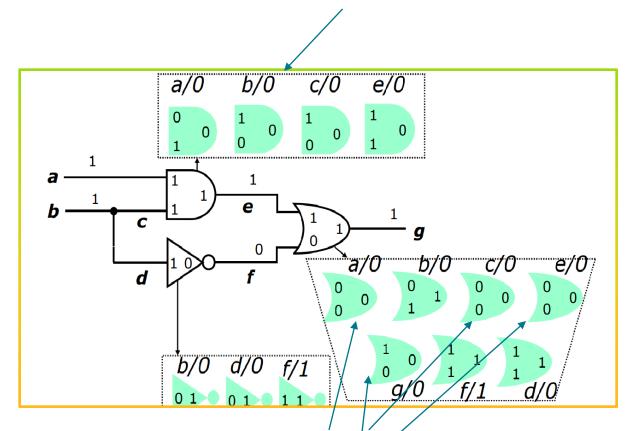
- Easy to migrate from Functional verification flows to Fault Injection
 - Additional file (Fault File) and option to be added to Elaboration
 - Elaboration has added steps for fault Instrumentation
- Fault Simulations
 - Serial Engine or
 - Concurrent Engine
- Hybrid Mode Support
 - Xcelium Safety Simulation allows for users to run the hybrid flow where Concurrent followed by Serial
- Reporting
 - Standalone Support Available



Xcelium Safety – Concurrent

- Inject and simulate multiple faults together
- Concurrent fault simulation is a throughput solution
 - Allows injection of multiple faults during simulation in a single run.
 - Better throughput than the serial engine.
 - New simulation kernel
 - new scheduler
 - fault management
- Native Integration with Xcelium Engine
- Good Simulation runs along with Fault Simulation
 - Fault Value diverges then simulation continues, or fault is dropped
 - Multiple fault runs concurrently in a single simulation (corresponding test vector)
 - Single CPU core per simulation, no multi core multi thread support

At least one value differs Good Value



Incorrect Output Values in this list indicate detectable faults i.e., a/0, c/0, e/0, g/0



cadence

Concurrent Fault Simulation - Overview

Xcelium Elaboration

- Used for Fault Instrumentation
- Extra analysis done for Concurrent
- Example:
 - xrun -fault_file <input_fault_file> -fault_rtl

XFSG

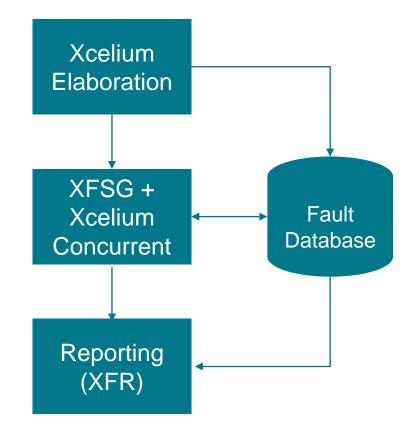
xfsg -fault_work ./fault_db/ -fault_type sa0+sa1 -fault_list foutput -fault_spilt_size <number of Faults>

Xcelium Concurrent Run

- Run the injected faults in concurrent mode
- Each fault simulated independent of the others
- Example:
 - xrun –fault_concurrent –input <injected_fault_list>

Reporting

- Separate utility to generate fault report (Xfr)
- Example:
 - xfr -fault_work <path_to_fault_database>



Fault Injection Summary:

Multiplicity: 1

Total number of faults: 3872/1936 (total/prime)

Number of fault runs: 1

Number of faults injected: 1869

SA0(546), SA1(1323), SEU(0), SET(0)

Expected finish time: 110us

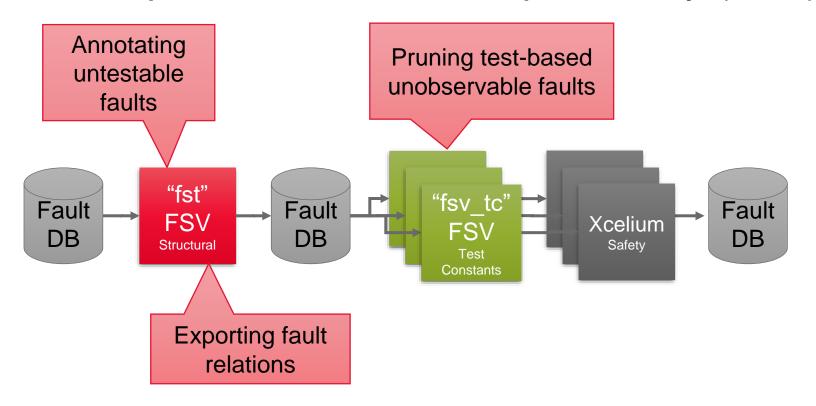
ON_TIME(657), DELAYED(0), PREMATURE(0), TIMEOUT(0), STOPPED(1212), UNKNOWN(0

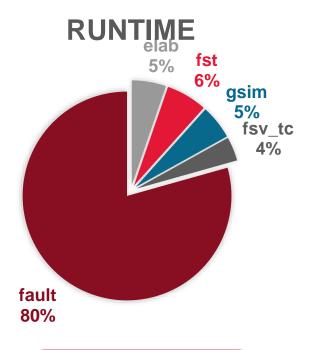
Stuck-At (0/1) Fault Table

Otdok / kt (o/ 1) 1 dait 1abio			
	Total #	Prime#	
Untestable	67		67
Detected	0		0
Potentially_detected	0		0
Undetected	0		0
Unobserved_detected	0		0
Unobserved_undetected	1078		657
Dangerous_detected	2727		1212
Dangerous_undetected	0		0
Not_injected	0		0
Total	3872		1936



FCM – Optimizations from Jasper Safety (FSV)





A few minutes of optimization can save hours of simulation

- FSV exports fault relations → equivalent faults will be skipped
- FSV annotates untestable faults → Safe faults will be ignored
- FSV annotates faults as unobservable by test → Pruned faults will be dropped



Jasper Functional Safety Verification App (FSV)

FSV Structural Fault Analysis

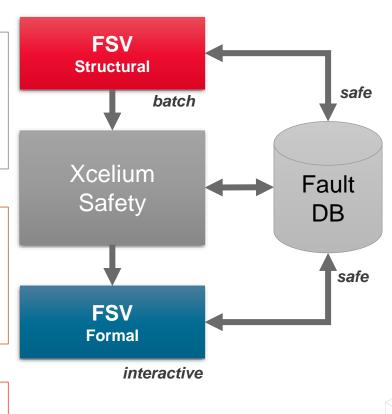
- Structural fault connectivity, activatability and relation analysis
- Highly automated pre-qualification flow for Xcelium Safety
- Reduces number and runtime of fault simulations

FSV Formal Fault Analysis

- Formal activatability and propagatability analysis
- Interactive debug, schematics and visualization of propagation
- Assists fault analysis sign-off with Xcelium Safety

FSV Custom Safety and Security Analysis

- Custom strobes and faults specification to model hacker attacks
- Advanced formal checks, barriers and multiplicity of faults
- Addresses safety and security hardware qualification



FSV Custom



FSV Structural Analysis Check Types



- Out-of-COI Analysis
 - A fault node outside the Cone-of-Influence (COI) has no physical connection to the functional strobe(s)
 - Fault is Out-of-COI = Safe

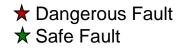


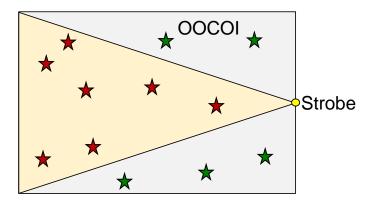
Activatability Analysis

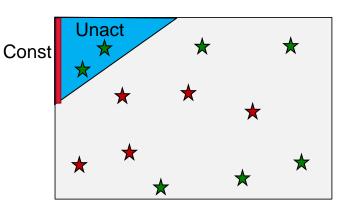
- A SA0/1 fault injected on a node which is constant 0/1 cannot be activated
- Fault is Unactivatable = Safe

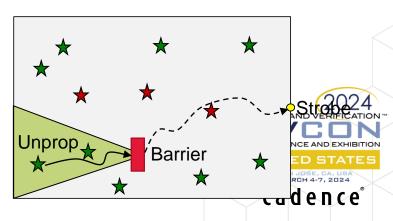


- Propagatability Analysis
 - A fault that is activated and in COI, but cannot propagate to the functional strobe
 - Fault is Unpropagatable = Safe









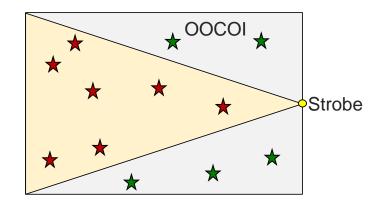
FSV – Structural Analysis



```
[<embedded>] % check fsv -structural
                                                         check fsv -structural
INFO (IFSV018): Analyzing whole FO strobe's COI.
INFO (IFSV018): Analyzing whole CO strobe's COI.
                                                            -[-fault relations (on|fo|co|off)]
INFO (IFSV010): COI analysis complete.
INFO (IFSV001): Fault collapse info :
                                                            [-coi (on|fo|co|off)]
         Equivalent: 3836393, Collapse ratio: 47%
         Observed: 1020441, Collapse ratio: 12%
                                                            [-constant (on|off)]
         Unobservable: 5819404, Collapse ratio
                                               : 72%.
INFO (IFSV019): Extracting FO strobe's COI.
                                                            [-propagation_analysis (on|fo|co|off)]
INFO (IFSV001): Results of COI analysis:
                                                            [-constant_propagation_analysis(on|fo|...)]
         Out: 1409152, In: 6622838, Unknown: 0.
INFO (IFSV019): Extracting CO strobe's COI.
INFO (IFSV001): Results of COI analysis:
         Out: 1610232, In: 6421758, Unknown:
INFO (IFSV011): Starting constant analysis.
INFO (IFSV012): Constant analysis complete.
                                                                        5 different structural
INFO (IFSV001): Results of constant analysis:
         Unactivatable: 411526, Activated: 416612, Unknown: 5794934.
                                                                          analysis checks
INFO (IFSV048): Starting Propagation analysis for FO strobes.
INFO (IFSV049): Propagation analysis for FO strobes complete. Found 123422 unpropagatable faults.
INFO (IFSV048): Starting Propagation analysis for CO strobes.
INFO (IFSV049): Propagation analysis for CO strobes complete. Found 123246 undetectable faults.
INFO (IFSV050): Starting constant propagation analysis for FO strobes.
INFO (IFSV051): Constant propagation analysis for FO strobes complete. Found 360534 unpropagatable faults.
INFO (IFSV050): Starting constant propagation analysis for CO strobes.
INFO (IFSV051): Constant propagation analysis for CO strobes complete. Found 351466 undetectable faults.
```

FSV – Structural Analysis – COI Analysis

- COI Analysis
 - Goal is to produce "safe" fault results
 - Sensitive to strobes and design
 - Scales up to multi-million gates



```
INFO (IFSV019): Extracting FO strobe's COI.
INFO (IFSV001): Results of COI analysis:
          Out: 1409152, In: 6622838, Unknown: 27.
INFO (IFSV019): Extracting CO strobe's COI.
INFO (IFSV001): Results of COI analysis
Out: 1610232, In: 6421758, Unknown: 27.
```

Out of COI FO means "safe"!

Out of COI CO means nothing for safeness. But it could be used for qualifying the diagnostic safety mechanism.

Unknown: Black boxes prevent deterministic results



FSV – Structural Analysis – Sequential Constant Propagation

FSV Structural Analysis benefits from constants in the design

```
assume scan_en==0 -env
```

- But regular constant propagation stops at flops/latches!
- FSV runs sequential constant propagation in the beginning of structural analysis
 - Design constants are propagated through sequential elements using reset, clock and design constraints

```
set_fsv_structural_seq_constants_propagation ( off | simple | formal )
```

- off: no analysis

- simple: using fast proof simplification only (default)

- formal: using regular prove engines* and associated time limits

Benefit

- * formal requires FSV license
- More propagated constants, more structurally safe faults
- Note: Only environment constraints (-env) are respected!
 - Task based constants are ignored in structural analysis

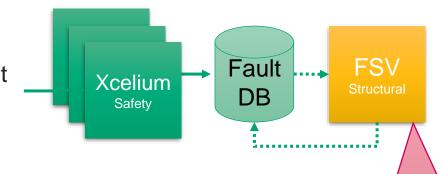
Example customer testcase

	off	simple	formal
constant flops	0	373	1206
faults out of COI	47695	47695	47695
faults unactivatable	1639	4850	9305
faults unobservable	3491	12175	14953
faults safe	52825	64720	71953



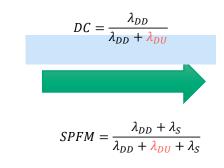
FSV – Structural UU Disposition Post-Fault Simulation

- Try hard to find more SAFE faults in a fault injection campaign with many Unclassified faults (UU, UD)
 - Reduces the % of UU/UD fault
- By adding custom constraints and barriers
 - Declare UU/UD as SAFE!
 - Analysis of remaining UU/UD proposes additional test sequences in XFS to turn UU into DD or DU



UU/UD faults = unclassified DU/DD/S faults = classified Confidence of SPFM/ASIL:

SPFM 99.3% with 50% UU - low SPFM 99.1% with 2% UU - high

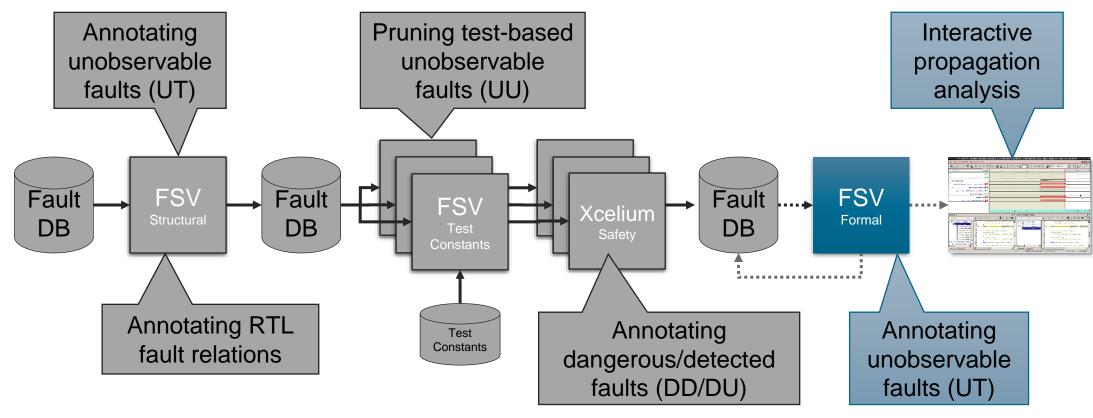


SPFM	ASIL
>= 99%	D
>= 97%	С
>= 90%	В
< 90%	А

Annotating unobserved faults as SAFE



FSV Integration with Xcelium Safety Simulator

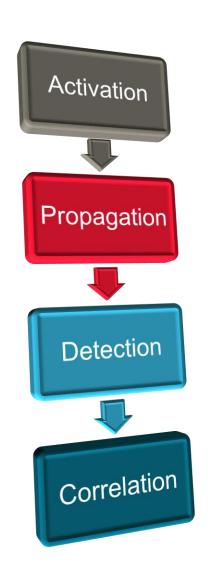


- FSV Structural automatically annotates unobservable faults and RTL fault relations in database
- FSV TC prunes faults not exercisable by particular simulation test
- Xcelium Safety simulates and annotates all remaining faults in database
- FSV Formal annotates unobservable faults and provides interactive propagation analysis

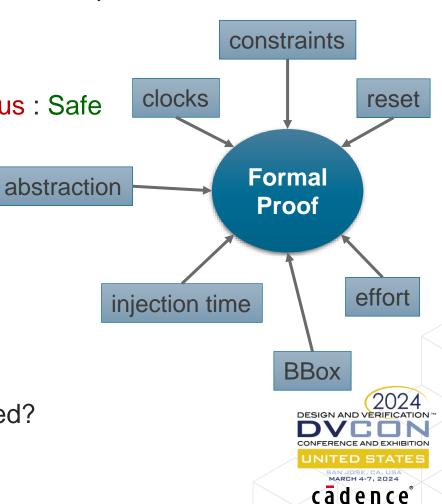


FSV Formal Analysis Check Types





- Activation Analysis
 - Can the fault be functionally activated from the inputs? No = Safe
- Propagation Analysis
 - Can the fault propagate to FO? Dangerous : Safe
 - Will it always propagate to FO?
- Detection Analysis
 - Can the fault be detected at the CO?
 - Will it always be detected at the CO?
- Correlation Analysis
 - Will a propagated fault always be detected?



Generating Properties



FSV can generate 6 types of formal properties

```
check_fsv -generate [-id <tcl_list>] [-task <name>]
    [-activatability (on|off)]
    [-propagatability (on|off)]
    [-detectability (on|off)]
    [-always_propagated (on|off)]
    [-always_detected (on|off)]
    [-propagated_always_detected (on|off)]
```

6 different formal analysis checks

Easiest, runs in an optimized region

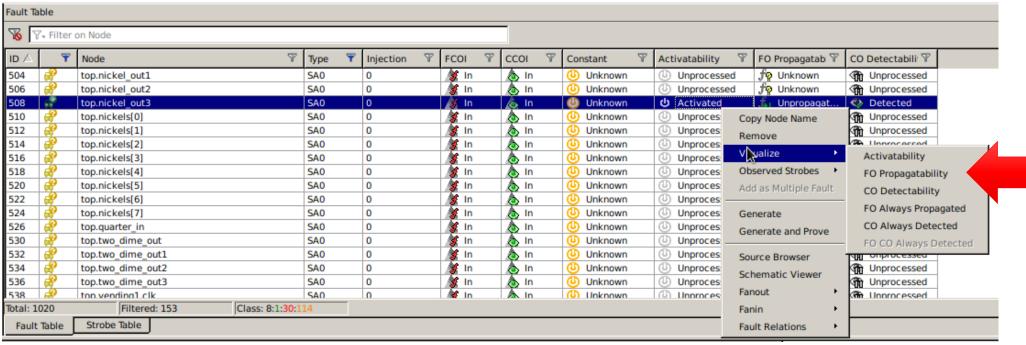
Most difficult, yet most meaningful check

```
INFO (IFSV007): Starting generate.
INFO (IFSV002): Mapping X and undriven.
INFO (IFSV004): Analyzing non-resettable regs.
INFO (IFSV005): Completed analyzing non-resettable regs.
INFO (IFSV013): Creating <fsv_task_0>.
INFO (IFSV016): Modeling task <fsv_task_0> faults.
INFO (IFSV003): Mapping non-resettable regs.
...
INFO (IFSV014): Task <fsv_task_0> created.
INFO (IFSV009): Generate completed.
```



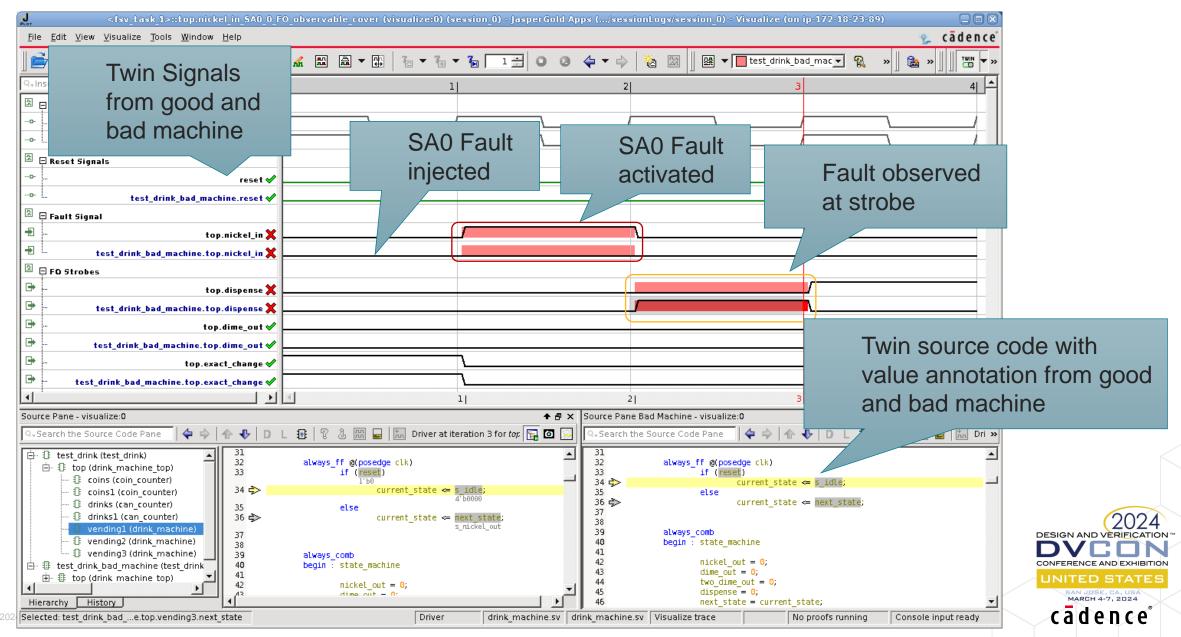
FSV Formal – Debugging Visualize Waveforms

- Visualize for detection traces and unobservable analysis
 - Use Right-Mouse-Button Menu over an item in the Fault Table

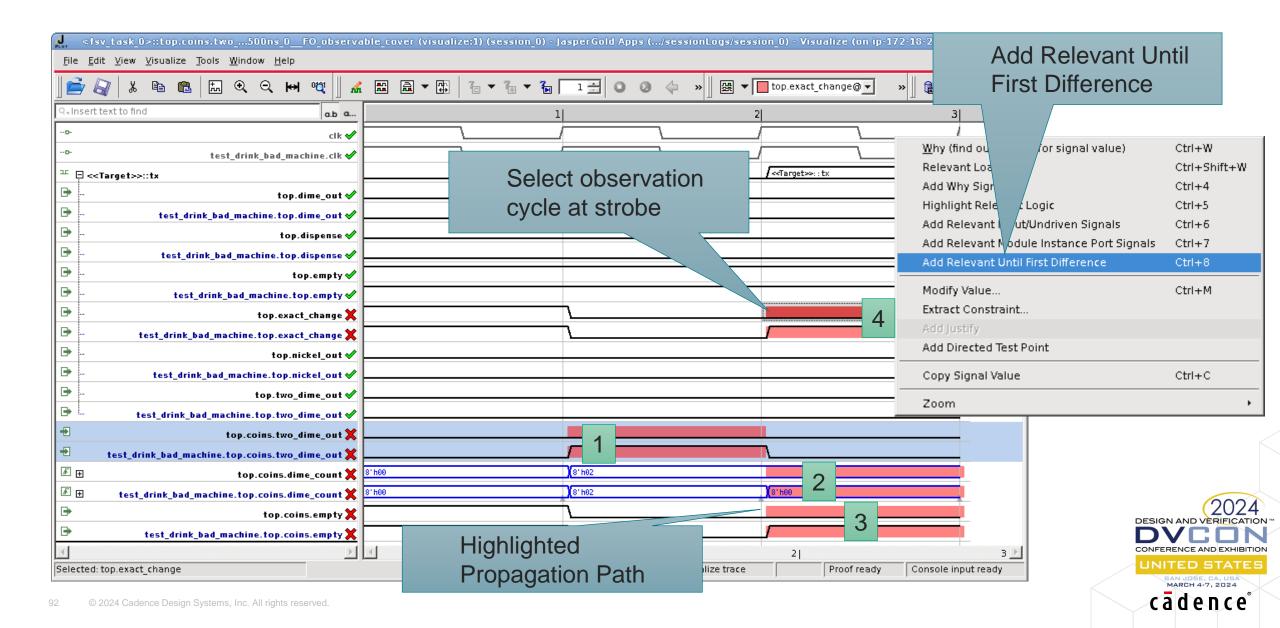




FSV Formal – Visualize Fault Detection Traces



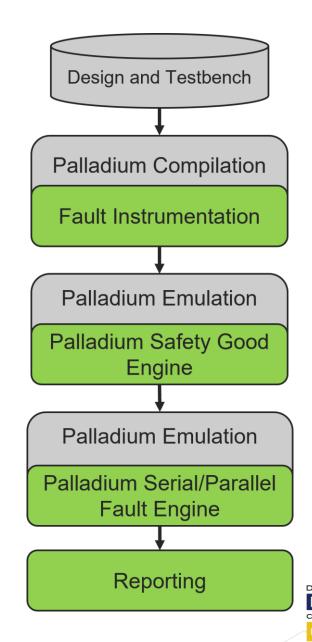
FSV Formal – Visualize Highlight Propagation Path



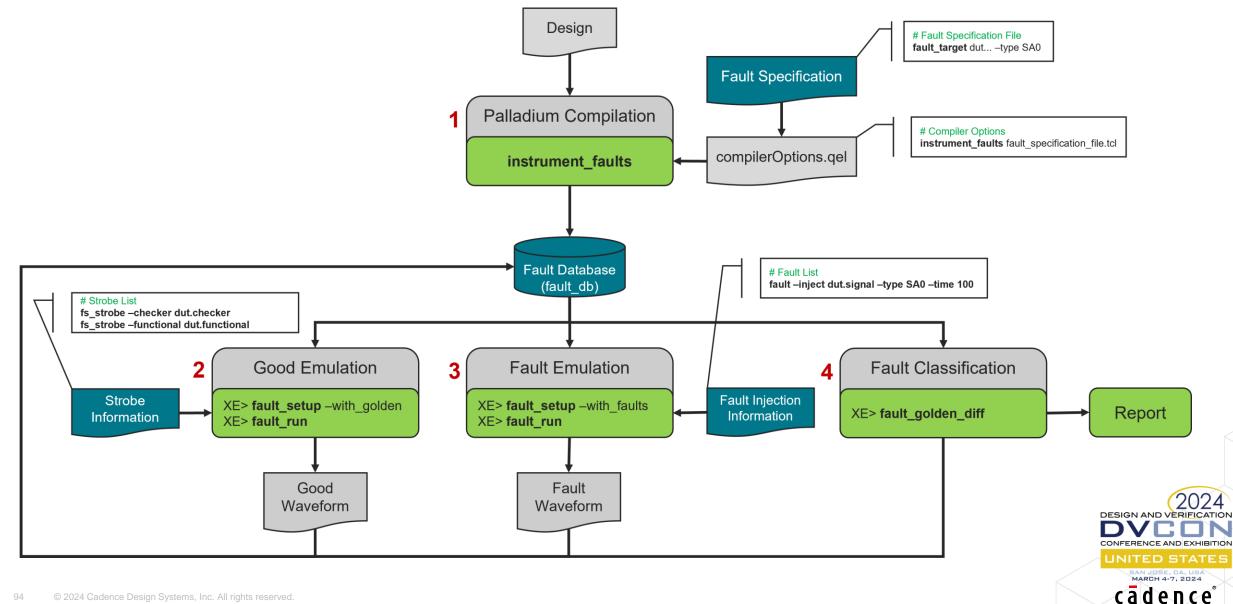
Palladium Safety

User Flow

- Easy to migrate from Functional verification flows to Fault Injection
 - Some files and option to be added to Palladium compilation
 - Faults are identified and instrumented during compilation
- Fault-free circuit emulation (Good Emulation)
 - Process strobe points and capture good waveform
- Fault Emulation Flows
 - Serial Fault Injection
 - Parallel Fault Injection
 - Interactive Fault Injection
- Fault Detection
 - Post-processing
 - Compares good and fault waveforms after each run
 - Inline
 - Detects the fault during the run using detection system
- Reporting
 - Standalone or using Xcelium utility (xfr)



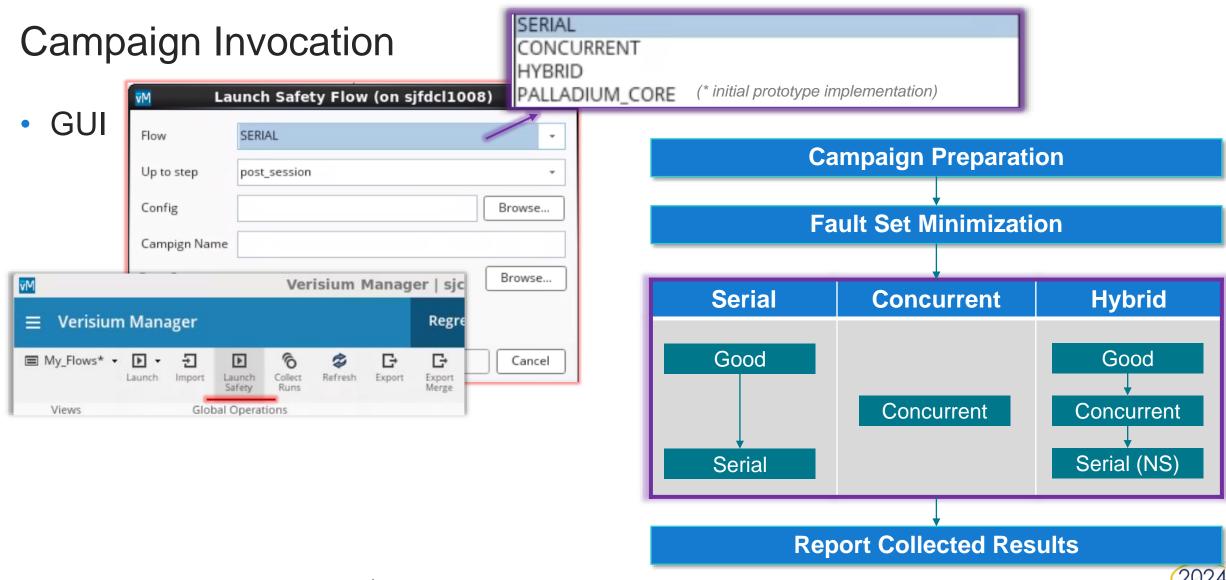
Palladium Safety Flow Overview





Fault Campaign Automation







Campaign Preparation

Organize Data

Campaign directory

Translate Inputs

• <u>User-input</u> (e.g., strobes)

strobe functional top.dut.o
strobe checker top.sm.alarm

Xcelium syntax

fs_strobe -functional top.dut.o
fs_strobe -checker top.sm.alarm

Jasper syntax

strobe functional dut.out strobe checker sm.alarm

Prune Tests (optional)

- Remove redundant tests
 - 0% additional coverage
- Order per cov/time
- Customizable heuristic
 - Coverage type and contribution threshold
- Permanent campaigns
 - Select functional tests





Analyze

Campaign Parameters

```
Fault spec.
fault target top... -type sa0+sa1
                                     Strobe list
strobe functional top.dut.o
strobe checker top.sm.alarm
                  Test List
session dv {};
Group tests {
                   xrun -64bit \
  test t1 : {};
                                       Sim script
  test t2 : {};
                     $FS SIM PARAM \
                                      Customizations
                                                     FS FAULT STOP SEVERITY
                                                     FS FAULT REDUCTION LEVEL
```

Configuration file

```
FS EXEC FAULT TYPE
                            : permanent
FS FAULT LIST FILE NAME
                            : .../faults.list
                            : .../strobes.list
FS STROBE LIST FILE NAME
FS SAMPLING PERCENT
FS SAMPLING ...
                            : .../tests.vsif
FS REGR TESTS VSIF
                            : .../sessions
FS TOP DIR
FS FAULT TOP
                            : tb.top
FS REGR TESTS REFINE
                              .../fsim.csv
FS FSIM SCRIPT
FS STROBE DEFAULT EVENT
FS FAULT INJECT CONDITION
FS ENABLE TEST SELECTION
                            : FALSE
```

Domain driven configuration



FMEDA Analysis



Verification **Environment**



Fault Set Minimization

Legend: - Mandatory parameters

- Midas overridden



Verisium Manager Safety

: 3

: FSV FST ONLY

: FSV FST ONLY

: unobservable

: FSV TC ONLY



FS FAULT RELATION LEVEL

FS FAULT PRUNING LEVEL

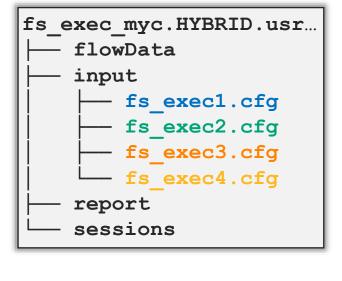
FS FAULT USE TEST CONST

FS FST SCRIPT

Campaign Configuration

Parameters override and traceability

```
fi_campaign -launch fi -flow_type CONCURRENT \
  -cfg master.cfg,project.cfg,activity.cfg,user.cfg
                                           User
                                                            User
              Project
                                                           Project
Master
                            Activity
                                                           Activity
                                                           Master
                                 Prepare
                                        Minimize
                                               Execute
                                                       Report
                                                               Analyze
```



Fault Set Minimization

Design Structure

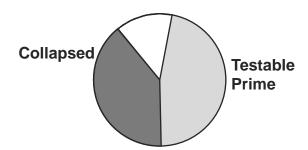
Testability Analysis

Identify faults:

- Uncontrollable
- Unobservable

Fault Collapsing

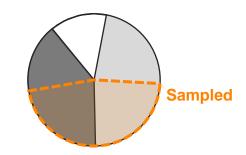
Group equivalent faults and consider only their <u>prime</u> representative



Statistics

Random Sampling

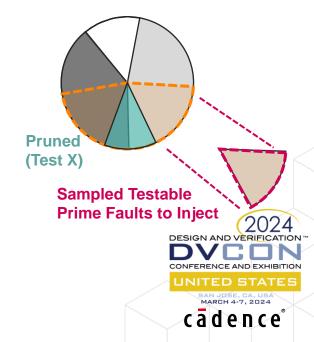
Estimate the overall results based on a representative sample



Test Stimulus

Fault Pruning

Find extra untestable faults by constraining testability based on stimulus patterns





Untestable

(Safe)

Testable

Statistical Sampling - Sample Size Calculation

Leveugle, R., Calvez, A., Maistri, P., & Vanhauwaert, P. (2009) Statistical fault injection: Quantified error and confidence. *2009 Design, Automation & Test in Europe Conference & Exhibition*, 502–506. https://doi.org/10.1109/DATE.2009.5090716

- ISO26262-11:2018 4.8.1 General Fault Injection
 - "NOTE 4 A sampling factor can be used to reduce the fault list if justified with respect to the specified purpose, confidence level, type/nature of the safety mechanism, selection criteria etc."
- Statistical Sampling
 - It allows selecting subset(s) to <u>estimate properties</u> of the population set
 - i.e., to estimate the "proportion" of faults that are covered (the campaign result)
 - The required <u>precision of the estimated result</u> defines the calculated sample size
 - i.e., the "confidence level" that the estimated "proportion" (result) is within the "error margin"
 - Note: current implementation assumes infinite population size (conservative) i.e., larger the "population", greater the sample size.

 Note: infinite vs. finite population size shows insignificant impact on the calculation of samples representing less than 5% of the population

Campaign Parameters	Conservative Recommendation	Typical values			
FS_SAMPLING_ERROR: 0.5 "error margin" percentage	Conservative/Tighter error margins (near 0%) are used when the estimated proportion gets closer to 100%	1	1	0.5	0.5
FS_SAMPLING_CONFIDENCE : 95 "confidence level" percentage	Conservative/High confidence levels (near 100%) increase sample size, but not as much as reducing error margin	95	99	95	99
FS_SAMPLING_PROPORTION : 50 "population proportion" or estimation			50	50	50
	Sample Size	9,604	16,588	38,415	66,349



Test Pruning & Ordering

e -name regr -cost cpu

- Optional selection of functional tests using toggle-coverage based heuristics
 - Suitable for permanent faults. Configurable coverage type and pruning cutpoint

1st Pruning

	Rank options: -entity top.pdtop.xess_top.i_xess_fpga.or1200_top.or1200_cpu -text -out_text /vols/vmanager_t2b/fer/ -name regr Rank metric elements: top/pdtop/xess_top/i_xess_fpga/or1200_top/or1200_cpu Cumulative covered (%): 164859/223419 (73.79%) Number of Optimized Runs: 2						rl	
	Name	regr(Rank)	delta_regr(Rank)	Index	Status	Duration (sec.)	Seed	1
-	<pre>/Risc_core_tests/fpu_test /Risc_core_tests/short_test /Risc_core_tests/medium_test</pre>	73.67% 73.79% 73.79%	73.67% 0.11% 0%	3 1 2	passed passed passed	26 14 23	143450035 -1285344334 861744621	<u> </u>

2nd Ordering

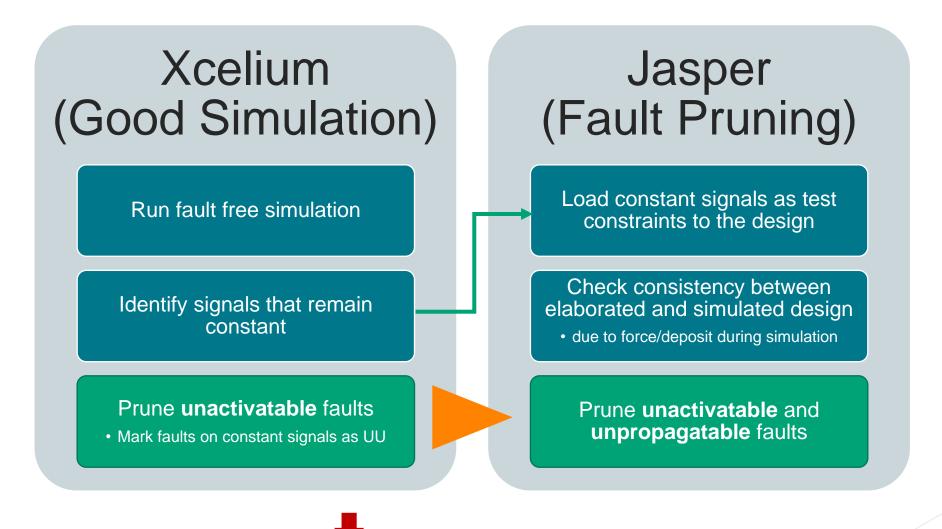
Rank options: -entity top.pdtop.xess top.i xess fpga.or1200 top.or1200 cpu -text -out text /vols/vmanager t2b/ferl





Fault Pruning





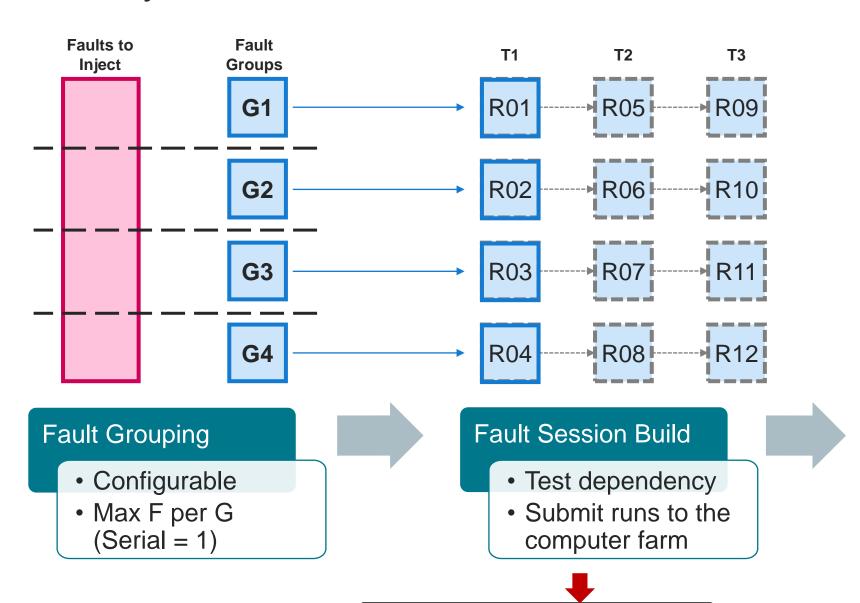




Prepare

Report

Fault Injection Execution



RUN XX

- 1. Filter Pruned Faults
- 2. Invoke Serial/Concurrent
 - 1.Inject fault/s
 - 2. Drop detected
 - 3. Stop simulation
- 3. Scan simulator logs
- 4. Remove dropped faults
 - 1. Skip next test if no left

Fault Run Execution

- Filter faults
- Check for errors
- Optimize runs



24 CATION



Analyze

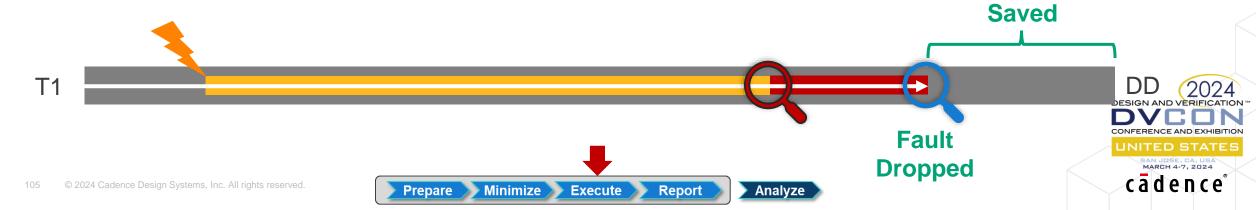
Fault Dropping

Fault injection
Checker Strobe
Functional Strobe
Test / Simulation

- Stopping simulating covered faults
- Without dropping



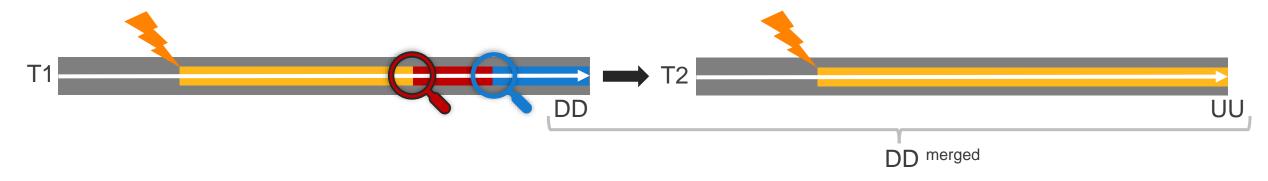
Optimized



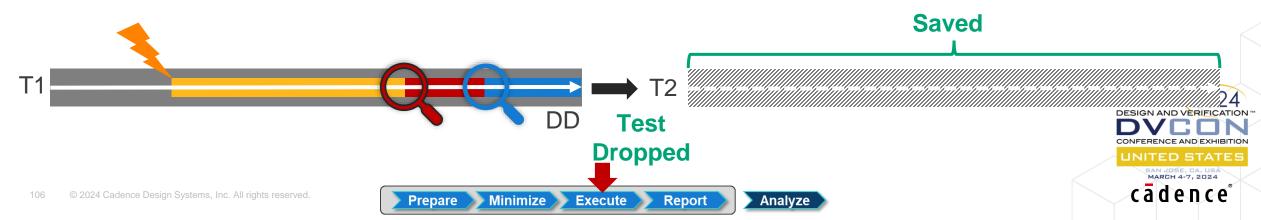
Test Dropping

Fault injection
Checker Strobe
Functional Strobe
Test / Simulation

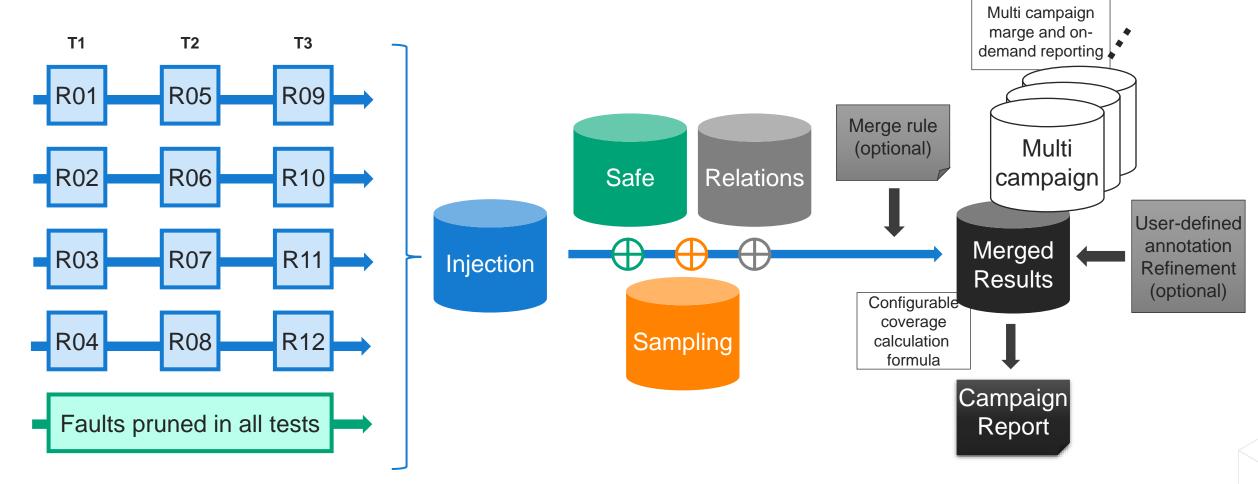
- Skip running already covered faults with subsequent tests
- Without dropping



Optimized



Reporting Campaign Results







Prepare

Minimize

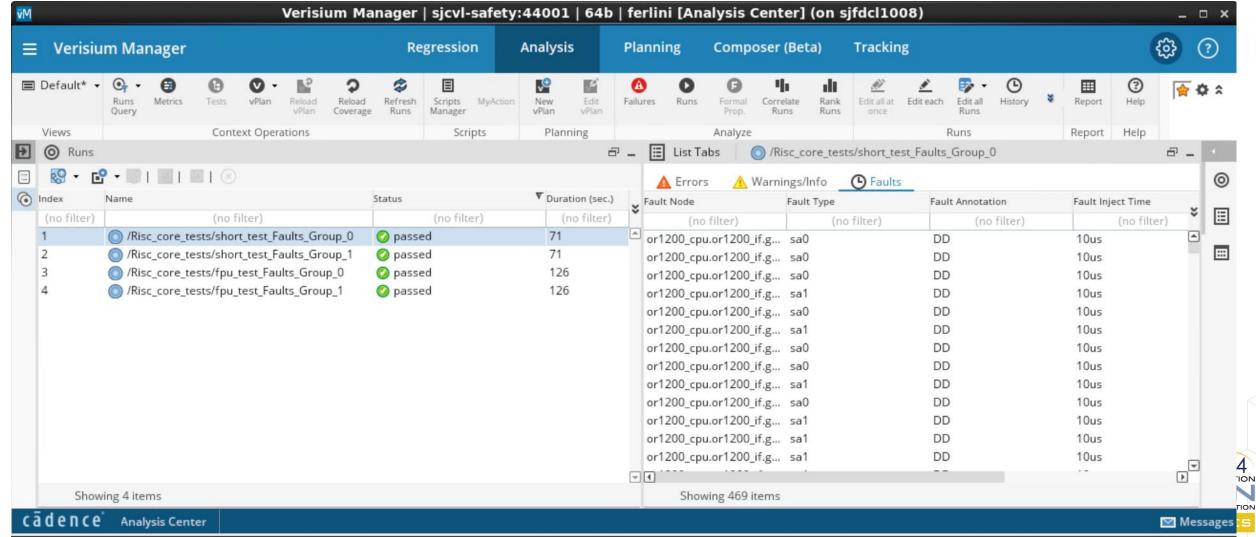


Fault Campaign Analysis



Fault Simulation Results

Run generated fault annotation



Minimize Execute

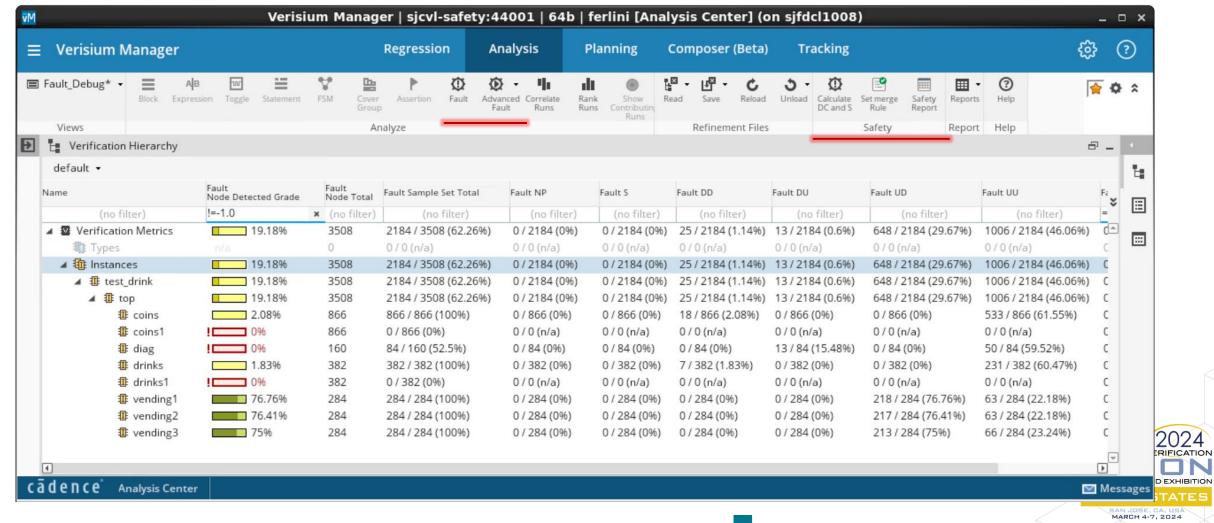
Prepare

Report

cādence

Fault Campaign Results - Hierarchical View

Merged annotation



Minimize 🔪

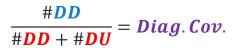
Prepare

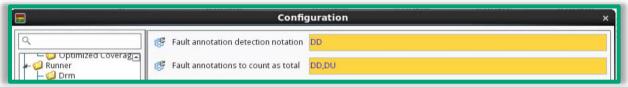
Execute

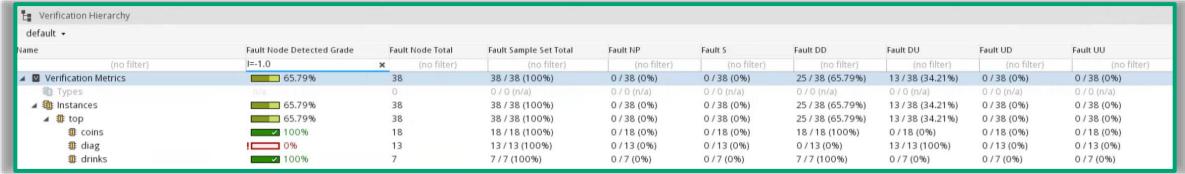
Report

cādence

Fault Campaign Analysis









$$\frac{\#DD + \#UD}{\#DD + \#UD + \#DU} = Custom\ Diag.\ Cov.$$

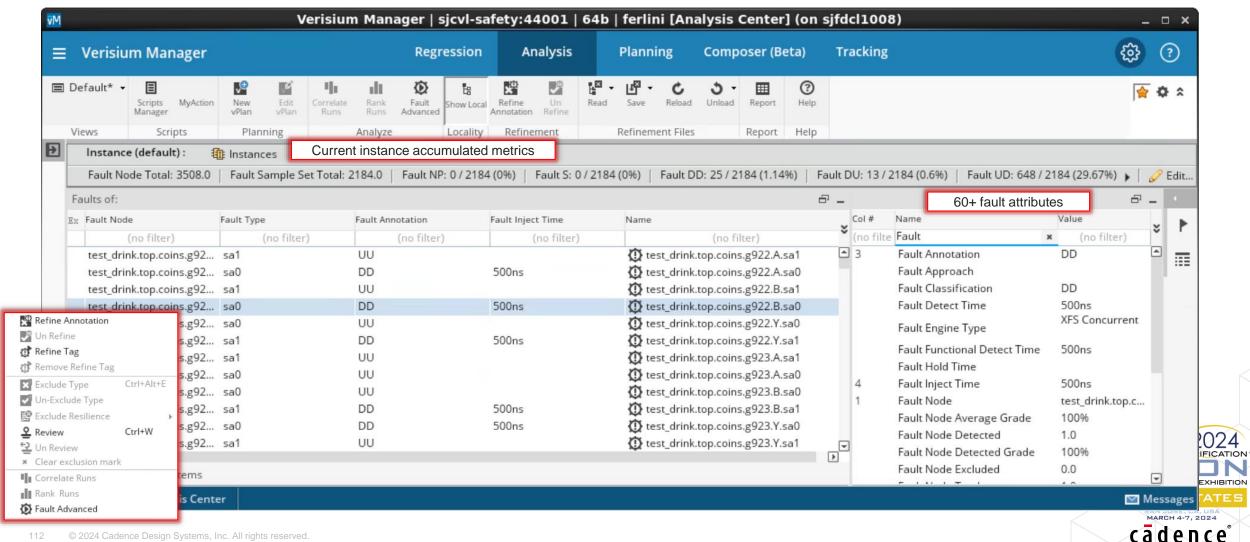
default -									
ame	Fault Node Detected Grade	Fault Node Total	Fault Sample Set Total	Fault NP	Fault S	Fault DD	Fault DU	Fault UD	Fault UU
(no filter)	I=-1.0	× (no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)
Verification Metrics	98.24%	737	737 / 737 (100%)	0 / 737 (0%)	0 / 737 (0%)	25 / 737 (3.39%)	13 / 737 (1.76%)	699 / 737 (94.84%)	0 / 737 (0%)
Types		0	0 / 0 (n/a)	0 / 0 (n/a)	0 / 0 (n/a)	0 / 0 (n/a)	0 / 0 (n/a)	0 / 0 (n/a)	0 / 0 (n/a)
■ Instances	98.24%	737	737 / 737 (100%)	0 / 737 (0%)	0 / 737 (0%)	25 / 737 (3.39%)	13 / 737 (1.76%)	699 / 737 (94.84%)	0 / 737 (0%)
■ III top	98.24%	737	737 / 737 (100%)	0 / 737 (0%)	0 / 737 (0%)	25 / 737 (3.39%)	13 / 737 (1.76%)	699 / 737 (94.84%)	0 / 737 (0%)
1 coins	✓ 100%	18	18/18 (100%)	0/18(0%)	0/18 (0%)	18 / 18 (100%)	0/18(0%)	0 / 18 (0%)	0 / 18 (0%)
	✓ 100%	18	18 / 18 (100%)	0 / 18 (0%)	0 / 18 (0%)	0 / 18 (0%)	0/18(0%)	18 / 18 (100%)	0 / 18 (0%)
diag	77.19%	57	57 / 57 (100%)	0 / 57 (0%)	0 / 57 (0%)	0 / 57 (0%)	13 / 57 (22.81%)	44 / 57 (77.19%)	0 / 57 (0%)
# drinks	✓ 100%	7	7 / 7 (100%)	0 / 7 (0%)	0 / 7 (0%)	7 / 7 (100%)	0/7(0%)	0 / 7 (0%)	0 / 7 (0%)
# drinks1	✓ 100%	7	7 / 7 (100%)	0 / 7 (0%)	0/7(0%)	0 / 7 (0%)	0 / 7 (0%)	7 / 7 (100%)	0/7(0%)
# vending1	✓ 100%	210	210 / 210 (100%)	0/210(0%)	0/210(0%)	0 / 210 (0%)	0/210(0%)	210/210 (100%)	0 / 210 (0%)
vending2	✓ 100%	210	210 / 210 (100%)	0 / 210 (0%)	0 / 210 (0%)	0 / 210 (0%)	0 / 210 (0%)	210 / 210 (100%)	0 / 210 (0%)
vending3	100%	210	210 / 210 (100%)	0 / 210 (0%)	0 / 210 (0%)	0 / 210 (0%)	0 / 210 (0%)	210 / 210 (100%)	0 / 210 (0%)

 $\frac{\#DD + \#UD}{\#DD + \#UD + \#DU} = Custom\ Diag.\ Cov.$

FERENCE AND EXHIBITION

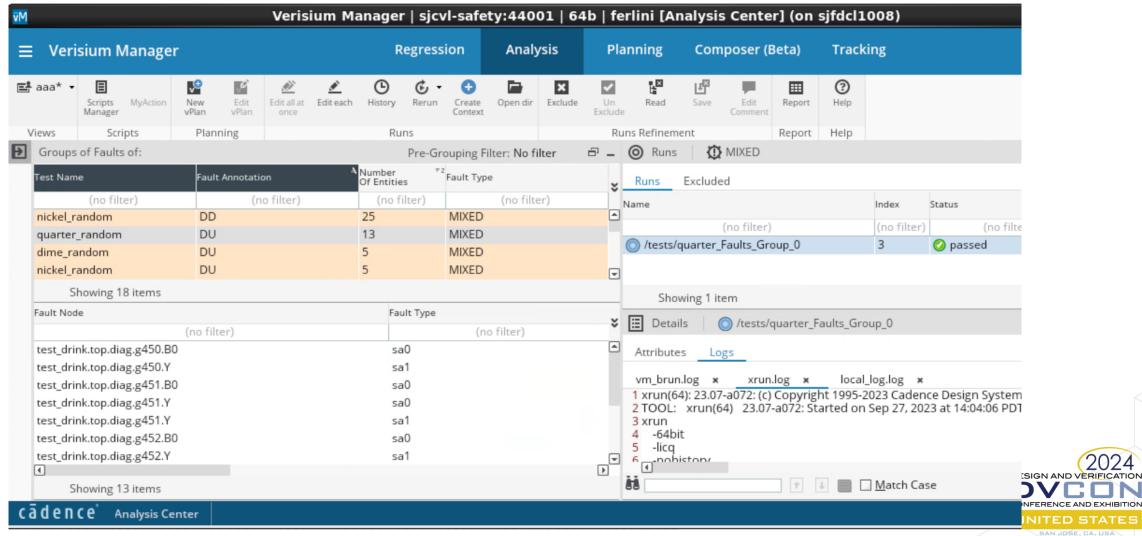
Fault Campaign Results – Annotated Fault List

Merged annotation



Fault Annotation Distribution per Test

Annotation per each test

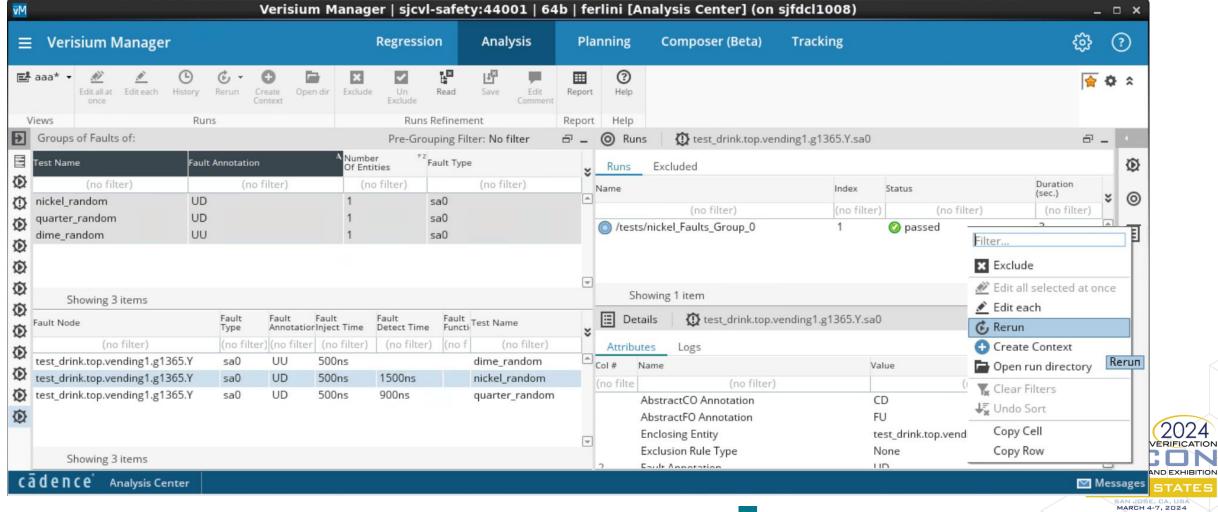


Prepare

cādence

Fault Annotation Traceability

Result per each test

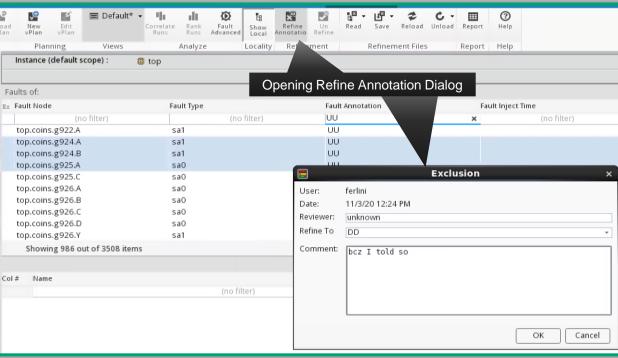


Minimize 🔪

cādence

Fault Annotation Refinement Dispositioning unclassified faults

GUI and CLI \rightarrow



```
vmanager> refine annotation -faults {top.vending1.\current state reg\[3\] } \
             -fault type SEU -refineTo S -comment {bcz I want}
A total of 8 faults were refined to S
vmanager> save -refinement fcm refinement.vRefine
vmanager> fi campaign -report -overwrite -output fcm refined report
Writing report to: fcm refined report/faultsim stat summary.report
```



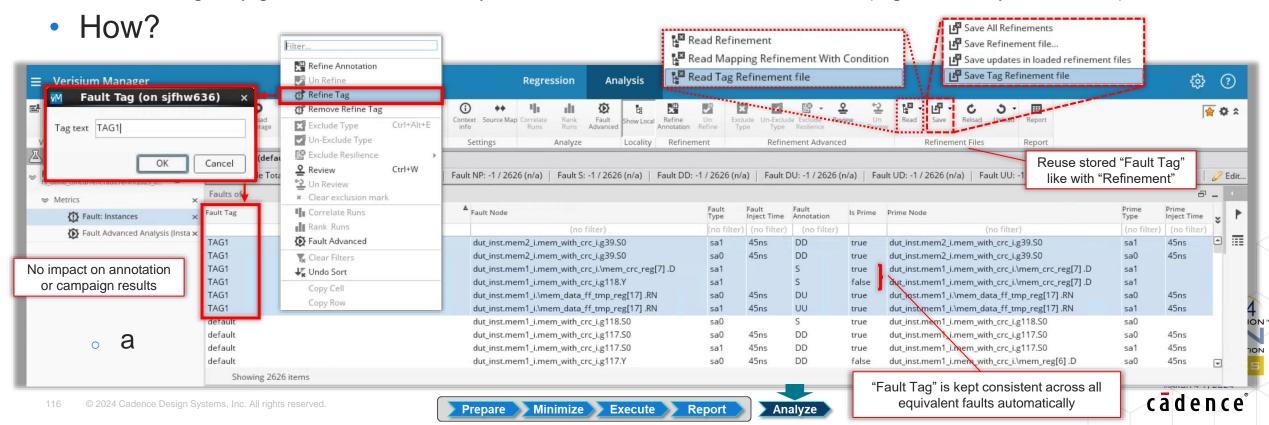
						Sample		-			
	INSTRUMENTATION	#	%	#	%	#	왕	#	%		
	Faults	2626		2546		484		465			
	Safe	1658	63.14	1658	65.12	0	0.00	0	0.00		
4	Not Injected	479	18.24	458	17.99	35	7.23	35	7.53		
7	Injected	489	18.62	430	16.89	449	92.77	430	92.47		
п	CLASSIFICATION	#	%	#	%	#	%	#	%		
ш	Fault Annotations	2626		2546		484		465			
п	SAFE	S 1666	63.44	1666	65.44	8	1.65	8	1.72		
п	DANGEROUS DETECTED	DD 362	13.79	303	11.90	322	66.53	303	65.16		
П	DANGEROUS UNDETECTED	DU 123	4.68	123	4.83	123	25.41	123	26.45		
п	Not Classified	475	18.09	454	17.83	31	6.40	31	6.67		
	UNOBSERVED DETECTED	UD 0	0.00	0	0.00	0	0.00	0	0.00		
-	UNOBSERVED UNDETECTED	UU 211	8.04	199	7.82	31	6.40	31	6.67		
п	NOT SIMULATABLE	NS 0	0.00	0	0.00	0	0.00	0	0.00		
М	INJECTION FAILED	IF 0	0.00	0	0.00	0	0.00	0	0.00		
11	NOT PROCESSED	NP 101	3.85	92	3.61	0	0.00	0	0.00		
Ш	Others	163		163	6.40	0	0.00	0	0.00		
Ш	REFINEMENT	#				#					
Ш	To S	8				8					
ш	From UU	4				4					
ш	From DU	3				3					
п	From DD	1				1					
	METRICS		%				%				
	Fault Coverage		16.83				71.08				
	Test Coverage		74.64				72.36				
	PARAMETERS										
4	Fault Coverage : 100 * (DI	D + D) / (DD -	+ DU + S	S + D + U +	+ P + U+	-U + U+D)					
	Test Coverage : 100 * (DI	O + D) / (DD -	+ DU + D) + U + P)							
	Merge File : default										
	Refinement : /vols/vmanager_t2b/ferlini/activities/2022/FCM_tech_up_22.09/refine2.vRefine										



Report

Fault Tagging

- What?
 - User-editable (string) attribute per fault metric element
- Why?
 - Support post-campaign analysis (debug, refinement, etc.) by tagging relevant faults
 - Logically gather faults even if they do not share a common attribute value (e.g., hierarchy, annotation)



Scripted Annotation Refinement Leveraging Fault Tagging

Load fault session and apply tags

```
vmanager> load fs demo concurrent.fault.ferlini.2023 01 20 09 04 38
                                                                                                                               Note: Wildcard '*' is supported in -faults <value>
vmanager> refine tag -faults {dut inst.mem2 i.mem with crc i.g39.S0} -refineTo TAG1
vmanager> refine_tag -faults {dut_inst.mem1_i.\\mem_data_ff_tmp_reg\[17] .RN} -refineTo TAG1
vmanager> refine tag -faults {dut inst.mem1 i.mem with crc i.\mem crc reg\[7] .D} -fault type sa1 -refineTo TAG1
                                                                                                                                  Fault Tag, Fault Annotation, Fault Type, Fault Node, Fault Inject Time
                                                                                                                                  TAG1, S, sa1, dut_inst.mem1_i.mem_with_crc_i.\mem_crc_reg[7] .D,
      Save tags (e.g., open in GUI)
                                                                                                                                  TAG1, S, sa1, dut inst.mem1 i.mem with crc i.g118.Y,
                                                                                                                                  TAG1, DU, sa0, dut_inst.mem1_i.\mem_data_ff_tmp_reg[17] .RN, 45ns
                 Optional – export filtered CSV
                                                                                                                                  TAG1, UU, sa1, dut inst.mem1 i.\mem data ff tmp reg[17] .RN, 45ns
                                                                                                                                  TAG1,DD,sa0,dut inst.mem2 i.mem with crc i.g39.S0,45ns
                                                                                                                                  TAG1,DD,sa1,dut inst.mem2 i.mem with crc i.g39.S0,45ns
vmanager> save -fault tag -refinement tech up cli.vRefineTag
vmanager> csv_export -metrics -fault -filter {fault_tag:==TAG1} -view MY -inst ... -out red.csv
                                                                                                                                  Fault Tag, Fault Annotation, Fault Type, Fault Node, Fault Inject Time
                                                                                                                                  TAG1, S, sa1, dut inst. mem1 i.mem with crc i. \mem crc reg[7] .D,
             Tag-based annotation refinement
                                                                                                                                  TAG1, S, sa1, dut inst.mem1 i.mem with crc i.g118.Y,
                                                                                                                                  TAG1, S, sa0, dut inst.mem1 i.\mem data ff tmp reg[17] .RN, 45ns

    Optional – export filtered CSV

                                                                                                                                  TAG1, S, sa1, dut inst.mem1 i.\mem data ff tmp reg[17] .RN, 45ns
                                                                                                                                  TAG1, S, sa0, dut_inst.mem2_i.mem_with_crc_i.g39.S0,45ns
                                                                                                                                  TAG1, S, sa1, dut_inst.mem2_i.mem_with_crc_i.g39.S0,45ns
vmanager> refine annotation -tag name TAG1 -refineTo S -comment {bcz...}
vmanager> csv export -metrics -fault -filter {fault tag:==TAG1} -view CLI -inst ... -out blue.csv
                                                                                                   ----- #
                                                                                                   To S
```

- Generate updated summary
 - Must save refinement

```
vmanager> save -refinement tag based.vRefine
vmanager> fi campaign -report -summary -output refined_summary_rpt
```

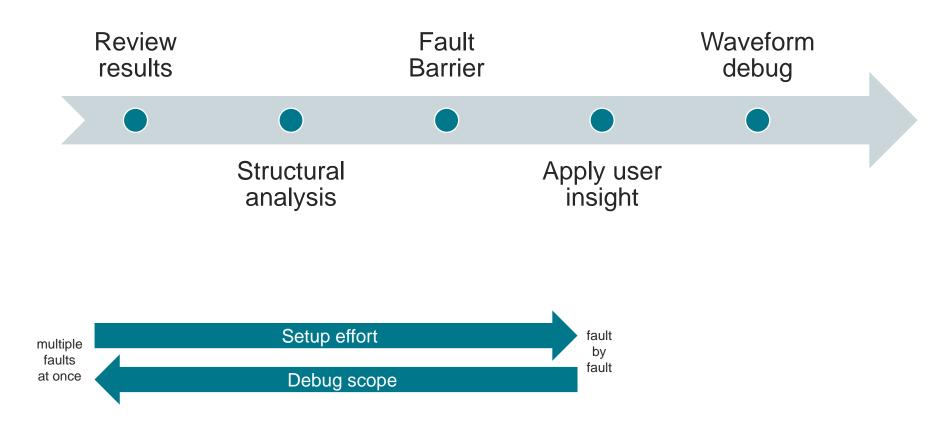
```
From DD
 From UU
 From DU
      ----- MFTRTCS ---- %
Fault Coverage
Test Coverage
                                      71.44
Fault Coverage : 100 * (DD + D) / (DD + DU + S + D + U + P + U+U + U+D)
Test Coverage
             : 100 * (DD + D) / (DD + DU + D + U + P)
              : default
Merge File
Refinement
               : tag based.vRefine
```



Fault Campaign Debug



Fault Campaign Closure



GOAL:
minimize and
guide the
effort towards
DC closure



Approach 1 – Fault Analysis to Improve Tests

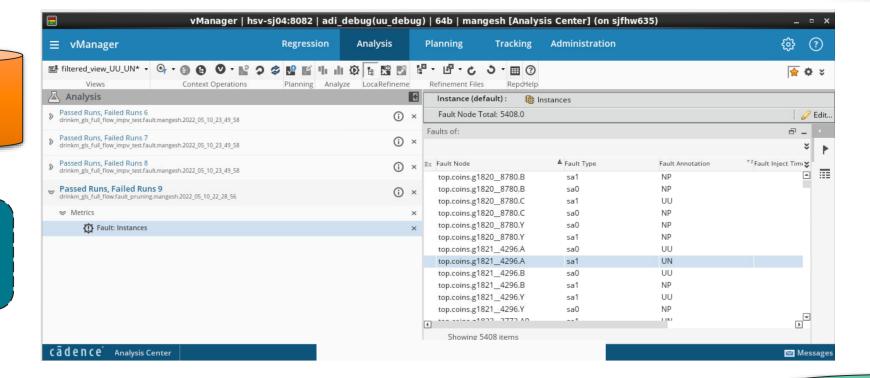
Configuration Superset

Reference Fault Campaign with FST,FSV TC Enabled in Verisium[™] Manager Safety

Reference Fault Campaign Results

Metrics, Report Analysis

Hierarchical, Filtering, Test Analysis, Report Reviews



Configuration With new tests

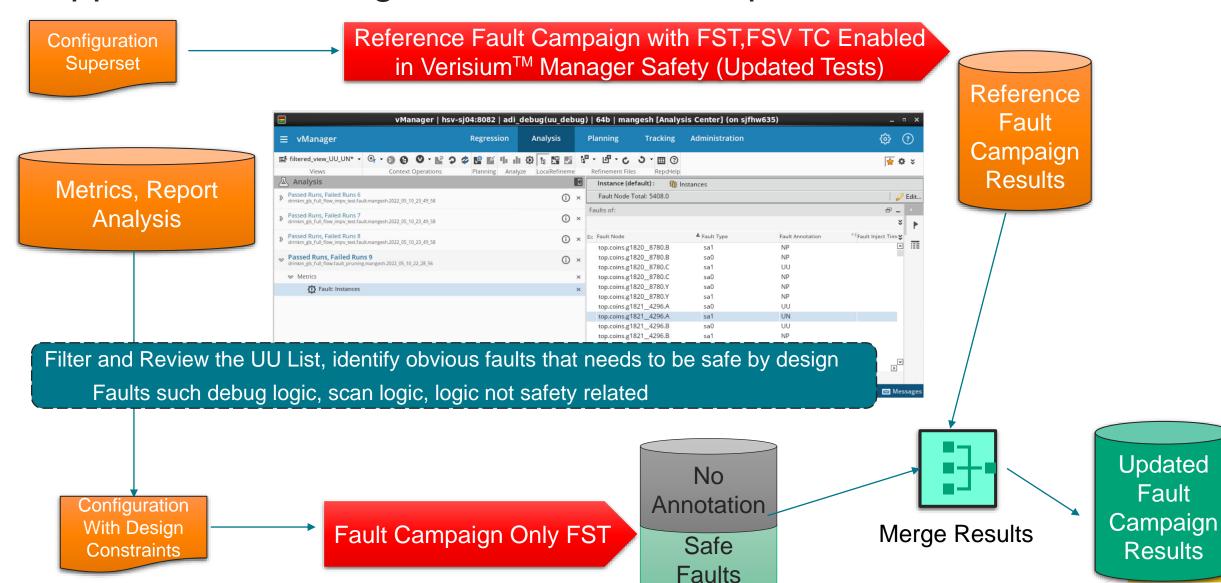
Updated tests based Fault Campaign with FST,FSV TC Enabled in vManager Safety

Updated Fault
Campaign Results

Add additional tests, modify tests to cover the UU Faults

cadence

Approach 2 – Design Constraints to Jasper FSV

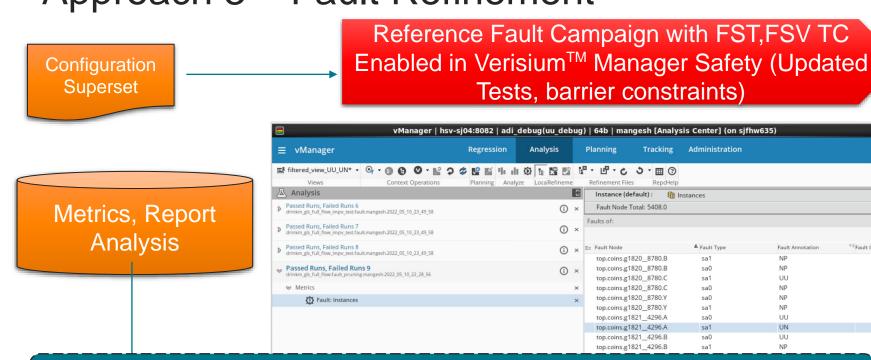


Fault

Results

cadence

Approach 3 – Fault Refinement



Reference Fault Campaign Results

(2)

<u>♠</u> ❖ ×

✓ Message

Filter and Review the UU List. Identify Flip Flops (Barrier Points).

Configuration
With Barrier Tcl
and UU Fault List
from Reference
Campaign

Identify faults belonging exclusively to the fan-in of given FFs

Fault Campaign Only FST

No Annotation Safe Faults



Refinement TCL



Approach 4 – Enable Formal

Configuration Superset

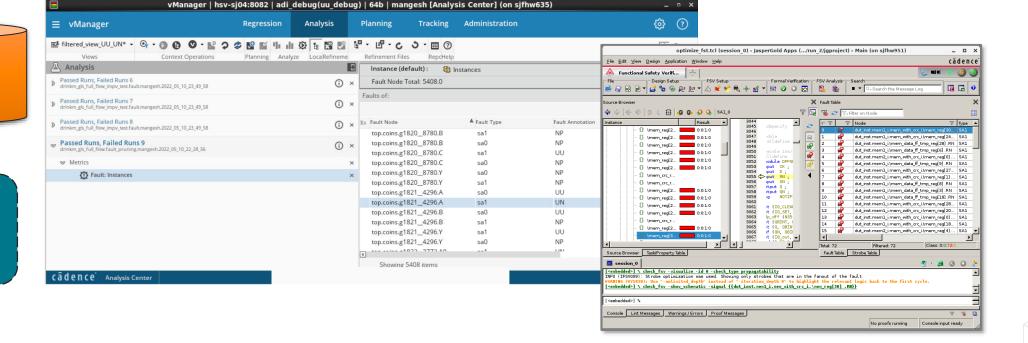
Available Reference Fault Campaign till FST in Verisium[™] Manager Safety (Updated Tests, Constraints)

Reference Fault Campaign Results

Metrics, Report Analysis

> Filter and Review the UU List

> > Configuration

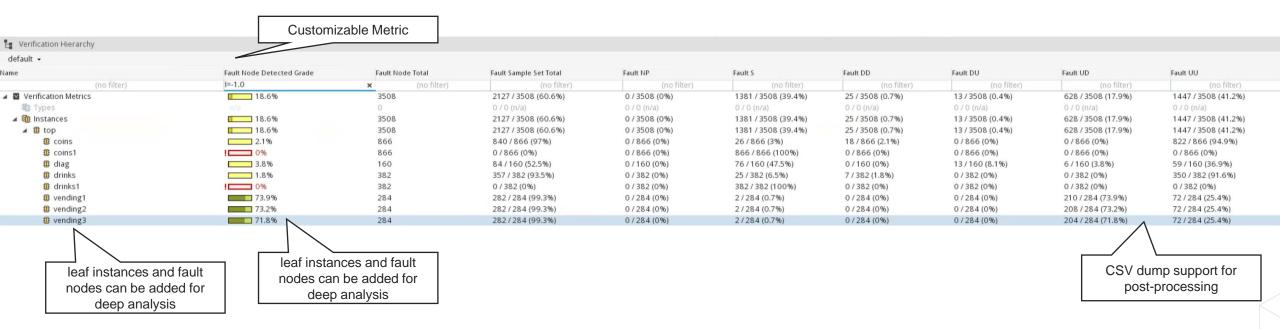


Rerun FST or Incremental Campaign with updated Fault List to invoke JG-FSV GUI

Debug Analysis, Safeness Annotation Refinement File

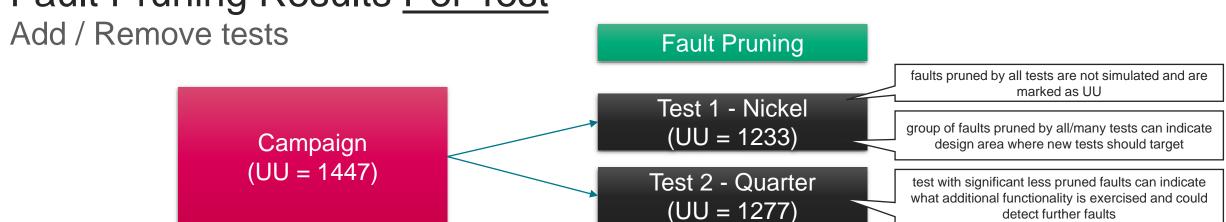
Fault Metric Analysis

- Customizable grade calculation
- Hierarchical results

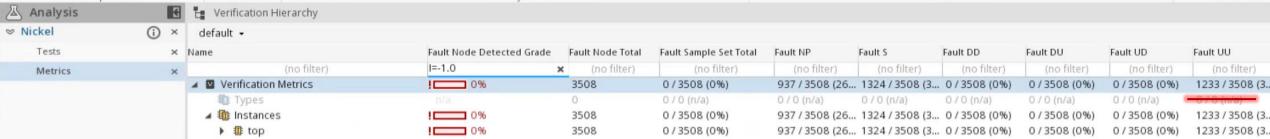




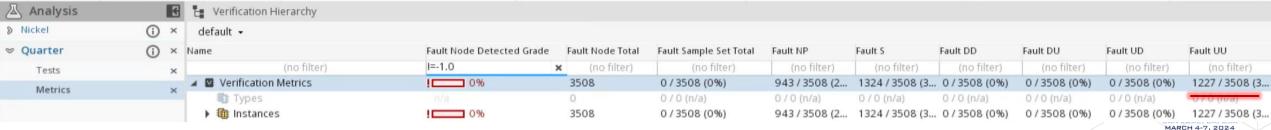
Fault Pruning Results Per Test



Test 1 - Nickel



Test 2 - Quarter



Individual Annotation Contribution of Each Test

Advanced Fault Analysis

Results grouped by Test and Fault Classification

Test 1 - Nickel DD: 25

Test 2 - Quarter

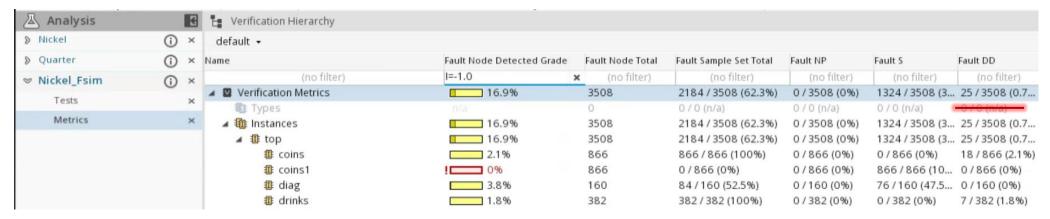
DD: 0??

Groups of Faults of:				Pre-Grouping Filter: No filter	ð -
Test Name	A Fault Classification	Fault Annotation	^{△2} Number Of Entities	^{▼3} Fault Type	
(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	1
	S	S	1783	MIXED	E.
nickel_random	DD	DD	25	MIXED	
nickel_random	DU	DU	13	MIXED	
nickel_random	S	S	296	MIXED	
nickel_random	NC	MIXED	2663	MIXED	
quarter_random	DU	DU	8	MIXED	
quarter_random	S	S	296	MIXED	
quarter_random	NC	MIXED	3091	MIXED	
Showing 8 items					
Fault Node	Fault Type	Fault Annotation	n ≜ Fai	ult Inject Time	
(no filter)	(no fi		×	(no filter)	
top.drinks.g214.D	sa0	UU			
top.drinks.g644.A0	saO	UU	50	00ns	
top.coins.\nickel_count_reg[6].Q	saO	UU			
top.coins.g2422.B0	sa1	UU			
top.coins.g2441.Y	sa1	UU			
top.coins.\nickel_count_reg[6] .D	sa0	UU			
top.vending3.g1349.B0	sa1	UU	50	00ns	
top.drinks.g644.A0	sa1	UU			
top.coins.g2360.A0	sa1	UU			
top.coins.g2422.C0	sa1	UU			
top.drinks.g643.B0	sa0	UU			
top.coins.\nickel_count_reg[5] .Q	sa0	UU			
top.coins.g2422.Y	sa0	UU	50	00ns	
top.drinks.g215.A	saO	UU			
top.coins.\nickel_count_reg[5] .D	sa0	UU			
top.coins.g2441.Y	sa0	UU	50	00ns	
					4-7, 20
ed.				\sim	eu (

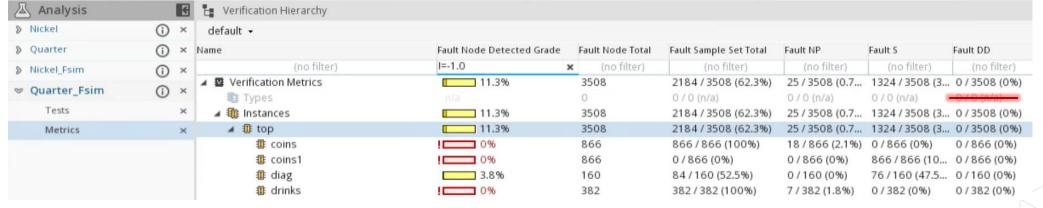
Fault Merged Annotation Per Each Test

Add / Remove tests

Test 1 – Nickel



Test 2 - Quarter





Functional Safety Flow: Barrier Analysis Details



- Barrier Analysis executed on UU Faults to debug/identify block points
- Xcelium Safety supports barrier Analysis "-fault_barrier" switch to dump the data in Fault DB for every **Fault Simulation**
- Cadence developed Python utility is executed on fault_db to generate two files faults.csv and barrier.csv
 - barrier.csv -> captures the barriers and the associated blocked faults
 - contains the instance; file name and line number of the code which block the fault propagation
 - faults.csv -> contains fault set and associated barriers for each of the fault nodes
- **Snippet of barriers.csv (Barrier to Fault Relation)**

```
Barrier ID, Barrier Node, FanIn Strength, Faults
1, test_drink.top.coins.g1824__4547.Y, 2, {1 2}
2, test_drink.top.coins.g1823__1474.Y, 2, {1 2}
3, test_drink.top.coins.g1822__3772.Y,2,{1 2}
4, test_drink.top.coins.g2634__7675.C0,1,{2}
5, test_drink.top.coins.g2588 1474.Y,1,{2}
```

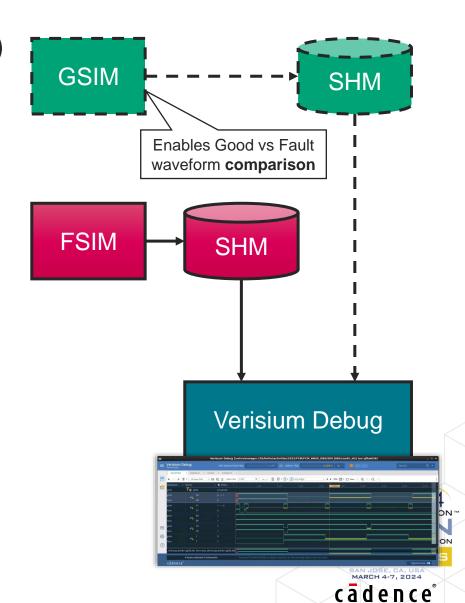
Snippet of faults.csv (Faults to Barrier Mapping)

Fault ID, Fault Node, Fault Type, Fault Injection Time, FanOut Strength, Barriers 1, test_drink.top.coins.RC_CG_HIER_INST1.RC_CGIC_INST.E, SA1, 402NS, 3, {1 2 3} 2, test_drink.top.coins.RC_CG_HIER_INST1.RC_CGIC_INST.ECK, SA1, 402NS, 5, {1 2 3 4



Waveform Generation

- 1. Good Simulation Waveform Generation (Xcelium)
 - Optional Allows good vs fault waveform comparison
 - Concurrent
 - Note: probing signals is applicable to the good simulation by default
- 2. Fault Simulation Waveform Generation (Xcelium)
 - Serial
 - standard Xcelium probing mechanism
 - Concurrent
 - Enabled by -fault_dump_shm <id>
 - <id> is the fault id according to the injection order of the given run
 - i.e., 1st injected faults has id = 1, 2nd injected fault has id = 2...
 - Recommendation: only keep the fault being debug
- 3. Waveform Visualization (Verisium Debug)
 - Good vs Fault Waveform comparison



Rerun vs Incremental

Rerun

- Rerun (e.g., debug/exploration) data is mixed with original campaign data (
- Risk: override valid results (unaffordable rerun to recover valid data)
- Recommended when original data is invalid/unavailable

Incremental

- Separate set of data. Independent original and incremental analysis/results
- Original and Incremental results can be analysed/reported independently or merged
- Native support of fault sub-set selection based on its metrics (e.g., annotation)
 - Avoid reruns by skip already available optimisations results (e.g., analyzing UUs)
- Flow type change support (e.g., concurrent → serial)
- Support analysing faults sub-set with different stimulus

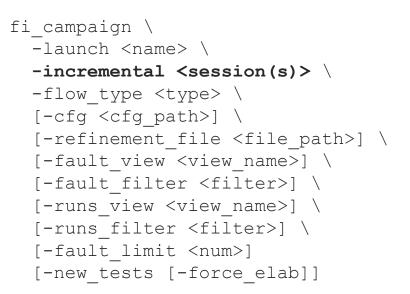


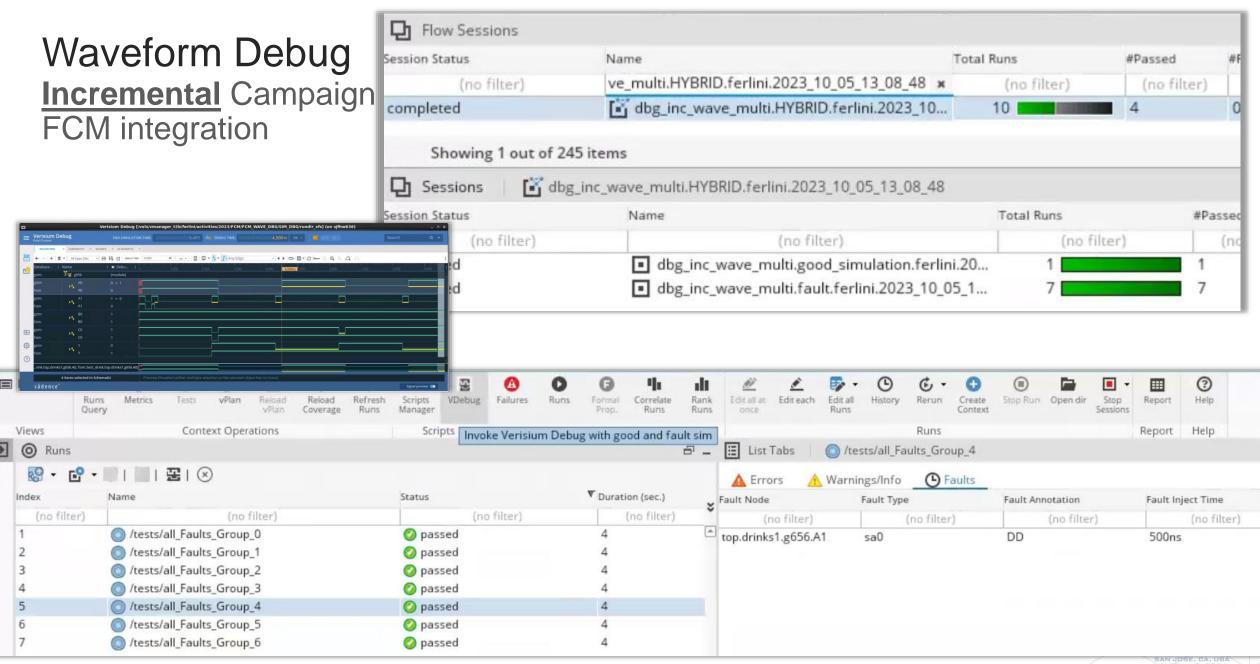
Fault Sub-Set Selection

Incremental campaign

- -fault_filter "attribute:value"
 - Select faults based on their attribute (e.g., annotation)
- -fault_limit <number>
 - Used to limit the number of selected faults for incremental campaign
- -runs_filter "attribute:value"
 - Selecting faults from specified runs of source campaign
 - E.g. –runs_filter "test_name:<run(s)_to_debug>"
- -fault_view / -runs_view
 - Instead of specifying the filters in batch, user can create filters via GUI and save the view
 - E.g. –fault_view "my_view_with_filters"
- -refinement_file "path/to/file.vRefine"
 - Used to apply user refinement on source campaign results, before applying the filters

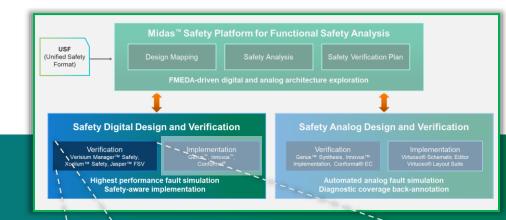
	y		_		_			
Fault Node Total: 3508.0		Fault NP: 0 / 3508 (0%)	Fault S: 1324 / 3508 (37.74%)	Fault DD: 25 / 3508 (0.71%)	Fault DU: 13 / 3508 (0.37%)	Fault UD: 600 / 3508 (17.1%)	Fault UU: 1546 / 3	508 (44.07%)
Faults of:								
g _x Fault Tag	Fault Node		Fault Type	Fault Annotation	Fault Inject Time	Fault Engine Type	Is Prime	Is Sampled
(no filter)		(no filter)	(no filter)	(no filter)	(no filter)	(no filter)		(no fil
default	test_drink.top.coins.g922.A		sa1	UU	500ns	XFS Concurrent	true	true
default	test_drink.top.coins.g922.A		sa0	DD	500ns	XFS Concurrent	false	true
DBG	test_drink.top.coins.g922.Y		sa0	UU	500ns	XFS Concurrent	true	true
default	test_drink.top.coins.g922.Y		sa1	DD	500ns	XFS Concurrent	true	true
DBG	test_drink.top.coins.g922.B		sa1	UU	500ns	XFS Concurrent	true	true
default	test_drink.top.coins.g922.B		sa0	DD	500ns	XFS Concurrent	false	true
DBG	test_drink.top.coins.g923.A		sa1	UU	500ns	XFS Concurrent	true	true
default	test_drink.top.coins.g923.A		sa0	UU	500ns	XFS Concurrent	false	true
default	test_drink.top.coins.g923.Y		sa0	DD	500ns	XFS Concurrent	true	true

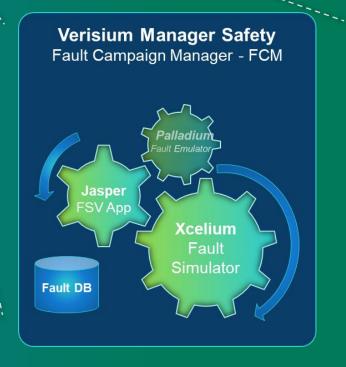




Digital Safety Verification Summary

- ✓ Fault Campaign Automation
 - Same verification environment (Verisium Manager add-on)
 - Single front-end campaign configuration
 - Jasper and both Xcelium fault engines orchestration
 - ✓ Data exchange via the proprietary unified fault database
 - Dedicated fault coverage analysis (GUI and reports)
- ✓ Multi-Domain Fault Analysis support
 - Permanent and Transient fault campaigns
 - Diagnostic Coverage and Safeness
 - ✓ Software-based Self-Test Library (STL) assessment
 - ✓ Safety Mechanism (integration) Verification (+Detection Time Interval)
 - Fault / Test Grading (DFT) + Architectural Vulnerability (RadHard)
- ✓ ISO26262 tool qualification up to ASIL D





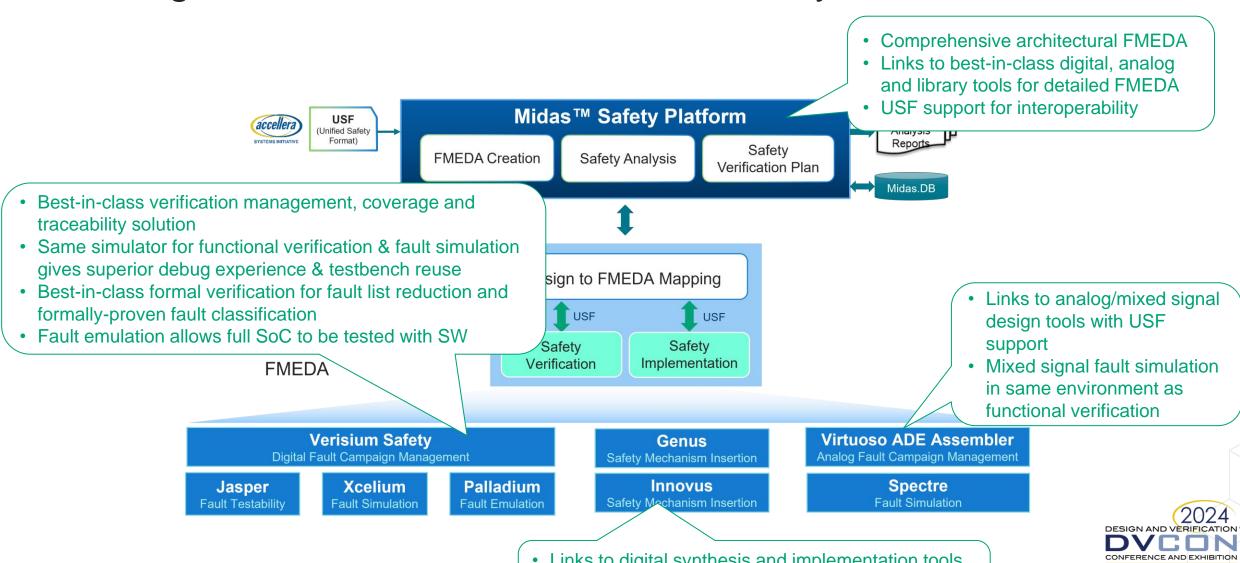




Summary



Advantages of the Cadence Functional Safety Solution



- Links to digital synthesis and implementation tools with USF support
- Best-in-class RTL/gate/netlist equivalence checking

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