CONFERENCE AND EXHIBITION

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Systematic Constraint Relaxation (SCR): Hunting for Over-Constrained Stimulus

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Introduction

- System Verilog Constraint Solver
 - Facilitates development of random tests
 - Constraints carve out feasible space stimulus that DUT can support
- Possible Root Causes of Overconstraints
 - Temporary Constraints added to mask out known design/checker issues
 - Incorrect Understanding of specification
 - Change in specifications not reflected in constraints
- Why over-constraints are bad?!
 - Coverage Loss and possible bug escapes
 - Can silently degrade the quality of stimulus







Prior Work

- No prior published work on automatically identifying over-constraints
- Standard Approach in Industry : Coverage Analysis
- Why Coverage Analysis is not sufficient?
 - Common mode misunderstanding in writing illegal bins
 - Does not directly point towards an over-constraint
 - Human in loop debug effort





Simple Analysis



(Summary) Relax L_i and generate P: $P \notin F$ and S==PASS => $P \in R \Rightarrow L_i$ is over-constrained











SCR – Constraint Splitting Demo







Results

- Ran 300 tests on Integration TB after script modified the constraints
- 22 cases of overconstraints were identified by the SCR
- 19/22 cases did not cause coverage loss
- 3/22 cases were overconstraints causing coverage loss

Example of over-constraint not leading to coverage loss

ID	Fields							
ID1	F1	F2		0	F3	F4		F5
ID2	F1	F6		F7		F8	F9	F5

```
Constraint c1{
F3 inside [x, y, z];
}
Constraint c1{
ID==ID1 -> F3 inside [x, y, z];
}
```





Conclusion

- Shows potential to quickly and automatically identify over-constraints
- Can identify redundant constraints leading to loss of simulation performance
- Limitations:
 - It is not guaranteed to find all over-constraint
 - Cannot find duplicated over-constraints



