2022 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

SAN JOSE, CA, USA
FEBRUARY 28 - MARCH 3, 2022

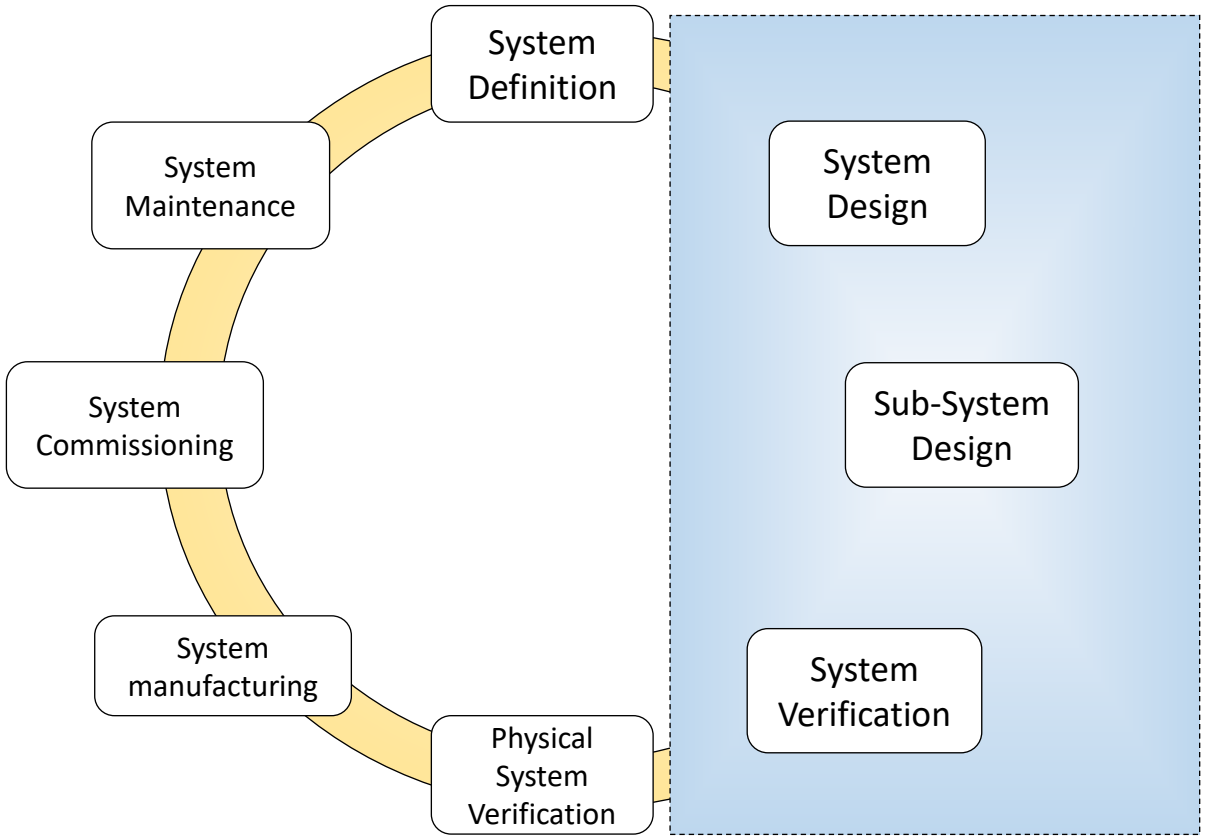
SystemC Virtual Prototype: Ride the earliest train for Time-to-Market!

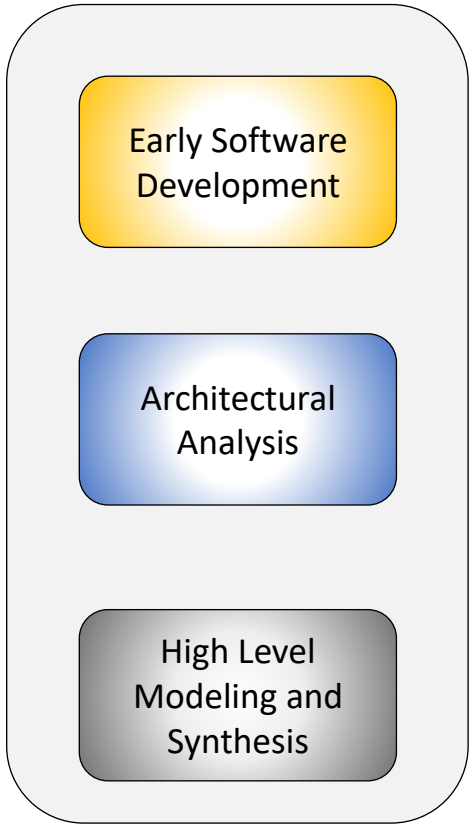
Shweta Saxena, Mahantesh Danagouda

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

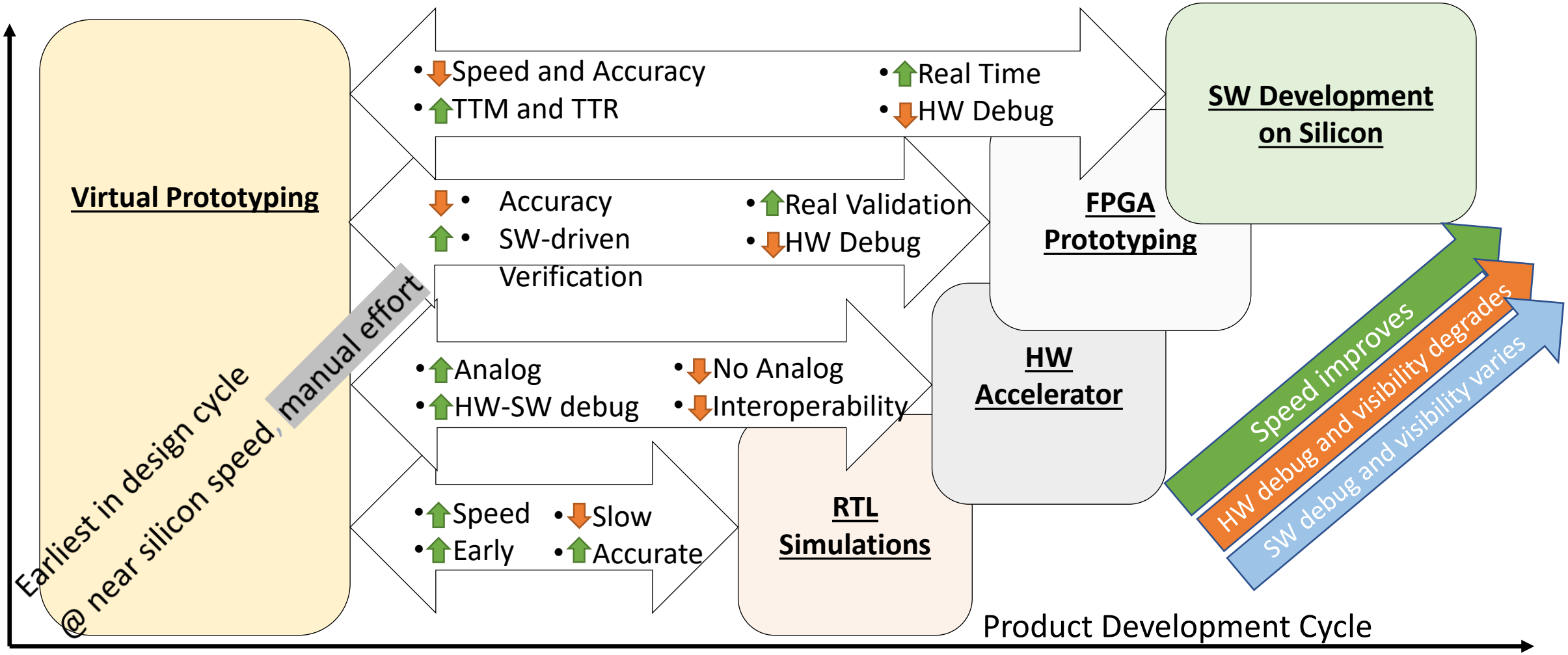
accellera
SYSTEMS INITIATIVE

System Virtual Prototyping





Review of SW Development Methodologies



Problem Statement

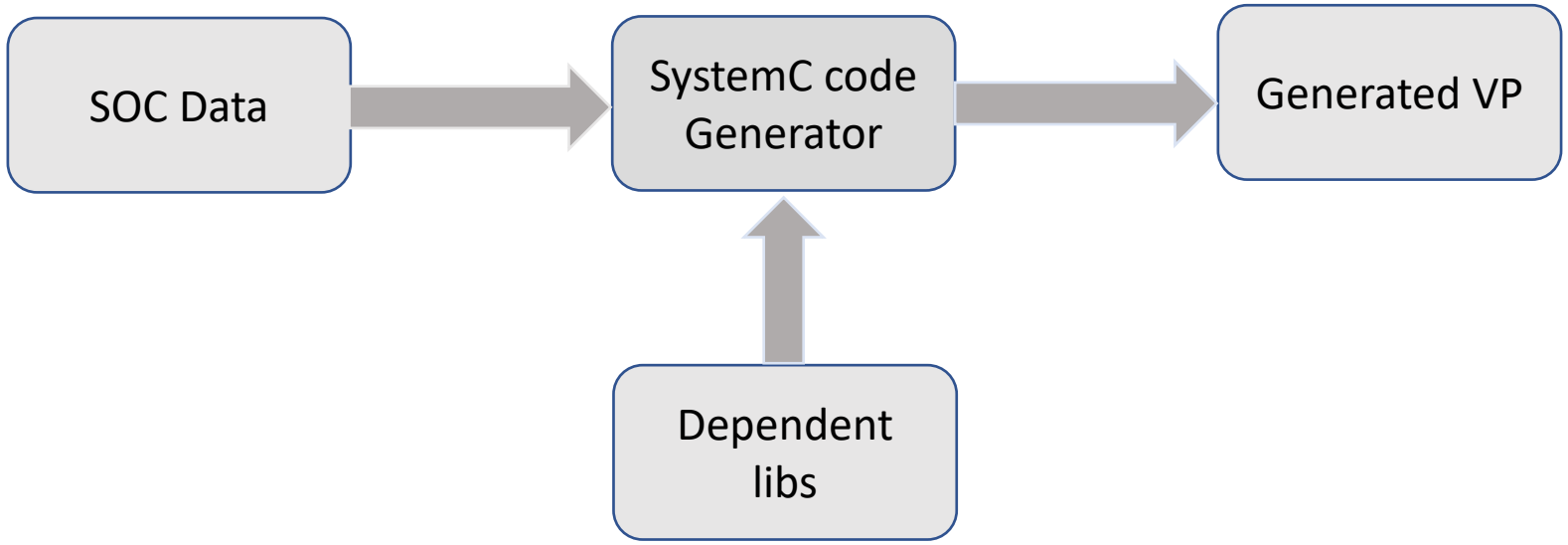
Software development challenges

- Time and effort is invested in HDS development(3-4 months).
- Blocked for validation until FPGA is set up, losing initial project time.
- Limited boards available.

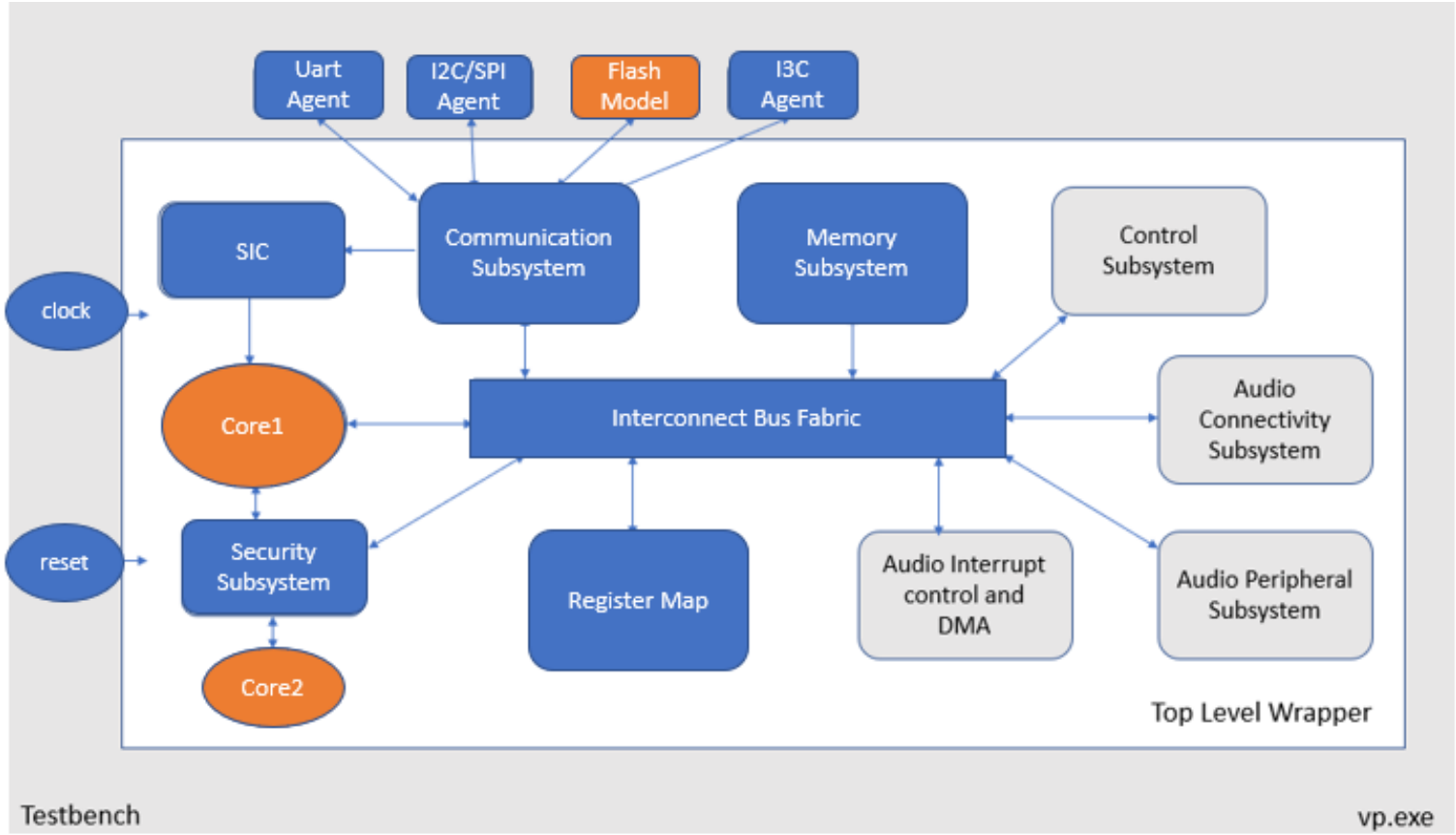
Software validation challenges

- UVM/System Verilog code difficult to navigate.
- No straightforward re-usability.

Our solution : Virtual Prototype(VP)



Inside the Virtual Prototype

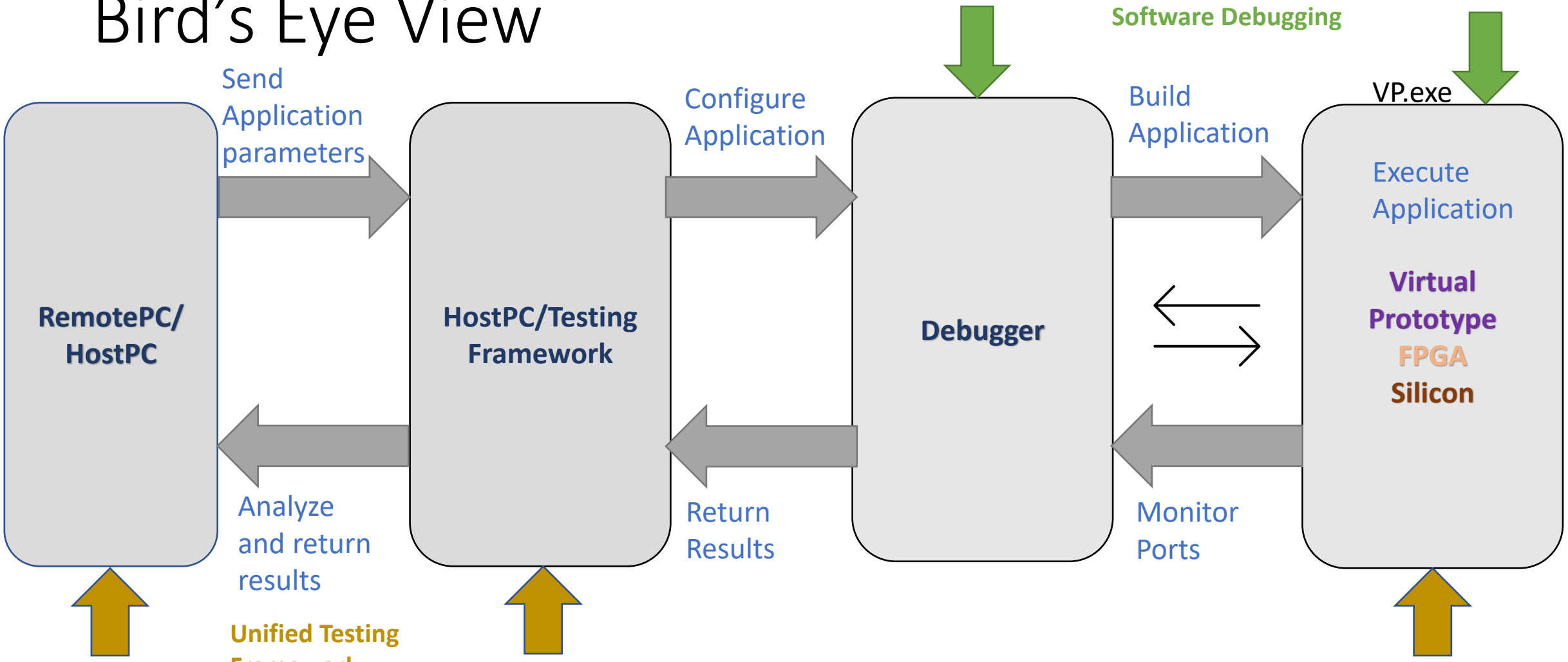


Model

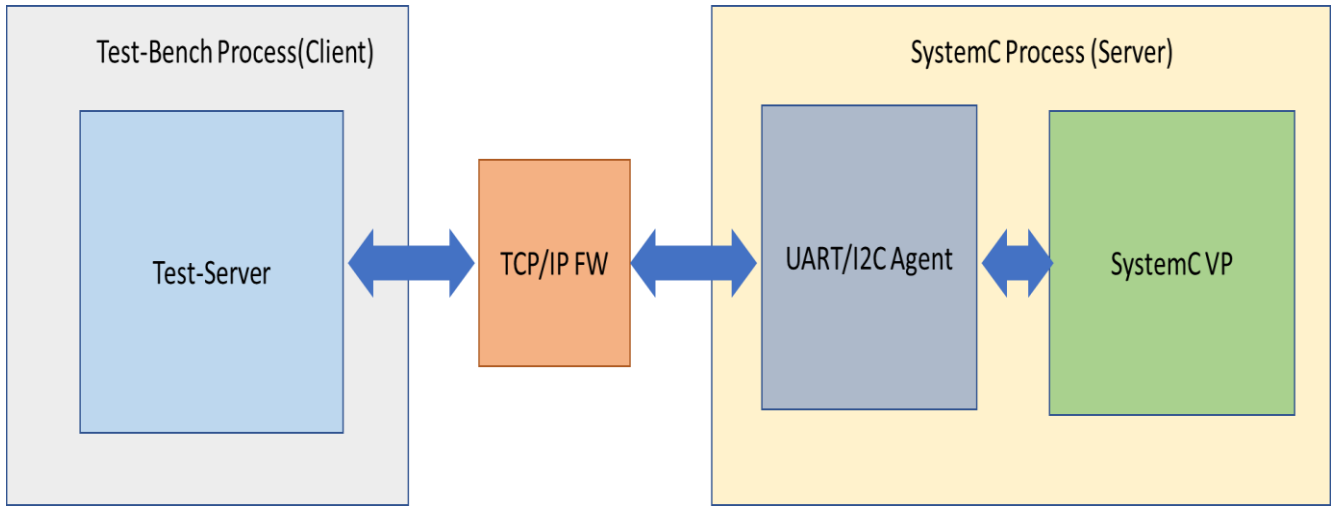
Vendor IP

Black Box

Bird's Eye View



Unified Testing Framework



- Early SW testing/validation
- Flexibility of use for SW
- Single application for multiple platforms(VP/FPGA/Silicon)
- Single block validation
- Multiple parallel users

Simulation Speed : RTL vs VP

1000X times faster

VP	RTL
CPU time : 30 seconds	CPU time : 311 seconds

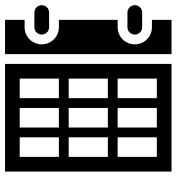
Just very slow.. That's all

Benefits for Software Validation

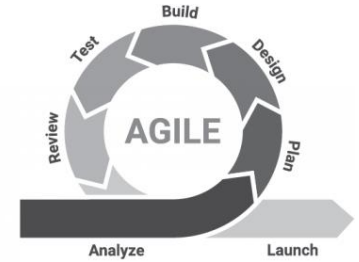
1000X faster than RTL

Ease of usage

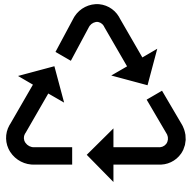
Debugging Advantage



Impacts Software Validation



Phased releases



Component Reuse

Conclusion and future work

- Accelerates time to market by up to 6 months
- Boost Customer Confidence
- Architectural Exploration
- Explore key algorithm performance
- In house automation

Questions