Smart TSV Repair Automation in 3DIC Designs

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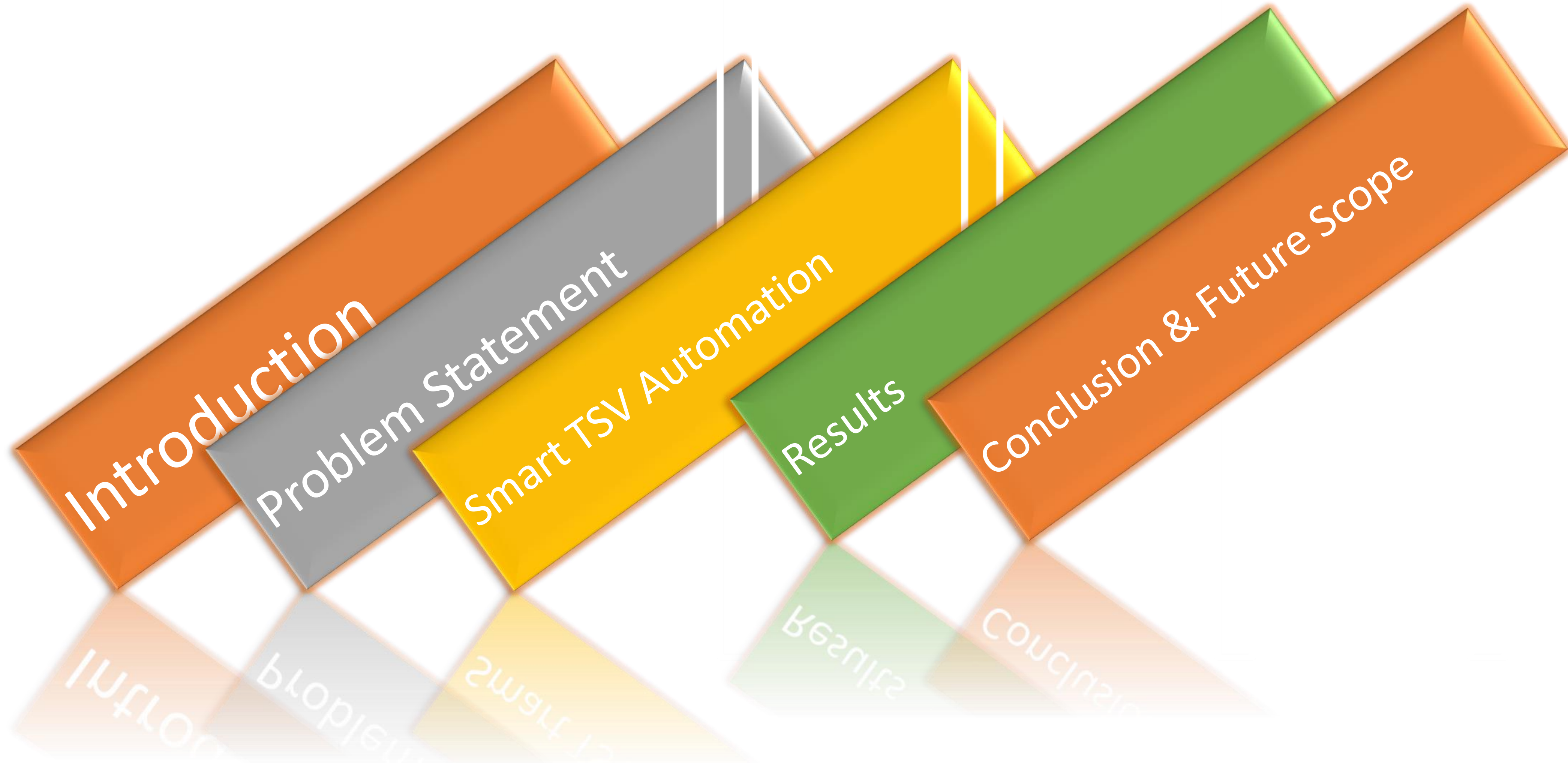
SAMSUNG

Agenda



Introduction

Logic
HBM
HBM

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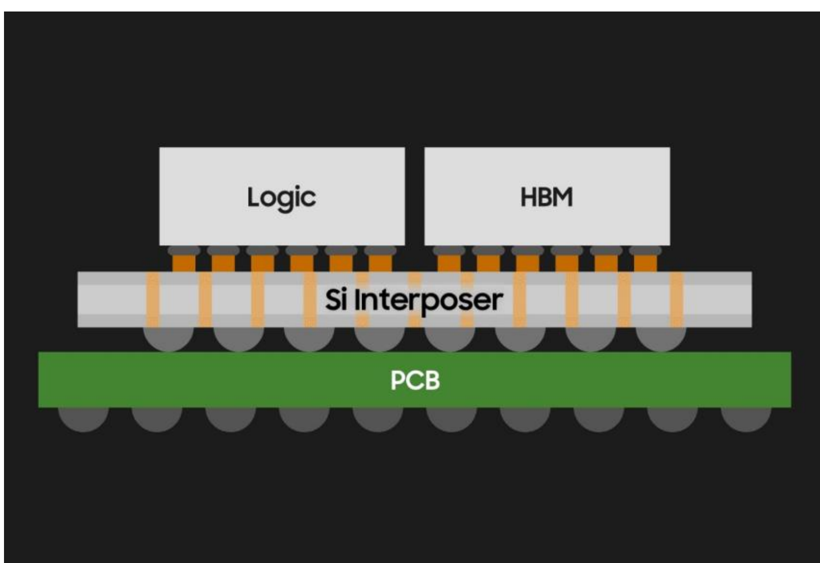
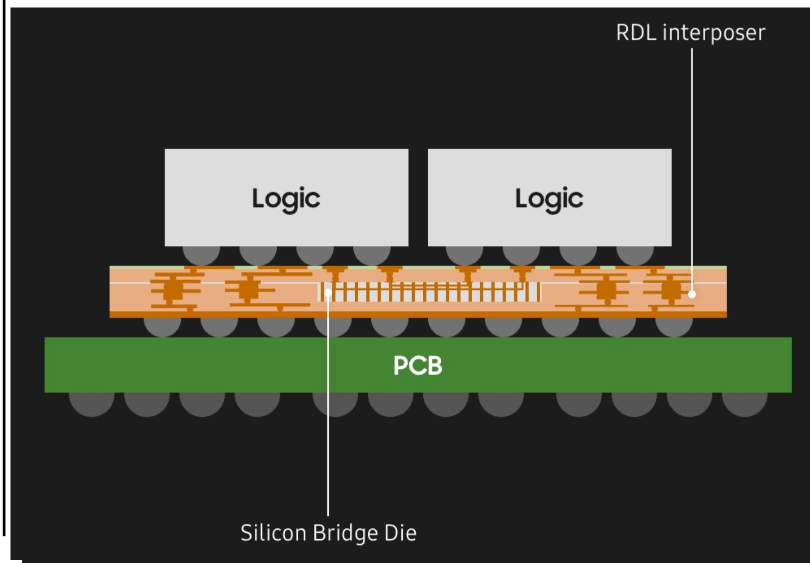
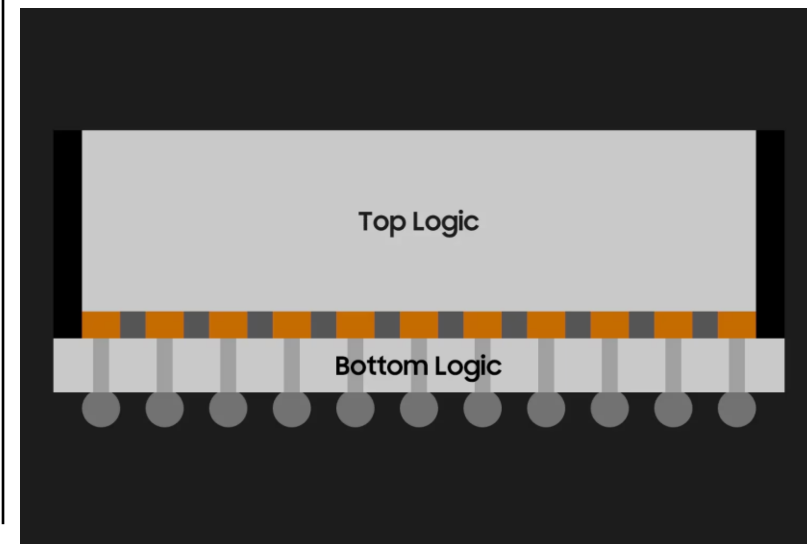
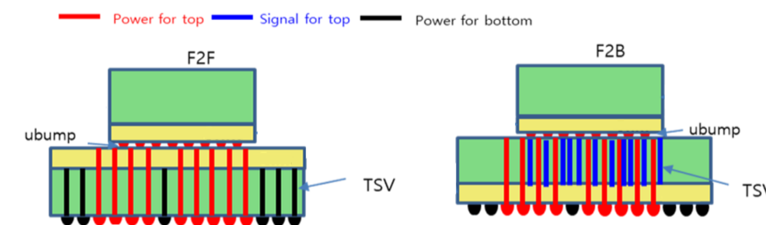
Introduction

HORIZONTAL INTEGRATION (2.5D) | X-CUBE (3DIC) (VERTICAL INTEGRATION)







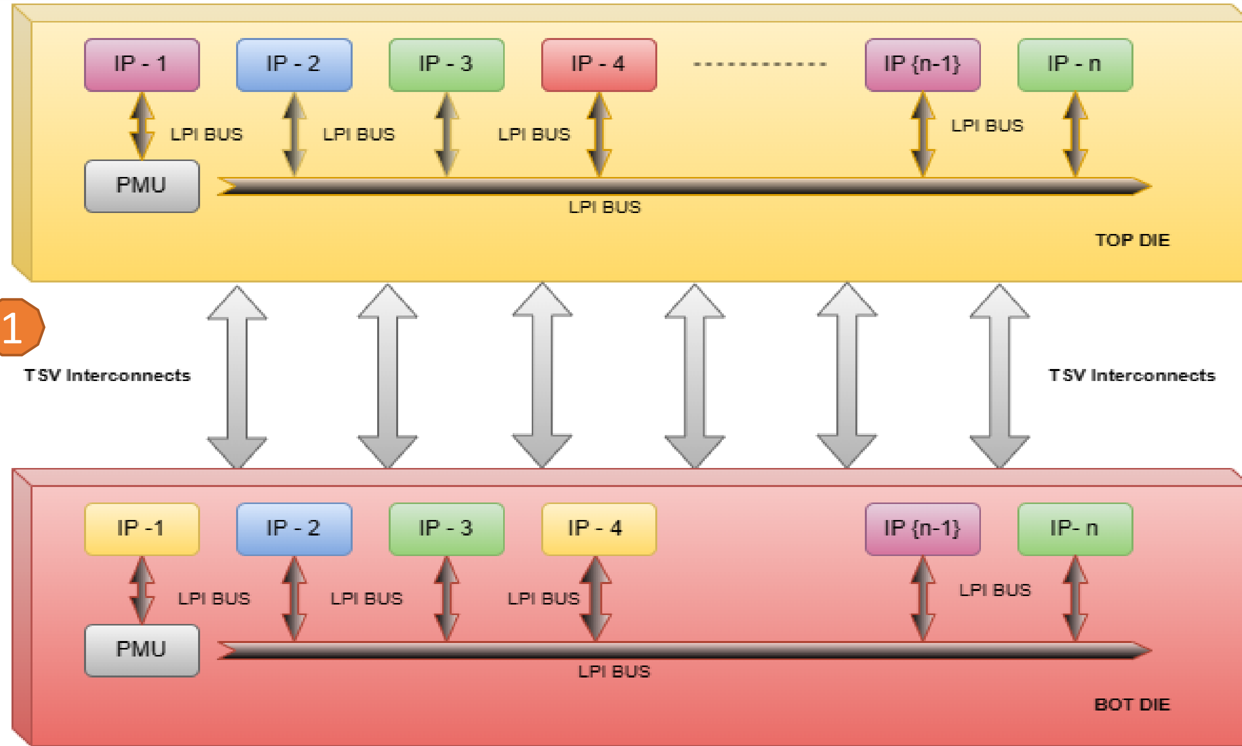


- 3DIC is most prominent technology advancement in Semiconductor Industry
- Offers Low latency, Higher bandwidth and package density
  - Shorter inter-connect lengths
- Heterogeneous Die Integration

Problem Statement

3DIC LOGIC DIEs

Faulty TSVs & Impact



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Power TSV Carries power from bottom die to upper dies

- Catastrophic
- Impacts the yield directly

Signal TSV Control and Data Signal TSVs between Dies

- Limits the design functionality (Hang situation, Integrity failures)
- Control Signal TSV → Hang situation – Timeout
- Data Signal TSV → Integrity failures – CRC, ECC, Parity issues

Pad TSV Input/Output/In-Out pads from Bottom ←→ Top

- Impacts functionality stacked dies in certain ways
  - Interrupt propagation
  - External Ref clock stuck

3

	Fault Metrics				Fault Classification		
BLK	Groups	No. of TSVs per group	No. of Faults	Fault Spectrum	Ctrl Path	Data Path	LPI
BLK A (Die to Die)	965	18	34740	5.56%	10422	5211	1737
BLK B (Memory Access)	554	32	35456	3.13%	5318	10637	1773
BLK C (Other IPs)	298	36	21456	2.78%	2146	7510	1073

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Smart TSV Automation

Verification Challenges

Multitude number of tests to cover all TSVs (Functional & Gate Sims)

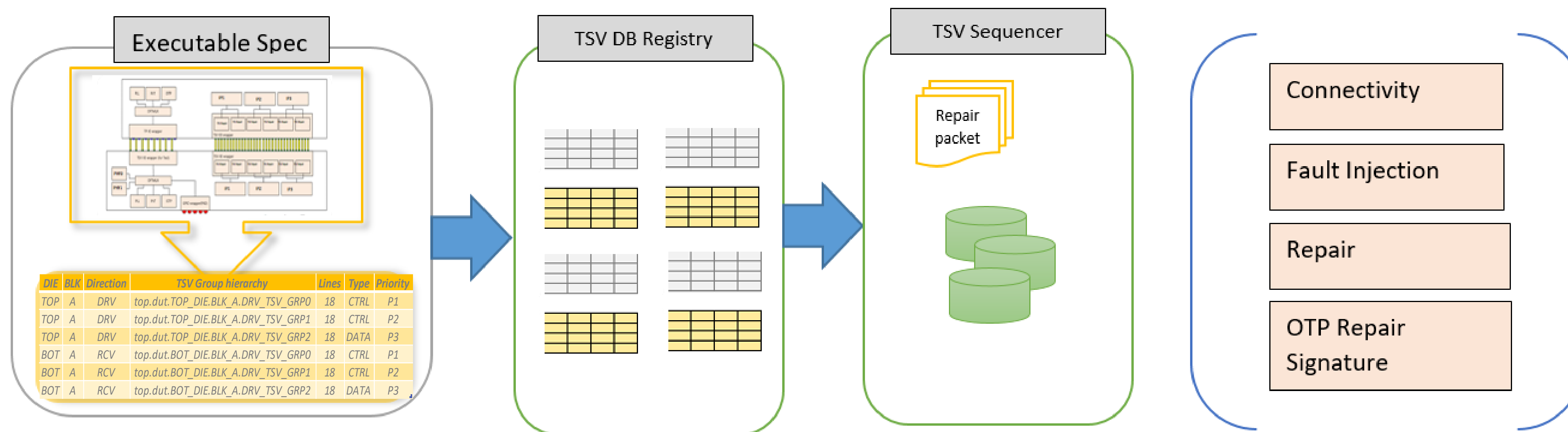
Repair Signature generation

Connectivity of TSVs across logical dies

A Bug escape can lead to potential issues

Coverage closure

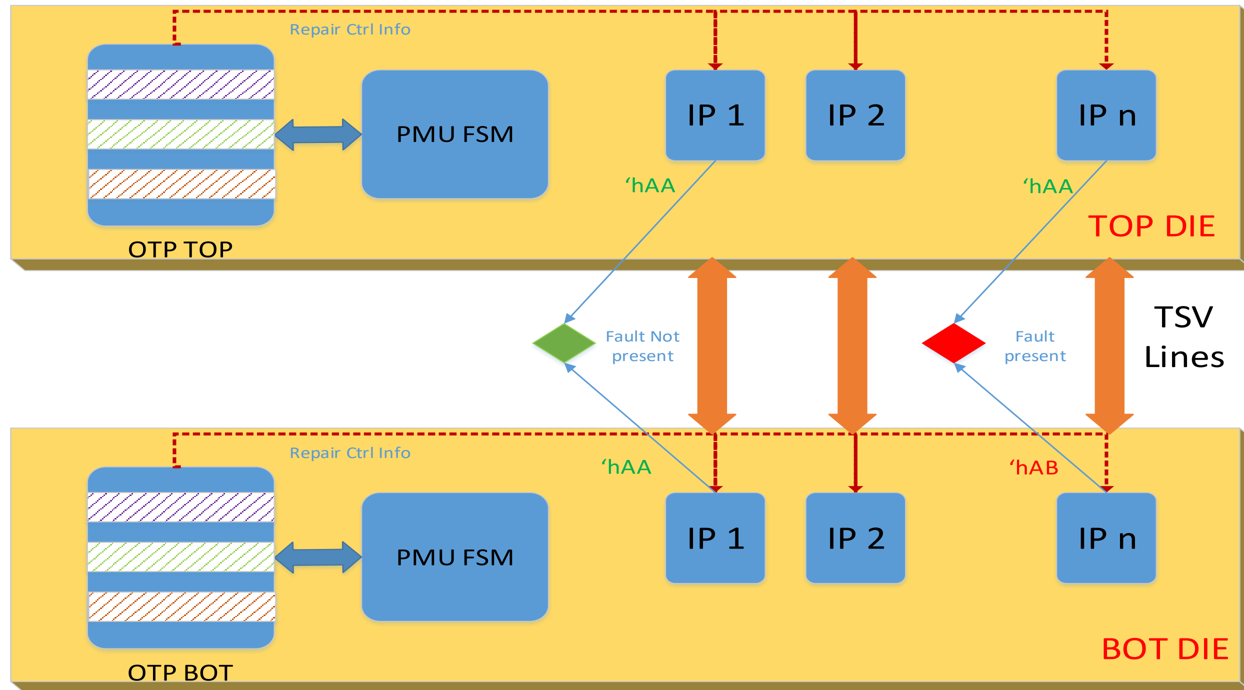
Automation - Concept



DIE	BLK	Direction	TSV Group hierarchy	Lines	Type	Priority
TOP	A	DRV	top.dut.TOP_DIE.BLK_A.DRV_TSV_GRP0	18	CTRL	P1
TOP	A	DRV	top.dut.TOP_DIE.BLK_A.DRV_TSV_GRP1	18	CTRL	P2
TOP	A	DRV	top.dut.TOP_DIE.BLK_A.DRV_TSV_GRP2	18	DATA	P3
BOT	A	RCV	top.dut.BOT_DIE.BLK_A.DRV_TSV_GRP0	18	CTRL	P1
BOT	A	RCV	top.dut.BOT_DIE.BLK_A.DRV_TSV_GRP1	18	CTRL	P2
BOT	A	RCV	top.dut.BOT_DIE.BLK_A.DRV_TSV_GRP2	18	DATA	P3

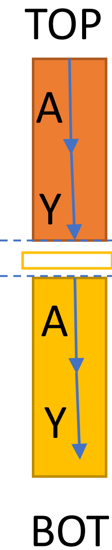
- Fully automated Sequences/APIs
- Embedded functional coverage instrumentation
- Random/Directed-random faults selection and OTP repair packets selection
- APIs for further writing custom test scenarios
- Test case Pruning with coverage-aware stimuli generator

TSV Connectivity



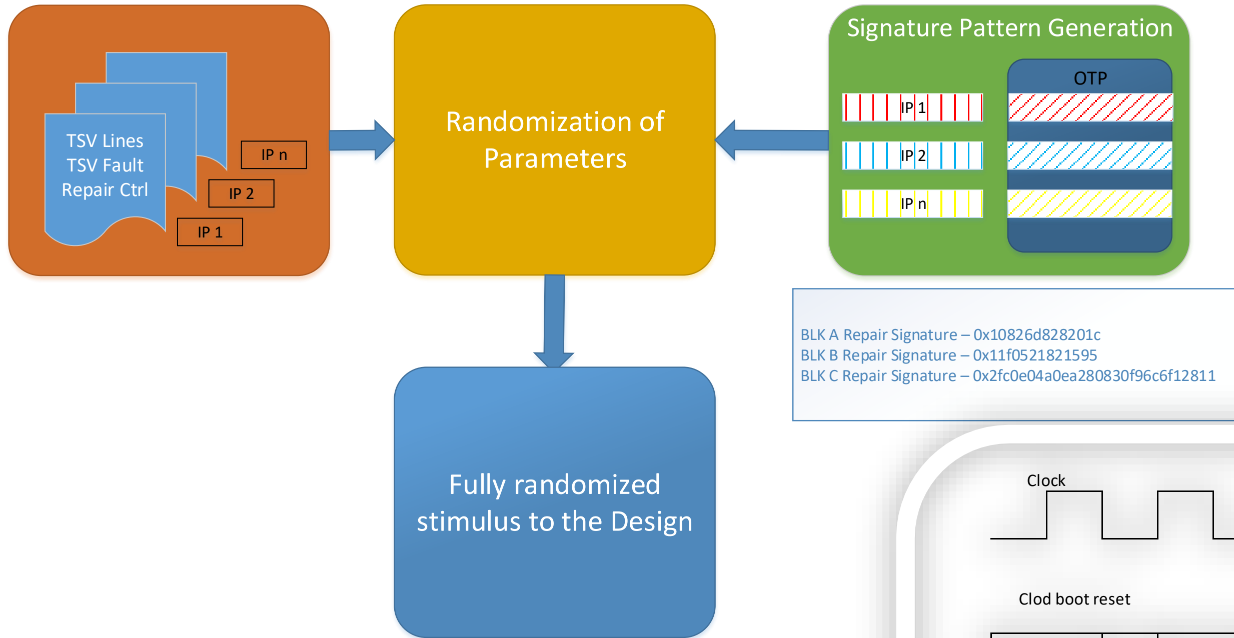
- OTP Repair signature connectivity
- TSV connectivity between dies

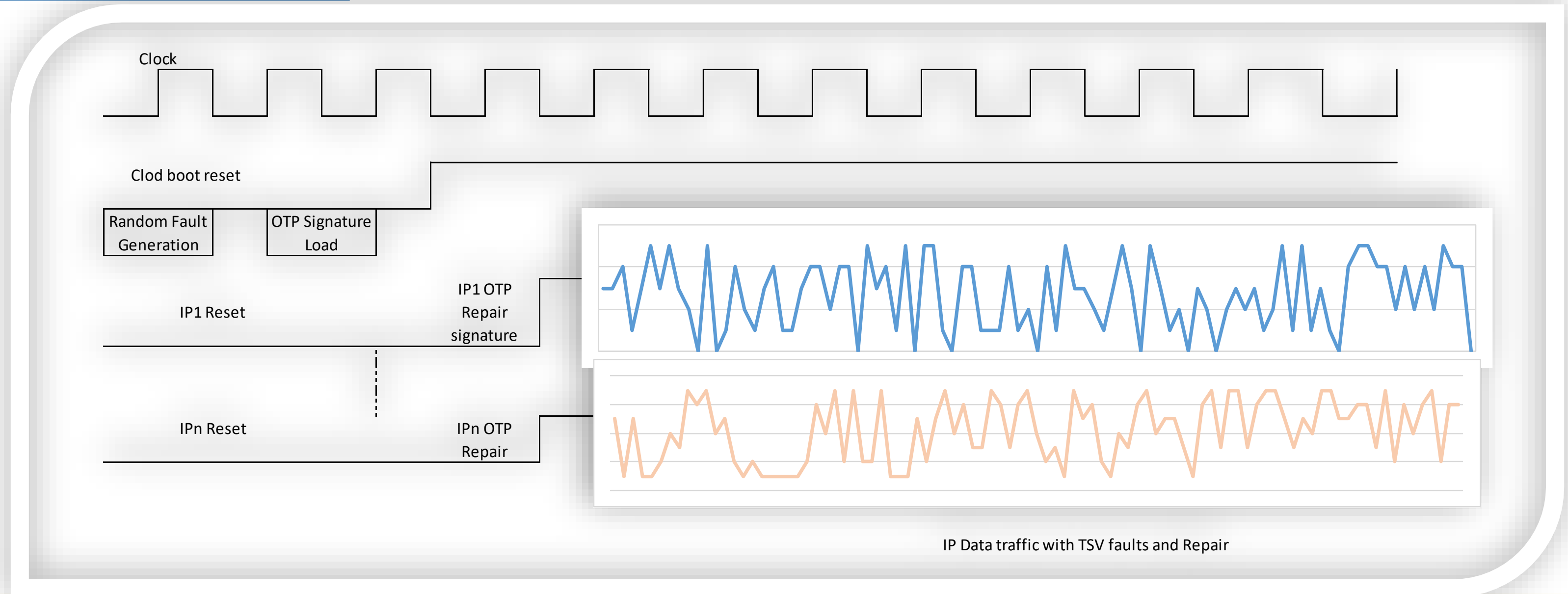
TSV Connectivity



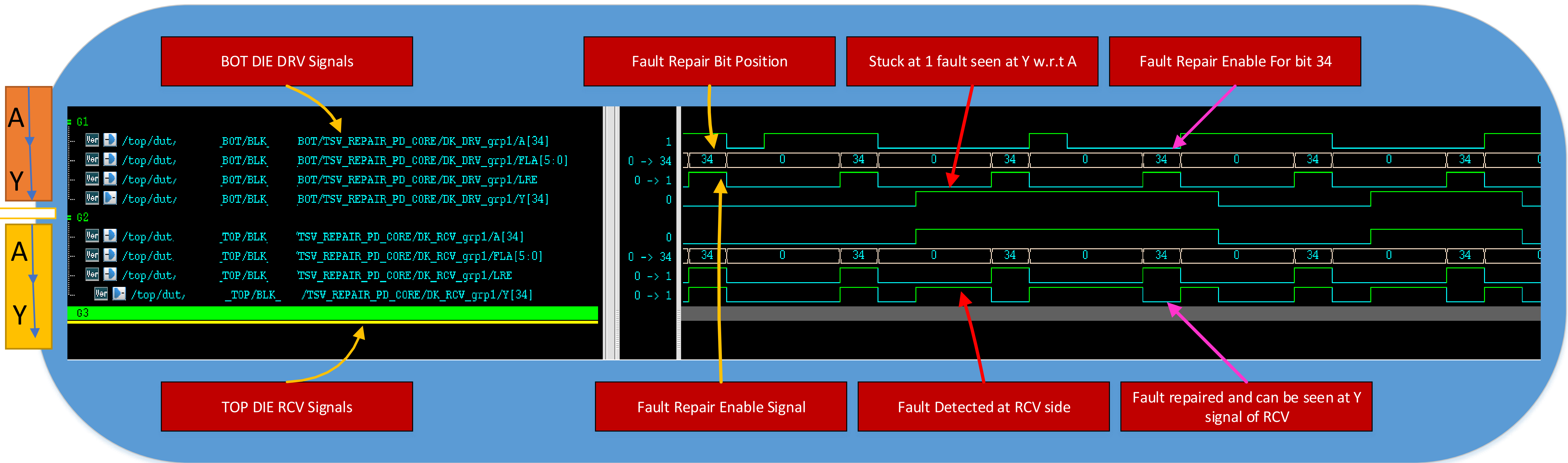
- As can be seen from the above snapshot, the Y output at the Driver side in TOP die *driver_grp1* is received at the A input of *receiver_grp1* in BOT die.
- The pattern sent are AA, 55, FF and Random data

Fault Injection, Repair





Fault Injection, Repair



Embedded Functional Coverage

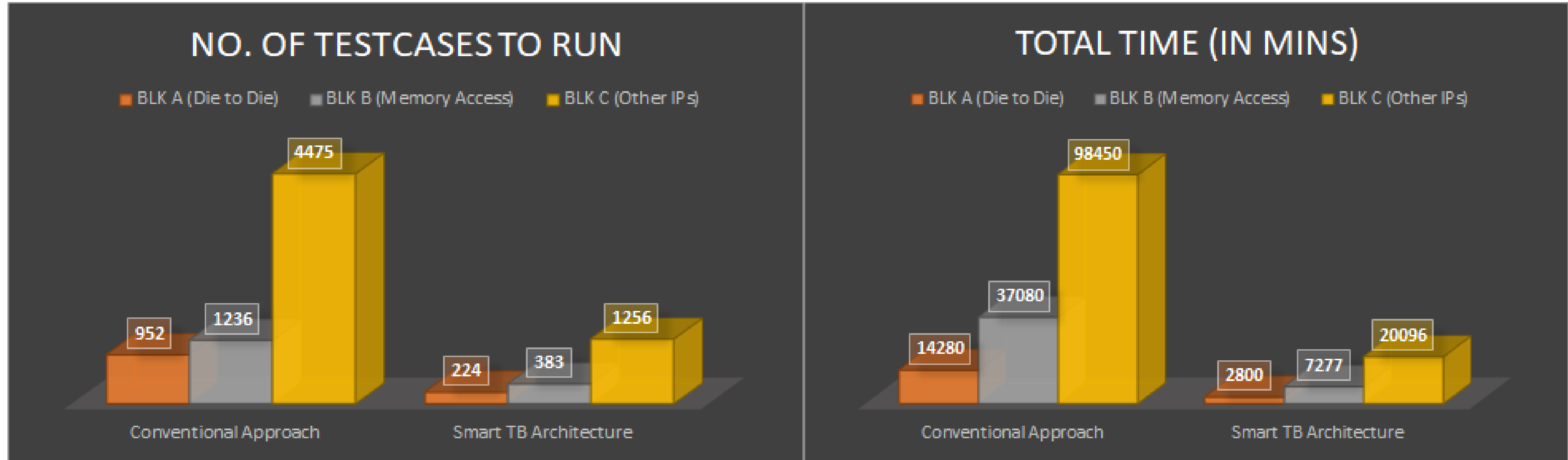
Faulty lines	• This coverpoint is used to make sure all the TSV lines are checked for Fault Injection for both stuck-at-0 and stuck-at-1
Signature based Repair check	• This coverpoint covers the TSV line repair based on the control signals and the Repair Signature for all the BLKs which are pre-loaded in OTP. This gives the complete coverage with the combination of TSV line and its control signal for Repair enable and the repairing of the same based on Signature.
Fault pattern	• Additional coverpoint is to check the fault pattern being injected with 0xAA, 0x55 and 0xFF patterns being the bins.

Results & Future Scope

Results – Test cases, Sim Time

	Conventional Approach			Smart TB Architecture			
BLK	**No. of Testcases to run**	**Avg. run time per testcase (in mins)**	**Total Time (in mins)**	**No. of Testcases to run**	**Avg. run time per testcase (in mins)**	**Total Time (in mins)**	**Reduction in time**
BLK A (Die to Die)	952	15	14280	224	12.5	2800	80.39%
BLK B (Memory Access)	1236	30	37080	383	19	7277	80.37%
BLK C (Other IPs)	4475	22	98450	1256	16	20096	79.59%

Results – Test cases, Sim Time



Results – Coverage

Covergroups

Name	Coverage
DK_DRV1	
u_TSV_DK_COV	
u_TsvRepairCoverage	100%
repair	100%
faultytsv	100%
DK_DRV2	
u_TSV_DK_COV	
u_TsvRepairCoverage	100%
repair	100%
faultytsv	100%
DK_DRV3	
u_TSV_DK_COV	
u_TsvRepairCoverage	100%
repair	100%
faultytsv	100%

Faulty TSV bins

Name	Overall Average Grade	Overall Covered	Score
(no filter)	(no filter)	(no filter)	(no filter)
Fline[64'h0000000000000000]	100%	1 / 1 (100%)	2880
Fline[64'h0000000000000001]	100%	1 / 1 (100%)	70
Fline[64'h0000000000000002]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000003]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000004]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000005]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000006]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000007]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000008]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000009]	100%	1 / 1 (100%)	120
Fline[64'h000000000000000a]	100%	1 / 1 (100%)	120
Fline[64'h000000000000000b]	100%	1 / 1 (100%)	120
Fline[64'h000000000000000c]	100%	1 / 1 (100%)	120
Fline[64'h000000000000000d]	100%	1 / 1 (100%)	120
Fline[64'h000000000000000e]	100%	1 / 1 (100%)	120
Fline[64'h000000000000000f]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000010]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000011]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000012]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000013]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000014]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000015]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000016]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000017]	100%	1 / 1 (100%)	120
Fline[64'h0000000000000018]	100%	1 / 1 (100%)	121
Fline[64'h0000000000000019]	100%	1 / 1 (100%)	121
Fline[64'h000000000000001a]	100%	1 / 1 (100%)	123
Fline[64'h000000000000001b]	100%	1 / 1 (100%)	121
Fline[64'h000000000000001c]	100%	1 / 1 (100%)	122
Fline[64'h000000000000001d]	100%	1 / 1 (100%)	134
Fline[64'h000000000000001e]	100%	1 / 1 (100%)	136
Fline[64'h000000000000001f]	100%	1 / 1 (100%)	160
Fline[64'h0000000000000020]	100%	1 / 1 (100%)	233
Fline[64'h0000000000000021]	100%	1 / 1 (100%)	317
Fline[64'h0000000000000022]	100%	1 / 1 (100%)	1229

TSV Line bins

Name	Overall Average Grade	Overall Covered	Score
(no filter)	(no filter)	(no filter)	(n
TsvLines[0]	100%	1 / 1 (100%)	80
TsvLines[1]	100%	1 / 1 (100%)	80
TsvLines[2]	100%	1 / 1 (100%)	80
TsvLines[3]	100%	1 / 1 (100%)	80
TsvLines[4]	100%	1 / 1 (100%)	80
TsvLines[5]	100%	1 / 1 (100%)	80
TsvLines[6]	100%	1 / 1 (100%)	80
TsvLines[7]	100%	1 / 1 (100%)	80
TsvLines[8]	100%	1 / 1 (100%)	80
TsvLines[9]	100%	1 / 1 (100%)	80
TsvLines[10]	100%	1 / 1 (100%)	80
TsvLines[11]	100%	1 / 1 (100%)	80
TsvLines[12]	100%	1 / 1 (100%)	80
TsvLines[13]	100%	1 / 1 (100%)	80
TsvLines[14]	100%	1 / 1 (100%)	80
TsvLines[15]	100%	1 / 1 (100%)	80
TsvLines[16]	100%	1 / 1 (100%)	80
TsvLines[17]	100%	1 / 1 (100%)	80
TsvLines[18]	100%	1 / 1 (100%)	80
TsvLines[19]	100%	1 / 1 (100%)	80
TsvLines[20]	100%	1 / 1 (100%)	80
TsvLines[21]	100%	1 / 1 (100%)	80
TsvLines[22]	100%	1 / 1 (100%)	80
TsvLines[23]	100%	1 / 1 (100%)	80
TsvLines[24]	100%	1 / 1 (100%)	80
TsvLines[25]	100%	1 / 1 (100%)	80
TsvLines[26]	100%	1 / 1 (100%)	80
TsvLines[27]	100%	1 / 1 (100%)	80
TsvLines[28]	100%	1 / 1 (100%)	80
TsvLines[29]	100%	1 / 1 (100%)	80
TsvLines[30]	100%	1 / 1 (100%)	79
TsvLines[31]	100%	1 / 1 (100%)	80
TsvLines[32]	100%	1 / 1 (100%)	76
TsvLines[33]	100%	1 / 1 (100%)	52

Conclusion & Future Scope

Conclusion & Future Scope

- Generic Smart TSV Testbench Automation (Re-use)
- Smart Test case selection (RTL & GLS) and overall TAT reduction
- Early bug detection
- Embedded coverage groups – Test case Pruning
- Power Analysis with TSV faults (SA0, SA1)

Q&A

Thank You