Smart TSV Repair Automation in 3DIC Designs

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Agenda

Introduction
Problem Statement
Smart TSV Automation
Results
Conclusion & Future Scope
Introduction

• 3DIC is most prominent technology advancement in Semiconductor Industry
• Offers Low latency, Higher bandwidth and package density
  • Shorter inter-connect lengths
• Heterogeneous Die Integration
Problem Statement
3DIC LOGIC DIES

Faulty TSVs & Impact

2. Power TSV
Carries power from bottom die to upper dies
- Catastrophic
- Impacts the yield directly

Signal TSV
Control and Data Signal TSVs between Dies
- Limits the design functionality (Hang situation, Integrity failures)
- Control Signal TSV → Hang situation – Timeout
- Data Signal TSV → Integrity failures – CRC, ECC, Parity issues

Pad TSV
Input/Output/In-Out pads from Bottom ↔ Top
- Impacts functionality stacked dies in certain ways
  - Interrupt propagation
  - External Ref clock stuck

Fault Metrics

<table>
<thead>
<tr>
<th>BLK</th>
<th>No. of TSVs per group</th>
<th>No. of Faults</th>
<th>Fault Spectrum</th>
<th>Ctrl Path</th>
<th>Data Path</th>
<th>LPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLK A (Die to Die)</td>
<td>965</td>
<td>18</td>
<td>34740</td>
<td>5.56%</td>
<td>10422</td>
<td>1737</td>
</tr>
<tr>
<td>BLK B (Memory Access)</td>
<td>554</td>
<td>32</td>
<td>35456</td>
<td>3.13%</td>
<td>5318</td>
<td>1773</td>
</tr>
<tr>
<td>BLK C (Other IPs)</td>
<td>298</td>
<td>36</td>
<td>21456</td>
<td>2.78%</td>
<td>2146</td>
<td>1073</td>
</tr>
</tbody>
</table>
Smart TSV Automation
Verification Challenges

- Multitude number of tests to cover all TSVs (Functional & Gate Sims)
- Repair Signature generation
- Connectivity of TSVs across logical dies
- A Bug escape can lead to potential issues
- Coverage closure
• Fully automated Sequences/APIs
• Embedded functional coverage instrumentation
• Random/Directed-random faults selection and OTP repair packets selection
• APIs for further writing custom test scenarios
• Test case Pruning with coverage-aware stimuli generator
TSV Connectivity

- OTP Repair signature connectivity
- TSV connectivity between dies
As can be seen from the above snapshot, the Y output at the Driver side in TOP die `driver_grp1` is received at the A input of `receiver_grp1` in BOT die.

The pattern sent are AA, 55, FF and Random data.
Fault Injection, Repair

Randomization of Parameters

Fully randomized stimulus to the Design

Signature Pattern Generation

OTP

BLK A Repair Signature – 0x10826d828201c
BLK B Repair Signature – 0x11f0521821595
BLK C Repair Signature – 0x2fc0e04a0ea280830f96c6f12811

Random Fault Generation

OTP Signature Load

IP1 Reset

IP1 OTP Repair

IPn Reset

IPn OTP Repair

IP Data traffic with TSV faults and Repair
Fault Injection, Repair

- BOT DIE DRV Signals
- TOP DIE RCV Signals
- Fault Repair Bit Position
- Fault Repair Enable Signal
- Stuck at 1 fault seen at Y w.r.t A
- Fault Detected at RCV side
- Fault repaired and can be seen at Y signal of RCV

Fault Injection, Repair
Embedded Functional Coverage

- **Faulty lines**: This coverpoint is used to make sure all the TSV lines are checked for Fault Injection for both stuck-at-0 and stuck-at-1.

- **Signature based Repair check**: This coverpoint covers the TSV line repair based on the control signals and the Repair Signature for all the BLKs which are pre-loaded in OTP. This gives the complete coverage with the combination of TSV line and its control signal for Repair enable and the repairing of the same based on Signature.

- **Fault pattern**: Additional coverpoint is to check the fault pattern being injected with 0xAA, 0x55 and 0xFF patterns being the bins.
Results & Future Scope
<table>
<thead>
<tr>
<th>BLK</th>
<th>Conventional Approach</th>
<th>Smart TB Architecture</th>
<th>Reduction in time</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>No. of Testcases to run</td>
<td>Avg. run time per testcase (in mins)</td>
<td>Total Time (in mins)</td>
</tr>
<tr>
<td>BLK A (Die to Die)</td>
<td>952</td>
<td>15</td>
<td>14280</td>
</tr>
<tr>
<td>BLK B (Memory Access)</td>
<td>1236</td>
<td>30</td>
<td>37080</td>
</tr>
<tr>
<td>BLK C (Other IPs)</td>
<td>4475</td>
<td>22</td>
<td>98450</td>
</tr>
</tbody>
</table>
Results – Test cases, Sim Time

**NO. OF TESTCASES TO RUN**

- **Conventional Approach**
  - BLK A (Die to Die): 952
  - BLK B (Memory Access): 1236
  - BLK C (Other IPs): 224
- **Smart TB Architecture**
  - BLK A (Die to Die): 4475
  - BLK B (Memory Access): 383
  - BLK C (Other IPs): 1256

**TOTAL TIME (IN MINS)**

- **Conventional Approach**
  - BLK A (Die to Die): 14280
  - BLK B (Memory Access): 37680
  - BLK C (Other IPs): 7277
- **Smart TB Architecture**
  - BLK A (Die to Die): 20096
  - BLK B (Memory Access): 2000
  - BLK C (Other IPs): 2000
## Results – Coverage

<table>
<thead>
<tr>
<th>Covergroups</th>
<th>Faulty TSV bins</th>
<th>TSV Line bins</th>
</tr>
</thead>
<tbody>
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<td><strong>Faulty TSV bins</strong></td>
<td><strong>TSV Line bins</strong></td>
</tr>
<tr>
<td>DK_DRV1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>u_Tsv,DK_COV</td>
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<td></td>
</tr>
<tr>
<td>u_TsvRepairCoverage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>repair</td>
<td></td>
<td></td>
</tr>
<tr>
<td>faultytsv</td>
<td>100%</td>
<td></td>
</tr>
<tr>
<td>DK_DRV2</td>
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<td></td>
</tr>
<tr>
<td>u_Tsv,DK_COV</td>
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<td></td>
</tr>
<tr>
<td>u_TsvRepairCoverage</td>
<td>100%</td>
<td></td>
</tr>
<tr>
<td>repair</td>
<td>100%</td>
<td></td>
</tr>
<tr>
<td>faultytsv</td>
<td>100%</td>
<td></td>
</tr>
<tr>
<td>DK_DRV3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>u_Tsv,DK_COV</td>
<td></td>
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</tr>
<tr>
<td>u_TsvRepairCoverage</td>
<td>100%</td>
<td></td>
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<tr>
<td>faultytsv</td>
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</tr>
</tbody>
</table>
Conclusion & Future Scope

• Generic Smart TSV Testbench Automation (Re-use)
• Smart Test case selection (RTL & GLS) and overall TAT reduction
• Early bug detection
• Embedded coverage groups – Test case Pruning
• Power Analysis with TSV faults (SA0, SA1)
Q&A
Thank You