Addressing Protocol Verification Challenges in the Evolving Landscape of AI and High-Performance Computing (HPC)

Gaurav Chugh
Varun Agrawal

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About Me

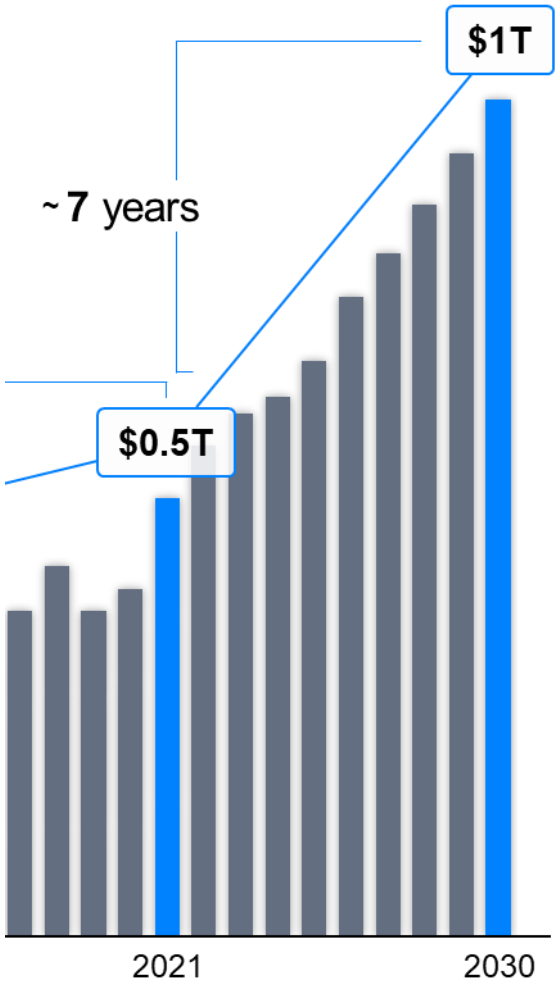
Gaurav Chugh is a Senior Director in the Protocol Solutions Engineering Group. He has been actively involved in Verification IP solutions, specifically focusing on pre-sales, evaluations, and deployments. Gaurav has around 20 years of industry experience and have published and presented papers at renowned conferences such as DAC, DVCON, and SNUG.

Gaurav Chugh
Senior Director
Synopsys

Agenda

- Market Overview – What is changing?
- Complexity and challenges – What is the impact ?
- Solutions Expected – What industry needs?
- Synopsys Protocol Verification Solutions – What Synopsys can offer?

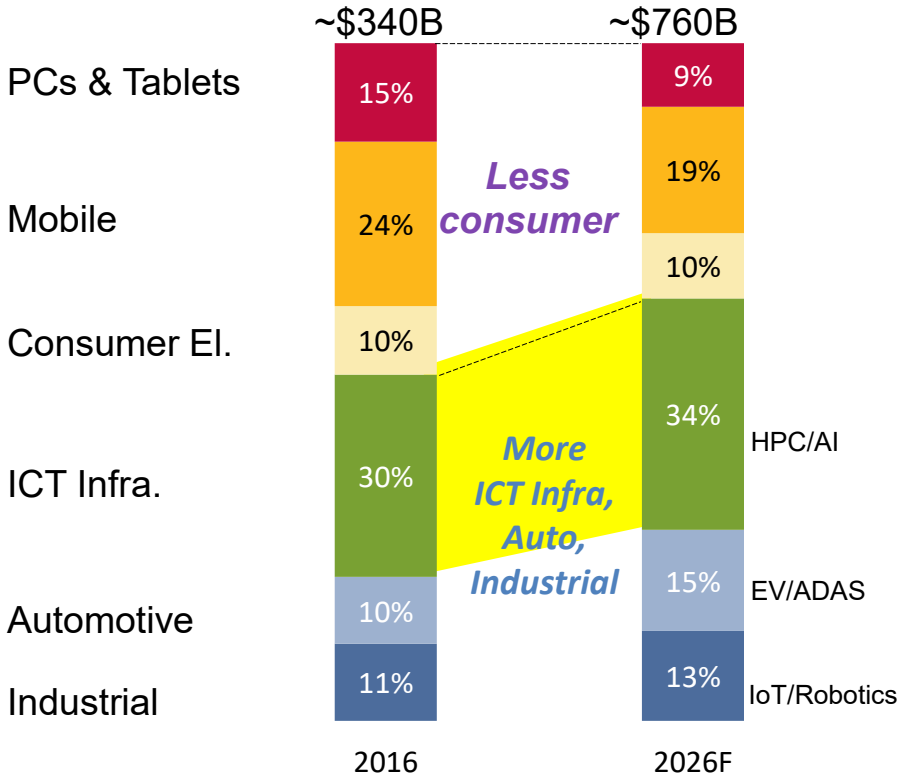
Artificial Intelligence (AI) - Single most trend driving the change



Sale total global semiconductor sales by end application market

Bar height = % of total semi sales

'Smart Everything (AI)' changes the mix



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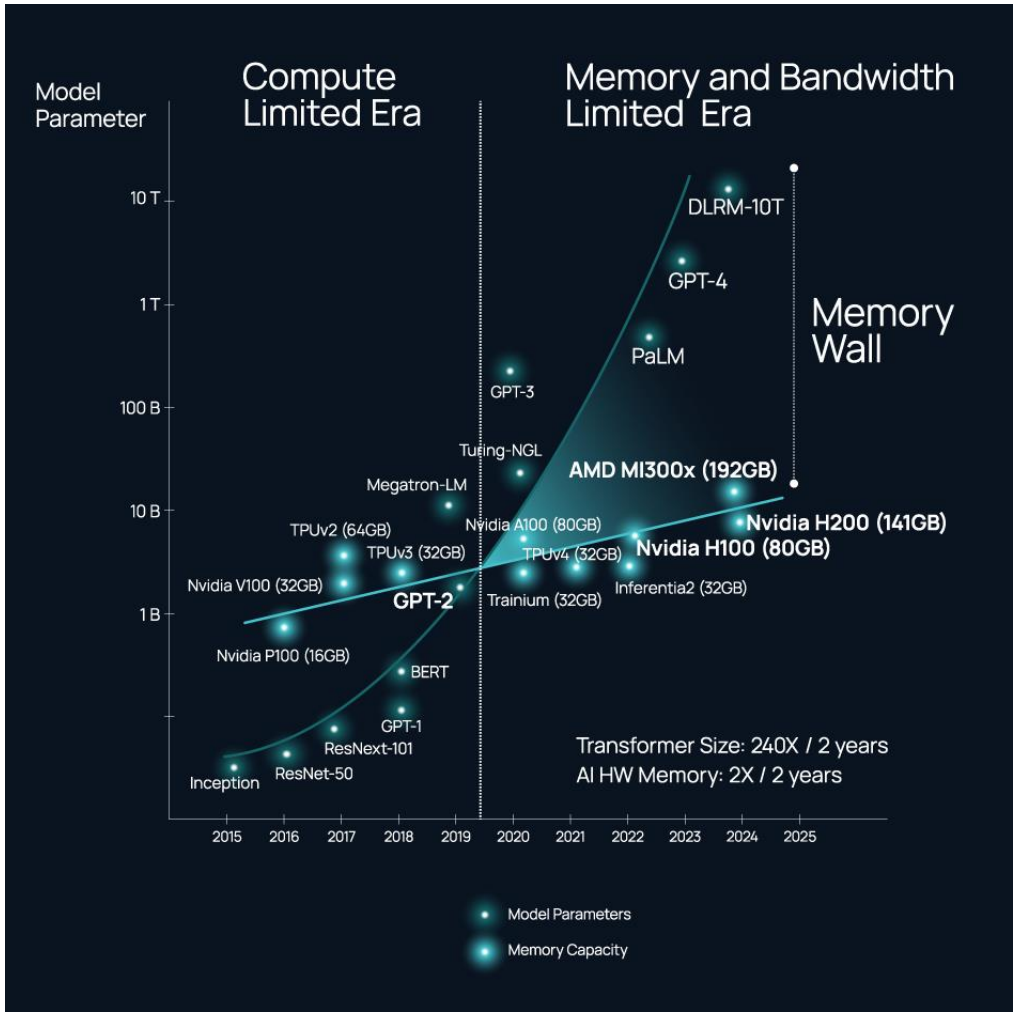
AI Driving Relentless Growth in Data Computation and Consumption



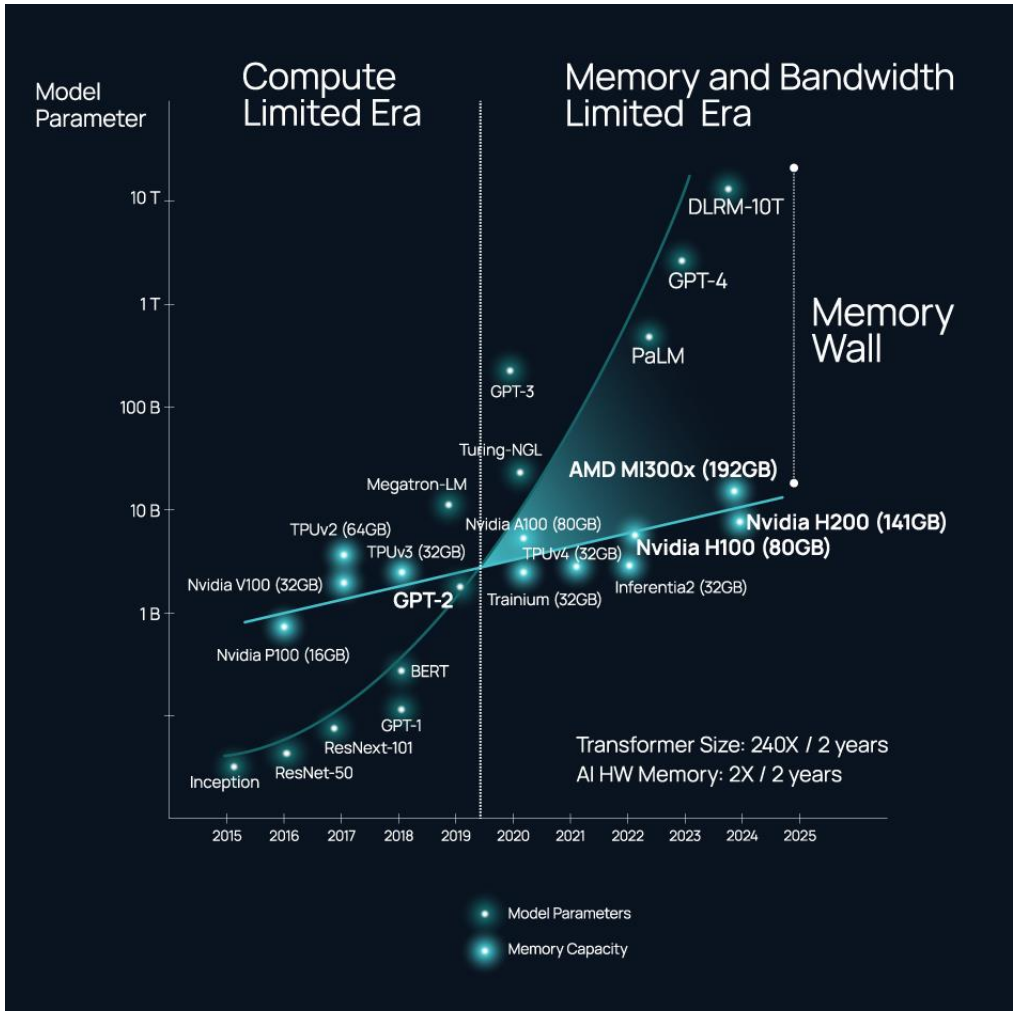
Number of parameters in AI models **doubles every 4 to 6 months**,
4x faster than Moore's Law, requiring more capacity, greater resources, and faster interconnects

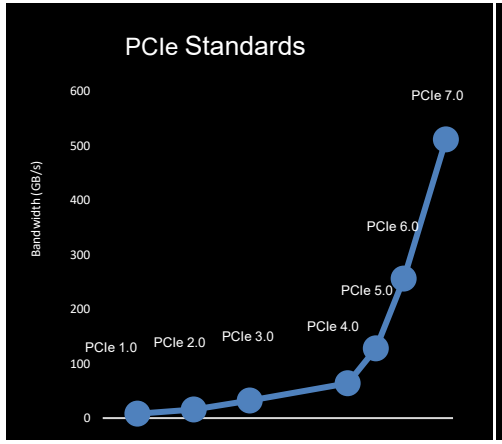
Llama 3:
+405B parameters
+15.6T tokens
Trained on 16,000 H100
70 days to train
More than $50M to train

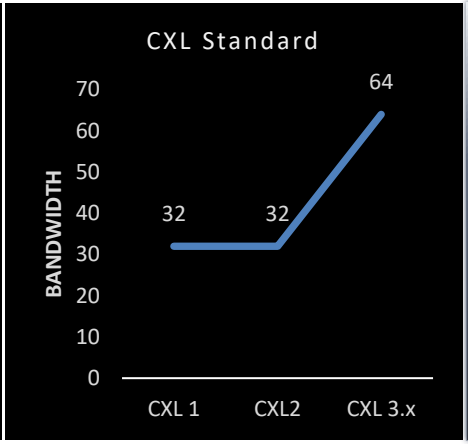
Source: Meta, OCP Summit Presentation Nov 2021

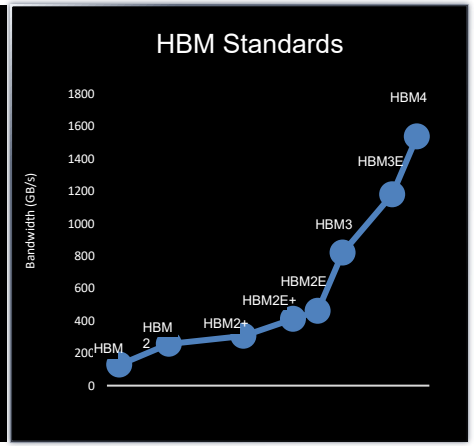
Hardware Capacity, Compute and Power – How does industry reduce cost ?

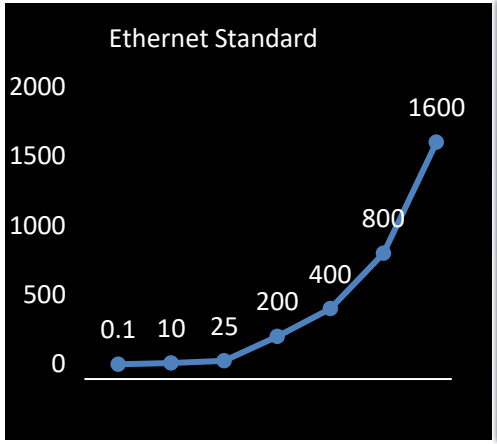
Interfaces evolving rapidly to support Incoming Compute Demands

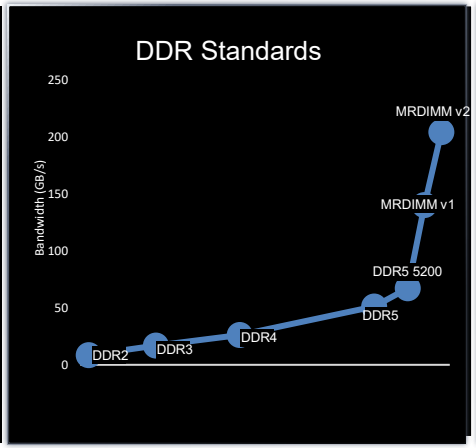


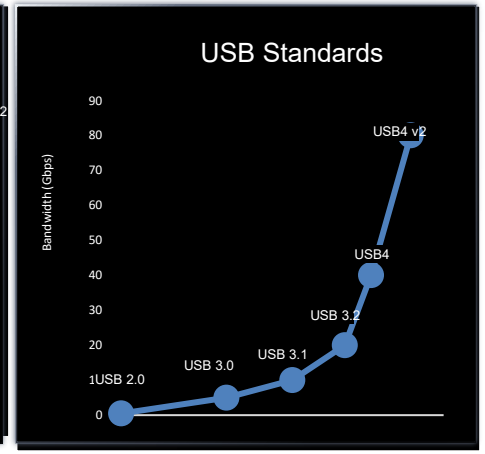












Faster data Interfaces demand driving faster standard evolution

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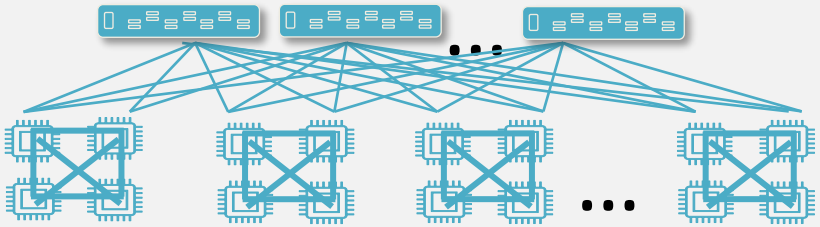
Newly Introduced AI Scaling Standards

Scaling Up with UALink

An Ethernet based open, interoperable, high performance stack architecture to meet the growing network demands of AI & HPC at scale.

ULTRA ACCELERATOR LINK™



9 Promoter Members

AMD, Intel, Meta, HPE, AWS, Astera, Cisco, Google, Microsoft

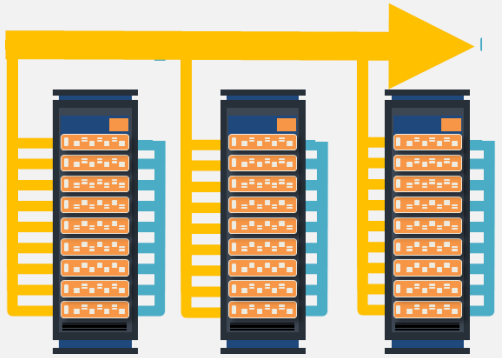
Alibaba Cloud, Apple, Synopsys, Teledyne LeCroy, XCONN TECH, anapass, Microchip, MIPS, Montage Technology, centec, Cluster Systems, CREDO, enfabrica, GIGA IO, H3C, auradine, Lightelligence, Linkdata, Marvell, ZTE中兴

ACTIVARA TECHNOLOGY PTE. LTD.
Beijing Sudo Information Technology CO., LTD
DreamBig Semiconductor Inc
M2 Semiconductor Ltd.
MemVerge
MetaX Integrated Circuits (Shanghai) Co., Ltd
Surge Intelligence
TeraHop Pte. LTD.
Theo End (Shenzhen) Computing Technology Co., Ltd.
Verkor IO LLC
Xinpal PTE. LTD.

Scaling Out with Ultra Ethernet

Open industry standard group formed to facilitate direct load, store, and atomic operations between AI Accelerators (i.e. GPUs).

Ultra Ethernet Consortium



Steering Members

AMD, Arista, Broadcom, Cisco, Eviden an atos business, Hewlett Packard Enterprise, intel, Meta, Microsoft, Oracle

General Members

Alibaba Cloud, Arrcus, Baidu 百度, 世纪互联 VNET, ByteDance, Dell Technologies, enfabrica, Huawei, IBM, Juniper Networks, Keysight Technologies, Lawrence Livermore National Laboratory, Marvell, H3C, Nokia, Preferred Networks, Spirent, Synopsys, ZTE中兴

Contributor Members

Accelink, Alphawave Semi, Asterfusion, centec, ciena, Cornelis Networks, CREDO, DreamBig, DriveNets, Fathom Computing, Fujitsu, FRAEO, Kalray, Lenovo, MemVerge, NEUREALITY, Rujie, Salience Labs, Samsung SDS, Sandia National Laboratories, SAPEON, Scala Computing, Tencent 腾讯, Xsight

*Please note that not all members are displayed on this page.

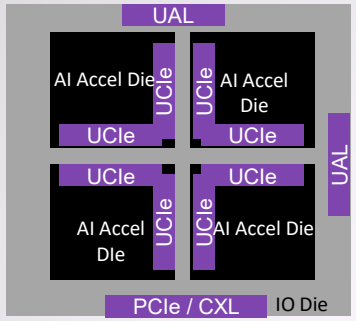
Custom Silicon/Interfaces/Methodologies Optimized For AI

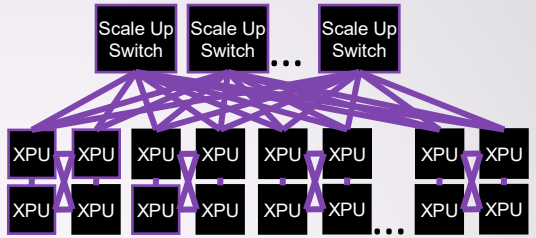
Custom Silicon	Interface Upgrades	Multi-die	New Standards and methodologies
Monolithic Die Hit Reticle Limits	High BW Memory & Multi-Die Systems w/Parallel Interconnect	NOW → Scale **Up**	AND → Scale **Out**

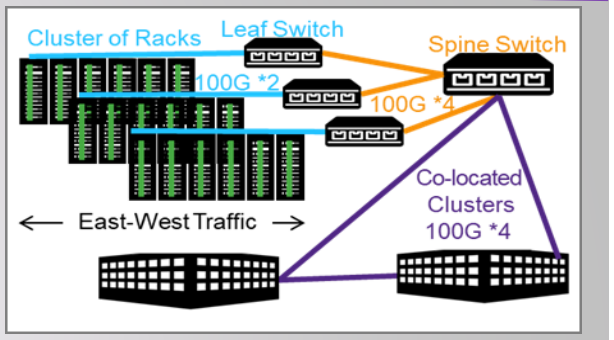
Monolithic AI Compute

AI Accelerator
Memory

HBM
AI Accelerator







Heterogenous Compute

AI Processors & Specialized Memories

HBM

DDR / HBM MRDIMM

UCIe Streaming

UCIe CXL/PCIe

UALink

PCIe / CXL

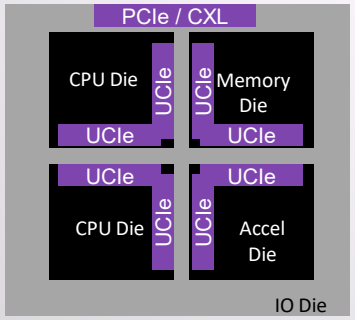
Ultra Ethernet

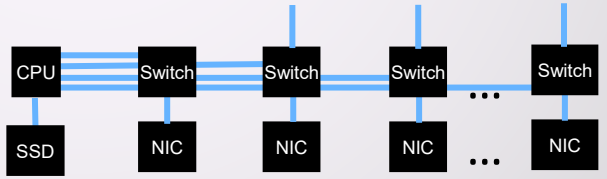
Ethernet

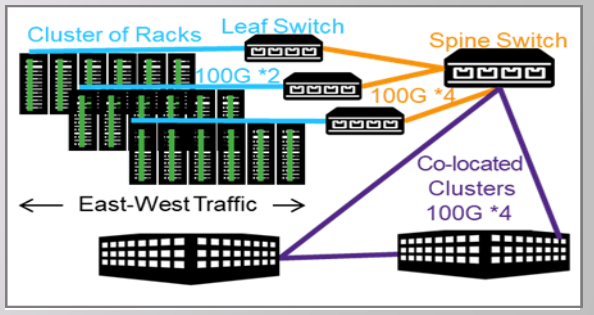
CPU
Memory

CPU

DDR/LPDDR HBM







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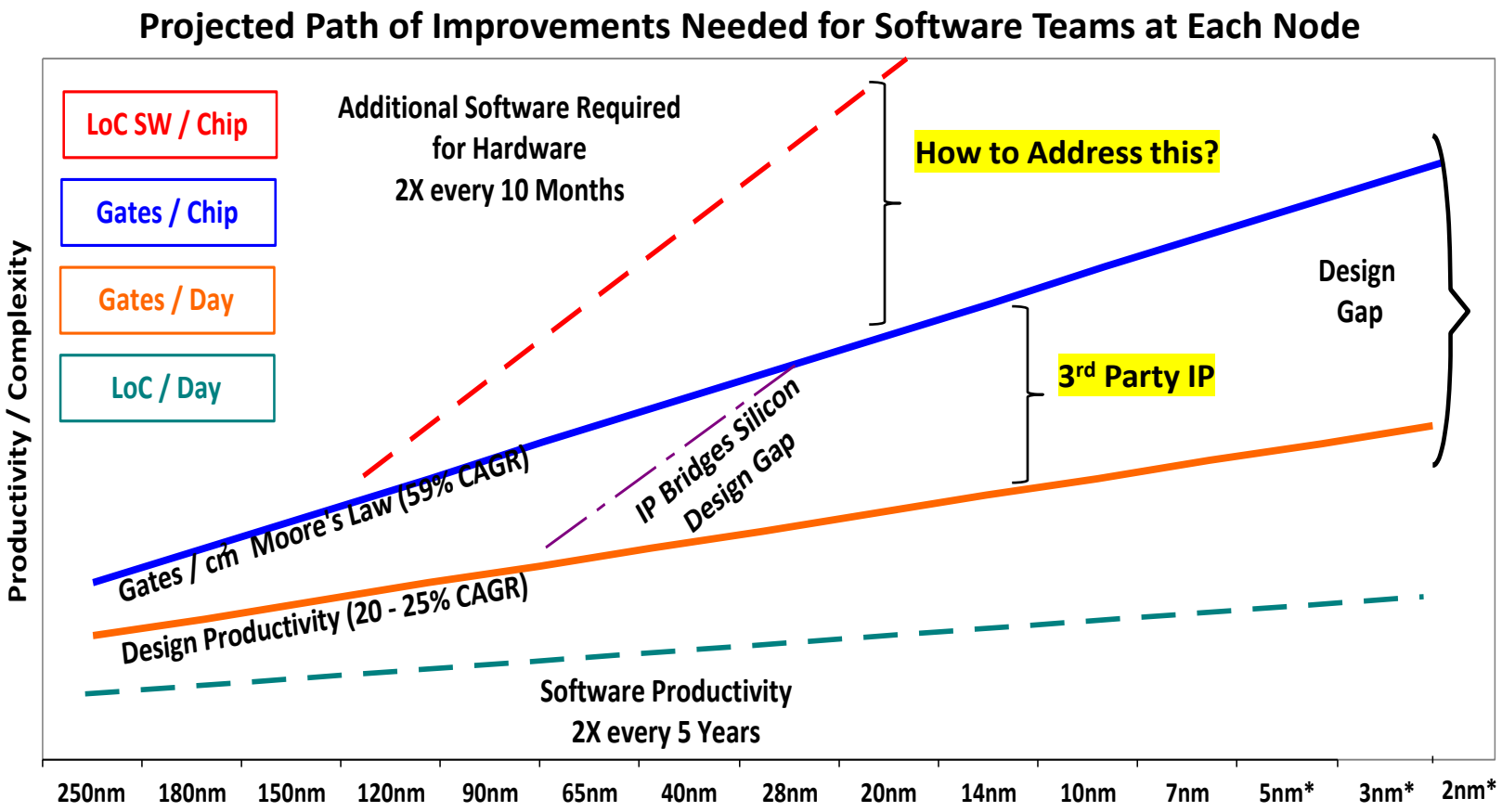
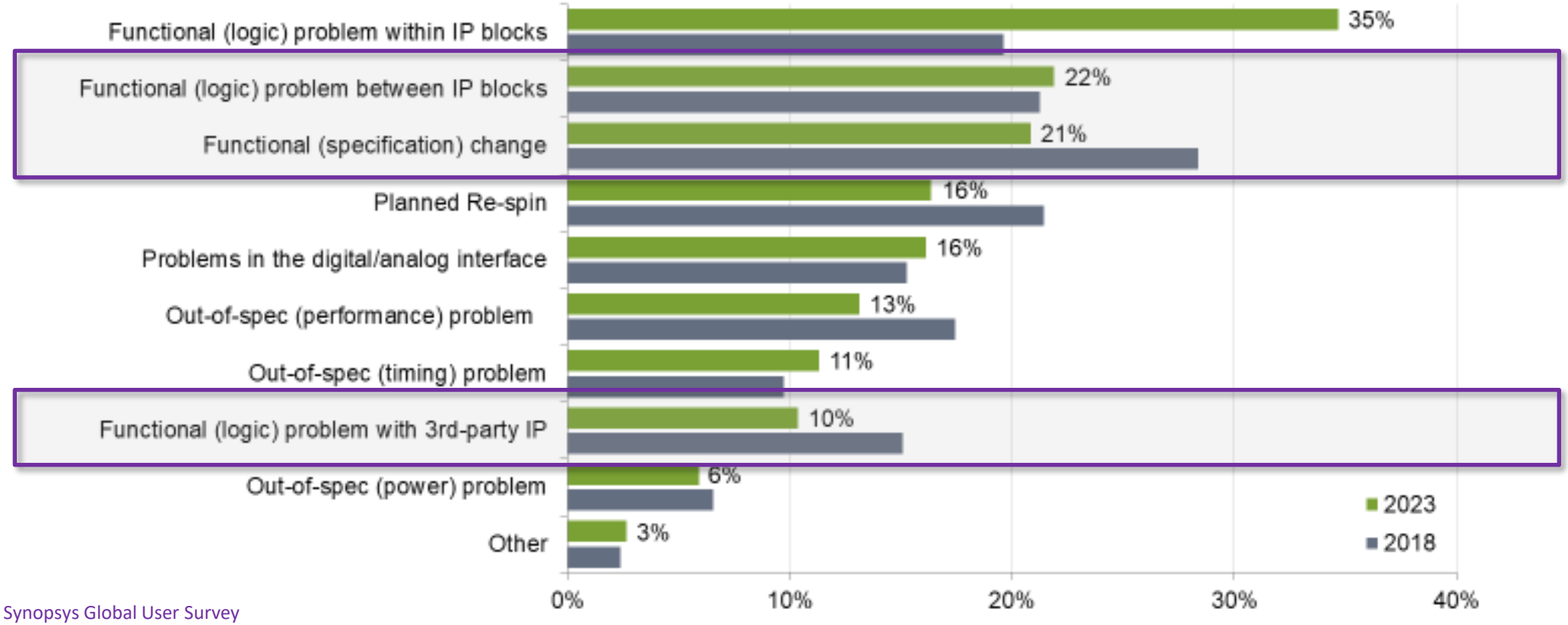
Design And Software Productivity Very Much Behind



Source ITRS and Semico Research Corp.

Talent pool, skillsets, tools and methodologies need to evolve

IP bring-up, interop, and convergence in SoCs leading causes of delay

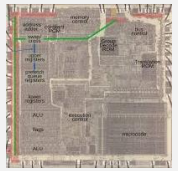


Source – Synopsys Global User Survey

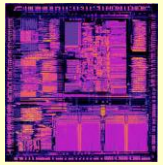
3rd Party IP Convergence And Cross Team/Partner Debug/Reference Consumes At Least 20% Of V&V Cycle Time

Test / Debug Approaches Sub-optimal for Peta-cycles Payloads

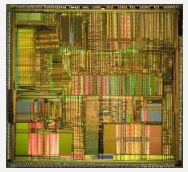
1978
Intel i386
29,000 Transistors



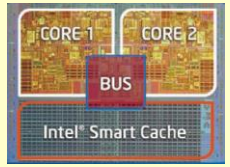
1985
Intel i386
275,000 Transistors



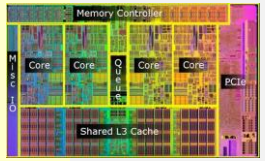
1994
Pentium P54C
3 million transistors



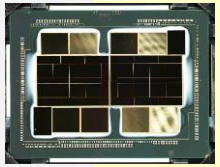
2006
Intel Core Duo
167 million Transistors



2009
Intel Core i5
774 million Transistors

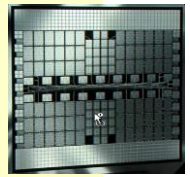


2021
Ponte Vecchio
100 billion Transistors



47 tiles

2025 (**not a "chip"**)
Grace Blackwell NVLINK72
130 trillion Transistors



5 orders of magnitude

3 orders of magnitude

Petacycles (10^{15})

Teracycles (10^{12})

Gigacycles (10^{9})

Megacycles (10^{6})

Kilocycles (10^{3})

Silicon bug escapes

Test/Verification Requirements

Test/Verification Generation Productivity

Test Generation Productivity Gap

Test Generation Productivity Gap

Accellera PSS, SW driven & directed

eRM, VMM, OVM, UVM, SystemVerilog *Constrained-random, assertions, coverage*

Manual *Ad-hoc, HW directed test*

Sub-system/SoC Blocks

1970 1980 1990 2000 2010 2020 2030

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What Solutions are needed

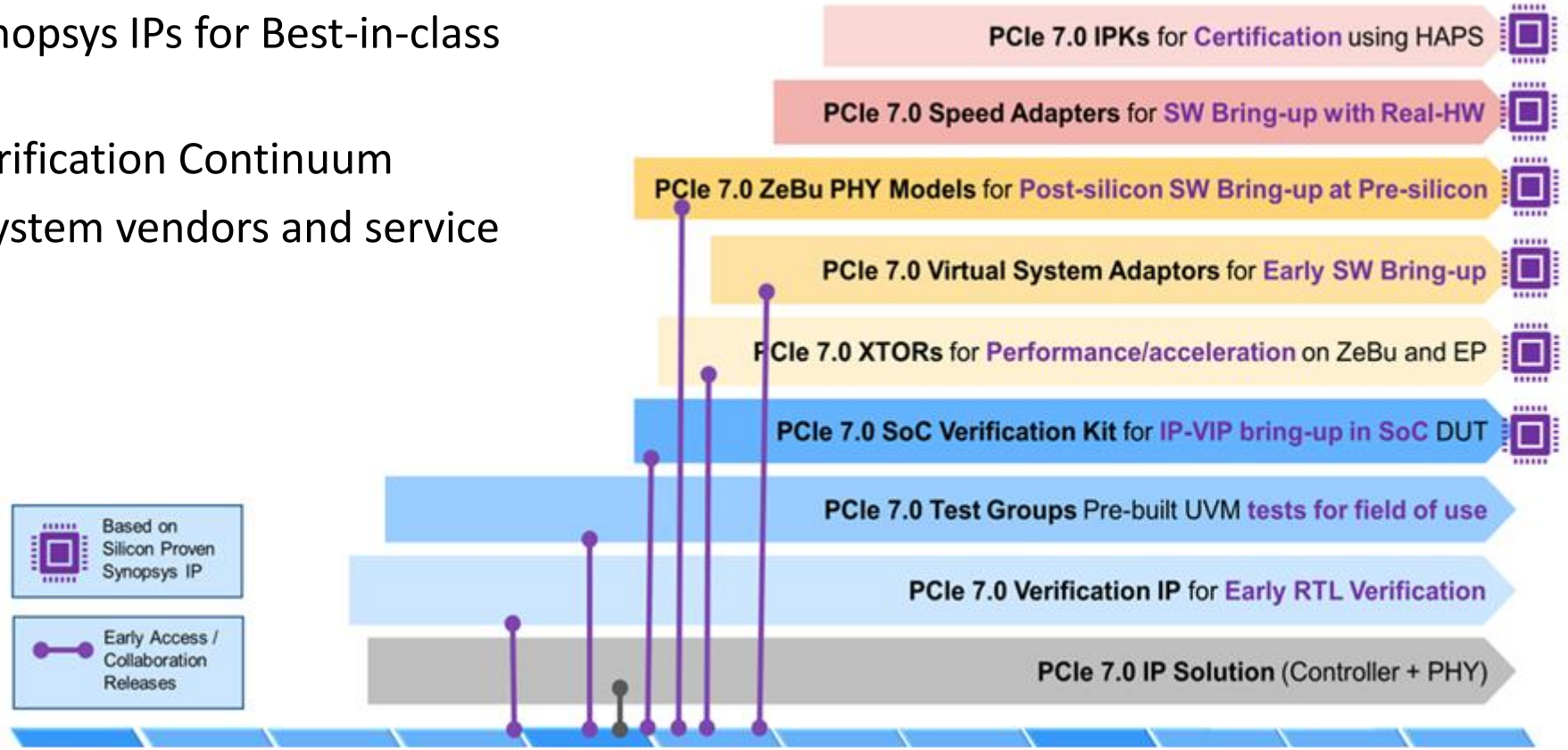
Trends	Top Challenges
Interfaces are evolving faster than ever	High quality **verification IPs and solutions** to match up to the project needs
Custom Silicon and Interfaces to fulfil market needs	Protocol and system **expertise** to support custom designs
More **3rd Party IPs and Subsystems** in the SoCs	IP/Subsystem **sanity and convergence** between teams and partners
AI necessitates **Software-first** workloads	Software first **Test and verification collaterals**
Increasing verification cycles requirement in tradition DV use-cases	Accelerated **Interface solutions to support HAV** for existing DV setups
Test and debug productivity gap is ever increasing	**Test generation** and debug for trillions of cycles

Eco-system Partnership growing both at Customer and EDA vendors to support market demand !

Leading HPC Protocol Solutions for all Use-cases

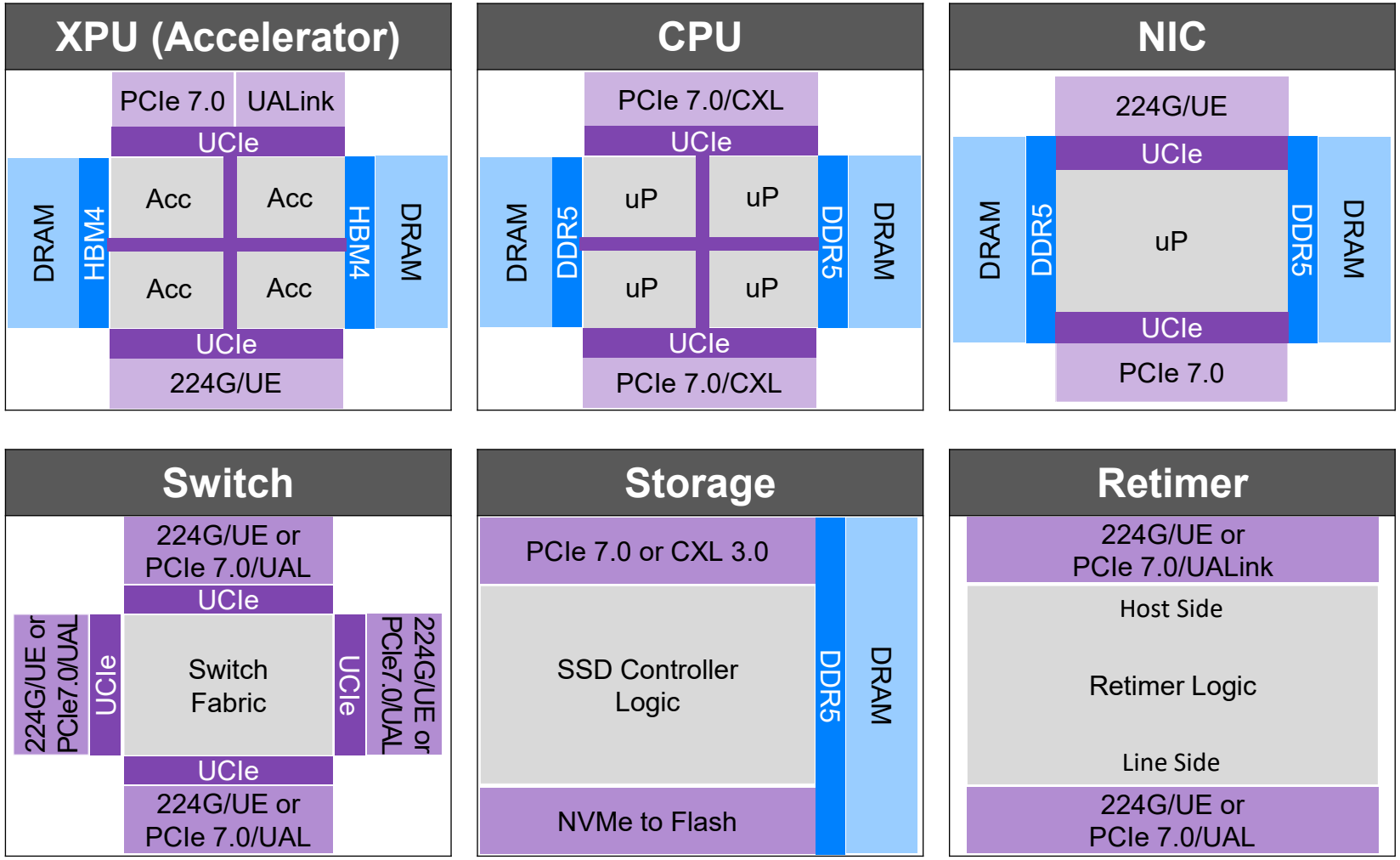
Strong Participation at PCI-SIG and Early Collaboration with Market makers

- Industry 1st VIPs and Protocol Solutions
- Leveraging Silicon Proven Synopsys IPs for Best-in-class QoRs
- Shifting left with Protocol Verification Continuum
- Collaboration with key eco-system vendors and service partners



Primary Interfaces in Data Center SoCs

Synopsys Provides VIPs and Protocol Solutions for all Interfaces and Usages

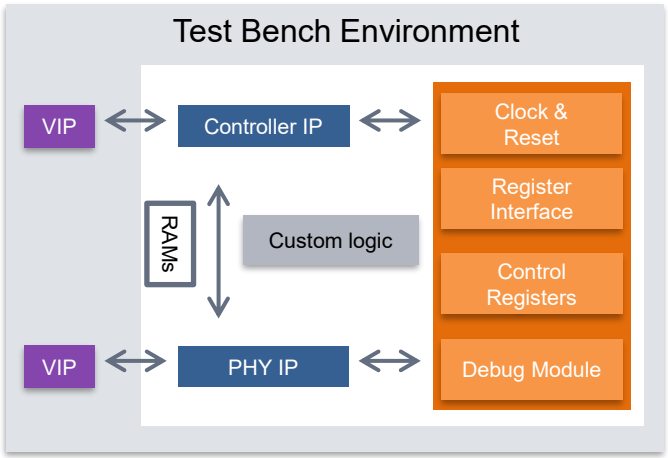


	PCIe	CXL	ENET	Mem	D2D	UAL
XPU	✓		✓	✓	✓	✓
CPU	✓	✓		✓	✓	
Switch	✓	✓	✓		✓	✓
NIC	✓		✓	✓	✓	
Storage	✓	✓		✓		
Retimer	✓	✓	✓			✓

Reduce SoCs Tape-out Risks with Synopsys VIPs/IPs

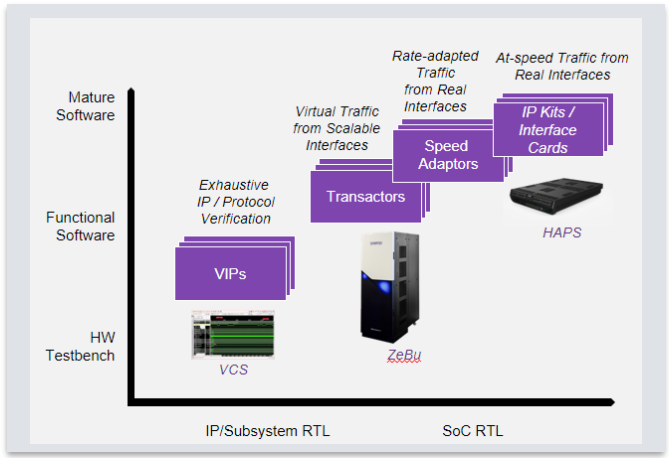
IP/Vendor Selection

- Broadest IP VIP portfolio
- Pre-tested, silicon-proven IP Subsystems for your SoC
- IP & SoC experts configure and customize to your requirements



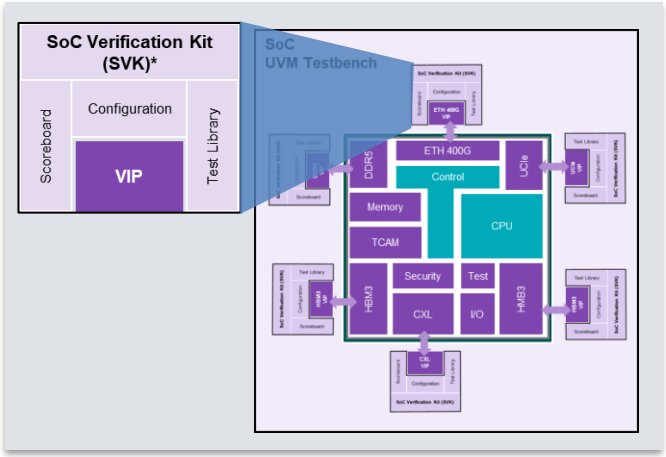
IP Qualification

- Active engagement with spec bodies and eco-system partners
- Ready-to-go Compliance test suites for IP qualification
- Frees your team to work on your product differentiation



IP Integration

- Reference flows and services for IP integration and convergence between project teams
- First-time-right SoC integration speeds TTM



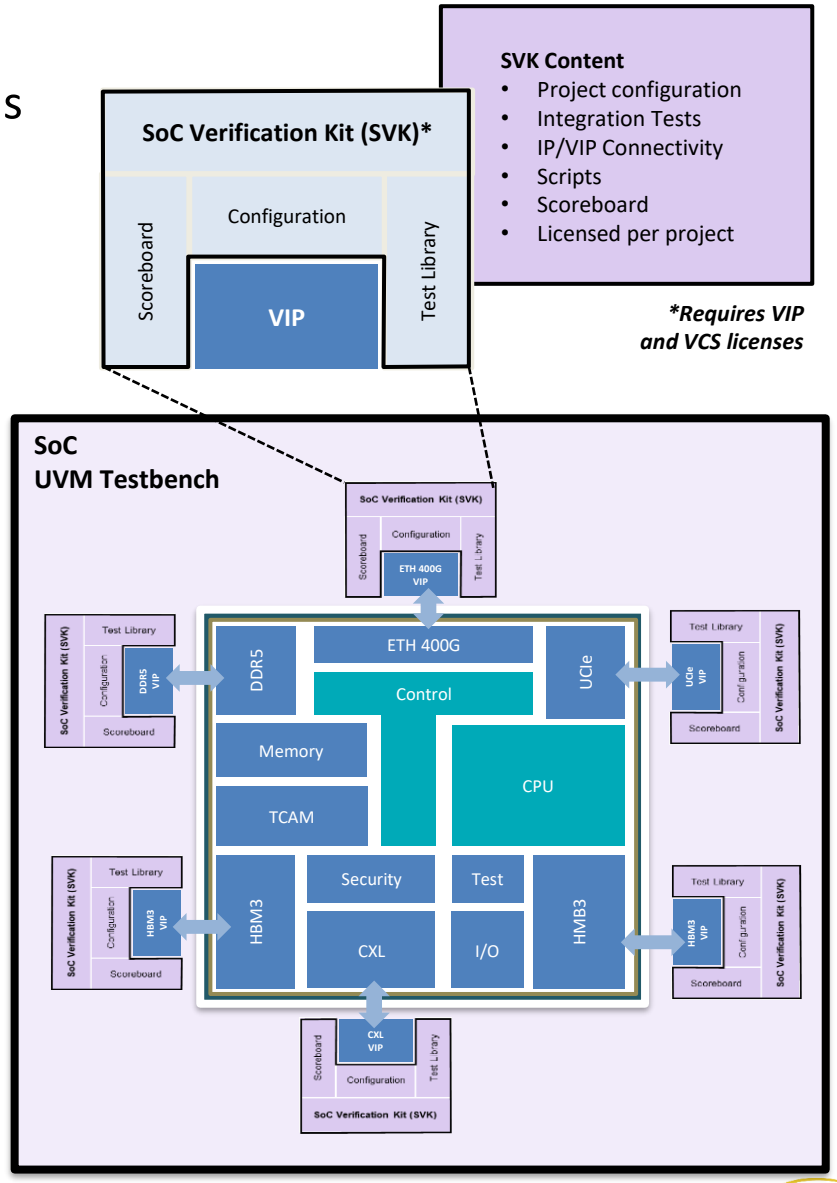
Synopsys SoC Verification Kit (SVK)

Accelerating SoC Verification with Synopsys IP, Protocol Solutions and Platforms

- Challenges
  - Expertise for scalable UVM/C/Application testbenches
  - Verification resource limitations

- SVK Benefits
  - Out-of-the-box verification solution for complex protocols
  - Tailor made for project-specific IP configuration
  - Accelerates the SoC testbench development
  - Enables testing of Synopsys IPs or IP subsystems in Subsystem/SoC environment
  - Lowers integration risk through proven verification methodologies
  - Offered in VIPs, XTORs, Virtual System Adaptors and other flavors

- Differentiated offering helping reduce IP Sanity and SoC bring-up cost and efforts by 50% or more

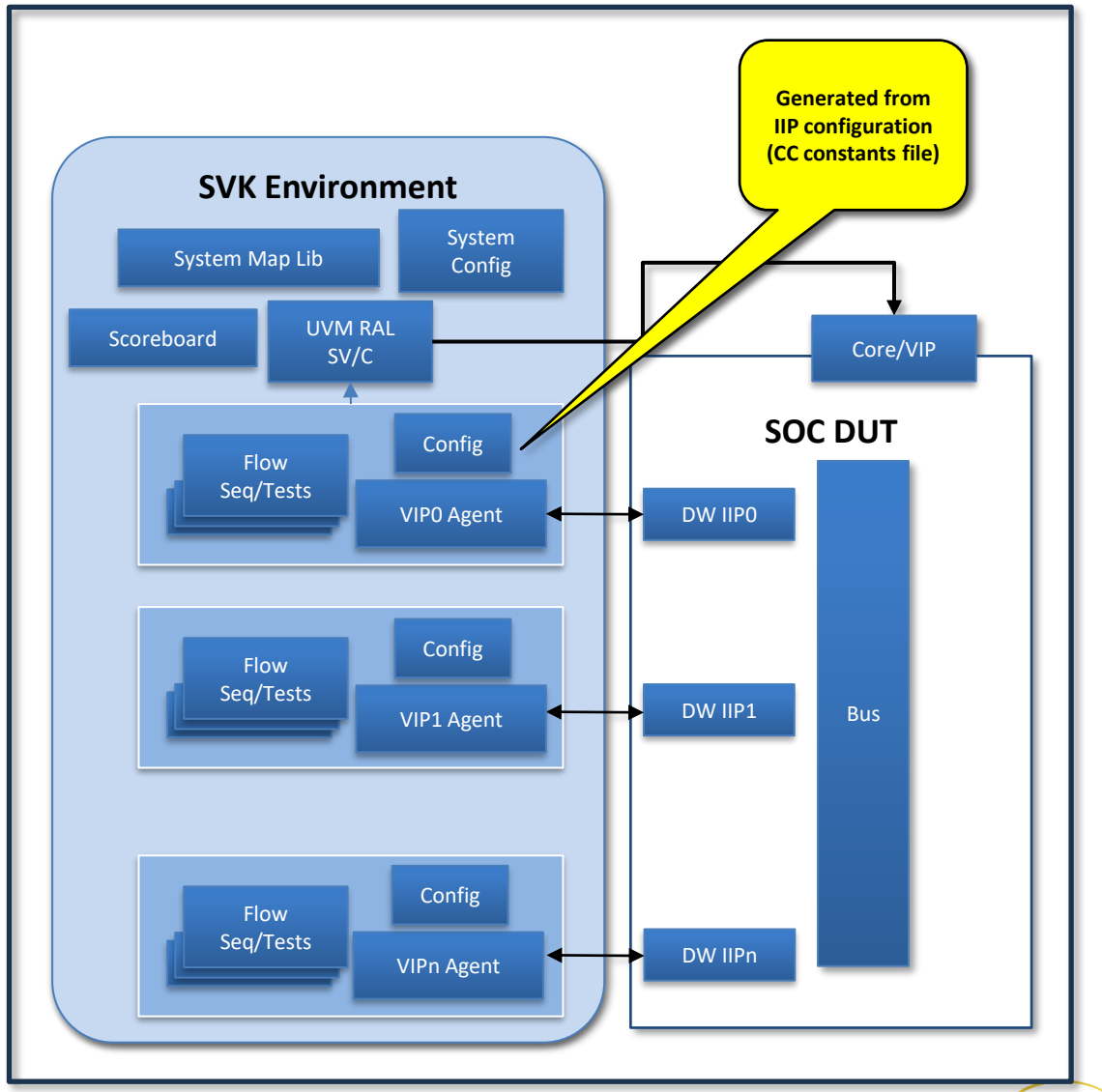


SVK SOC Integration Flow

Customizable per customer environment requirements

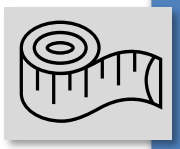
- SVK Integration Flow
  - Environment generation
  - Configuration generation from IIP config
- Flow Sequences
  - IP-VIP setup/sequences
  - Extracts configuration from IP
  - RAL based configuration APIs

Feature ID	Solution feature	Target Value Add
A	SoC Integration framework functionality	TB Bring Up, Easy Integration.
B	RAL model	IP configurability
C	AXI bus	Standard scalable environment
D	Glue logic, wrappers	Verification reuse
E	IP, VIP design, Tests	Interoperability



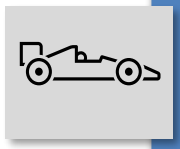
Expert Protocol Services

Helping Customers Meet Their Project Goals Through Specialized Services



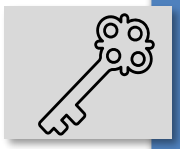
Customization / Custom Interfaces

- VIPs/Solutions for Non-roadmaped or Proprietary or Customizations to standard Interfaces
- NDA Adhered – Fees/Resource/T&M aligned SoWs
- Ex – AMBA CHI customization for China Mobile Company



Roadmap Acceleration

- Re-aligning resources to accelerate Roadmap of Standard VIP or Solutions to meet Customer Project needs
- Collaboration Fees – Customer Timelines - SoW defined
- Ex – 6+ Months roadmap acceleration for LP6/DFI for China EV



Project Consulting

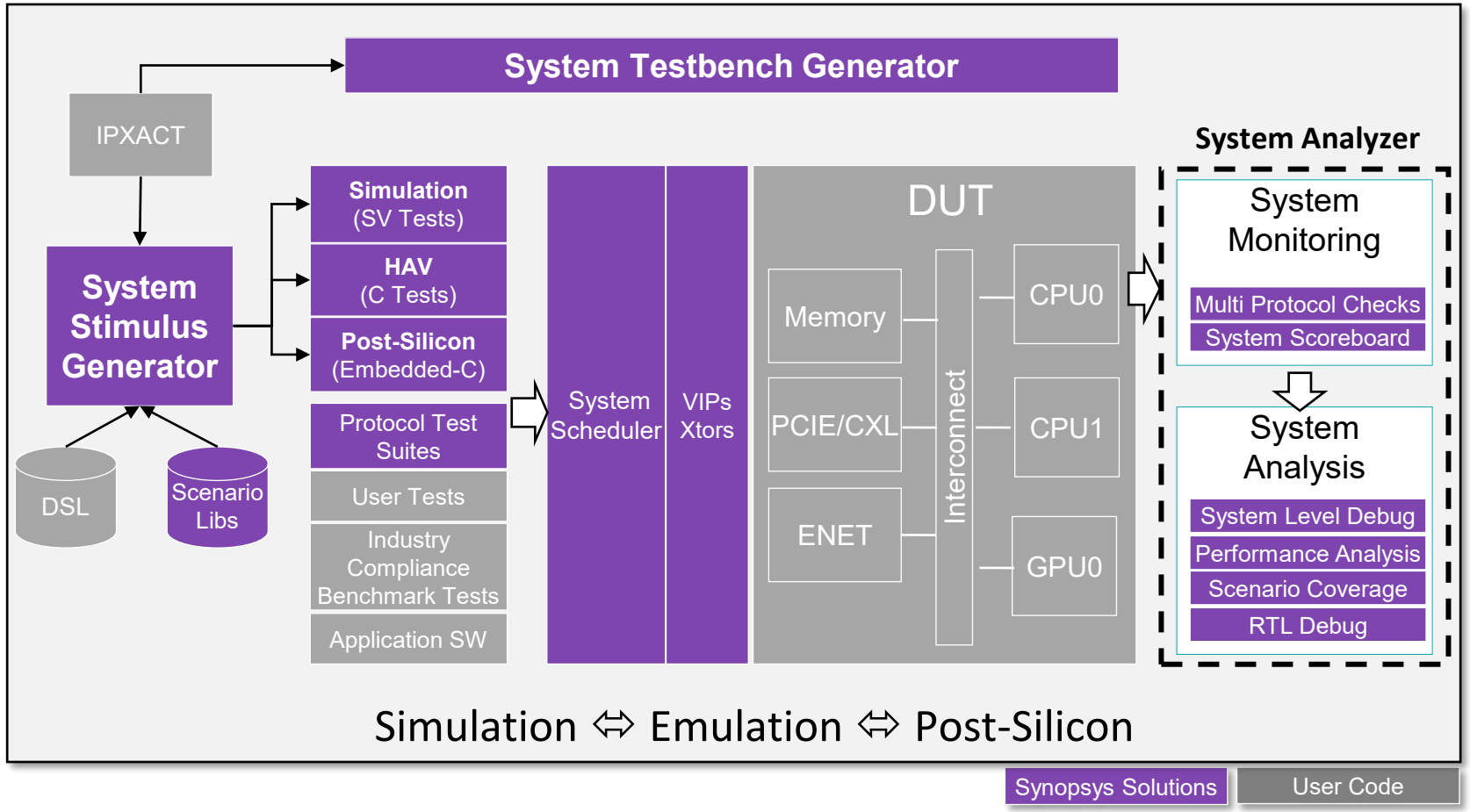
- Turn-key IP/Sub-systems/SoC Verification Services
- Verification Plan Driven – Fixed Fee – SoW-tied Deliverables
- Ex – Ethernet Subsystem Verification for Japanese Auto Company

Trainings / Hand-holding / IP-VIP Interops

- Specialized bring-up assistance – Protocol/Tool training – Additional Verification collateral
- Pre-paid fees for Fixed-days through Costart
- SVKs can also be considered for IP-VIP-TS Interops
- Ex – Add-on scenario specific testcases for Taiwanese Mobile Giant

Cross-platform System Verification and Test Solutions

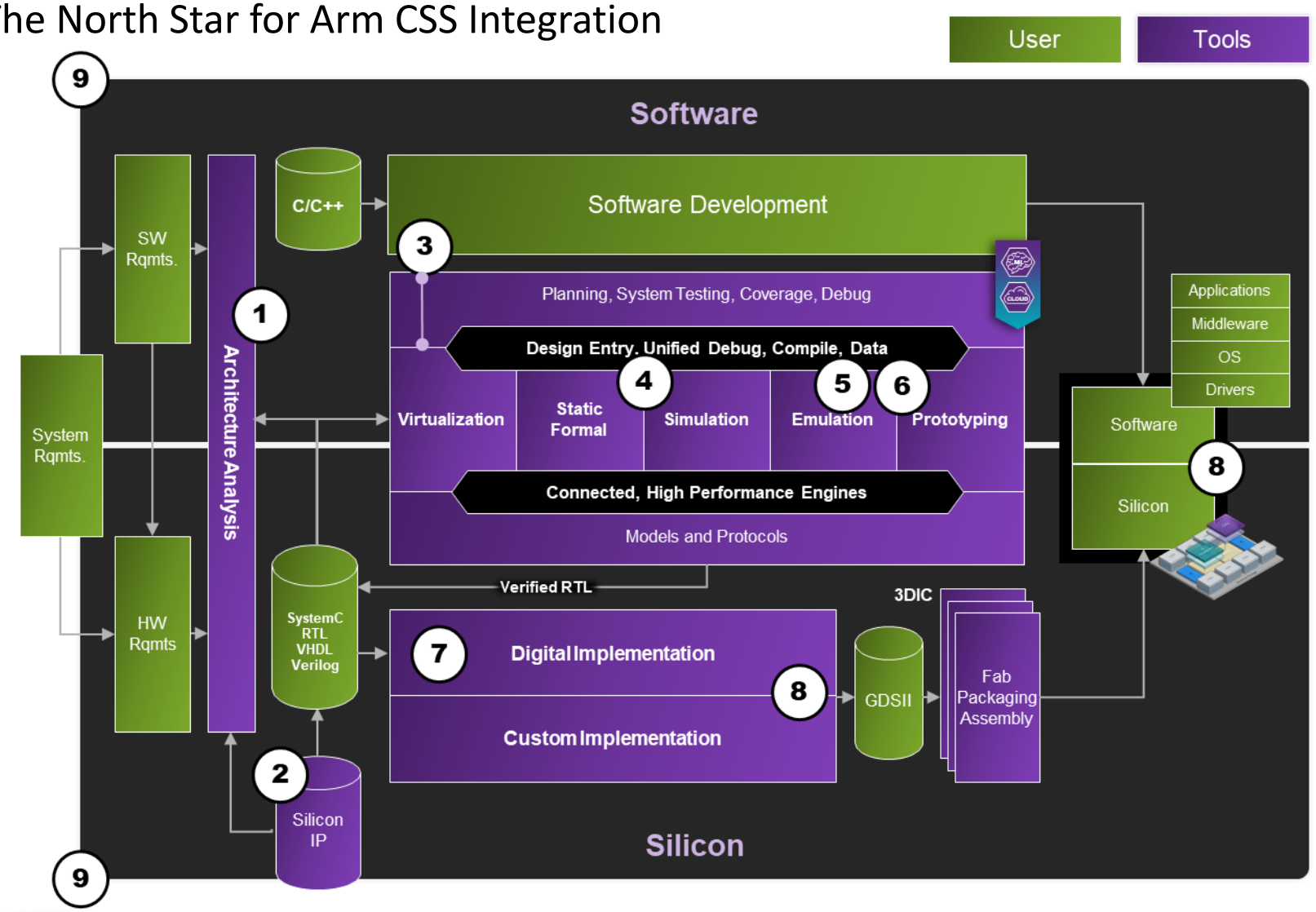
Efficient Configuration, Generation, and Analysis of System Scenarios



- Scalable testbench generation for IP/sub-system/system
- Ready-to-use system traffic generation portable across platforms
- System level data integrity checks
- System level debug and performance analysis
- Flow continuity across platforms from Pre-silicon to Post-silicon

Arm CSS - Ready Silicon to Systems Design

The North Star for Arm CSS Integration



1. Architecture Analysis for Arm CSS
2. Arm CSS-Ready IP Portfolio
3. Virtual Prototypes for Arm CSS SW Dev
4. Arm CSS/IP/VIP Integration Verification
5. Arm CSS in System V&V, Perf, Power
6. Arm CSS SW at high fidelity (Emu/Proto)
7. Arm CSS PPA Optimization
8. Silicon Lifecycle Management
9. Expertise & Services

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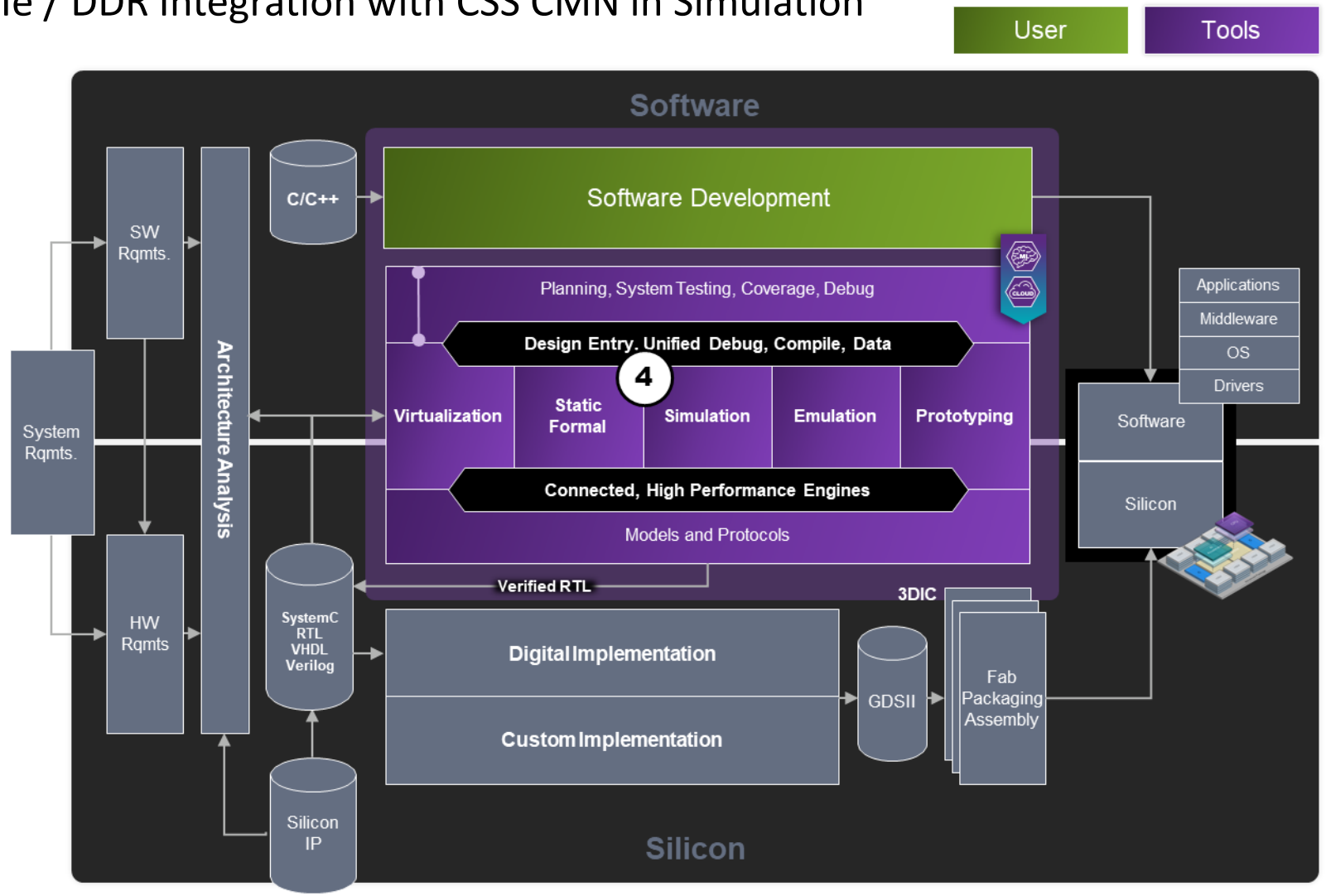
VIP / IP / CSS (Platform) Integration Verification

PCIe / DDR Integration with CSS CMN in Simulation



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Protocol Solutions for Chiplet Platforms

PCIe, CXL, USB, HBM, UCIe, …

arm — Arm CSS RTL

SYNOPSYS® — Synopsys VIP, IP
ZeBu™, HAPS™, VCS™

Exhaustive IP / Protocol Verification

VIPs

VCS

- IP & Blocks
- New Protocols
- UVM Coverage Closure

Virtual Traffic from Scalable Interfaces

Transactors

ZS5 or ZeBu EP1/2

- SoC-level
- New Protocols
- HW/SW Bring-up
- Performance &Power
- SW/HW

Rate-adapted Traffic from Real Interfaces

Speed Adaptors

ZS5, ZeBu EP1/2, HAPS-100

- HW/SW Bring-up with high fidelity
- Drivers
- Interoperability

At-speed Traffic from Real Interfaces

Protocol Interface Cards/IPK

ZeBu EP1/2 or HAPS-100

- Controller + PHY Integration
- Driver Compliance
- Protocol IP Certification
- At-Speed Interoperability Testing

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Summary

- AI is rapidly changing the infrastructure requirements from both hardware and software
- Existing interfaces are evolving, and new interfaces are getting formed to support insatiable data computation and transfer needs
- Design, verification, and test productivity has not caught up
- Verification solutions need to evolve to support increasing design capacity, evolving protocol interfaces, peta-cycle payload generation and debug, software-first methodologies, and ip-to-soc and tool-to-tool convergence
- Synopsys VIP and protocol solutions' vision is aligned to support these emerging requirements through industry first VIPs, IP-tied end-to-end protocol solutions for quality and convergence, and pre-to-post silicon continuum

THANK YOU