

# Verify your next AI/ML design with Questa One Avery VIP

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## Abstract:

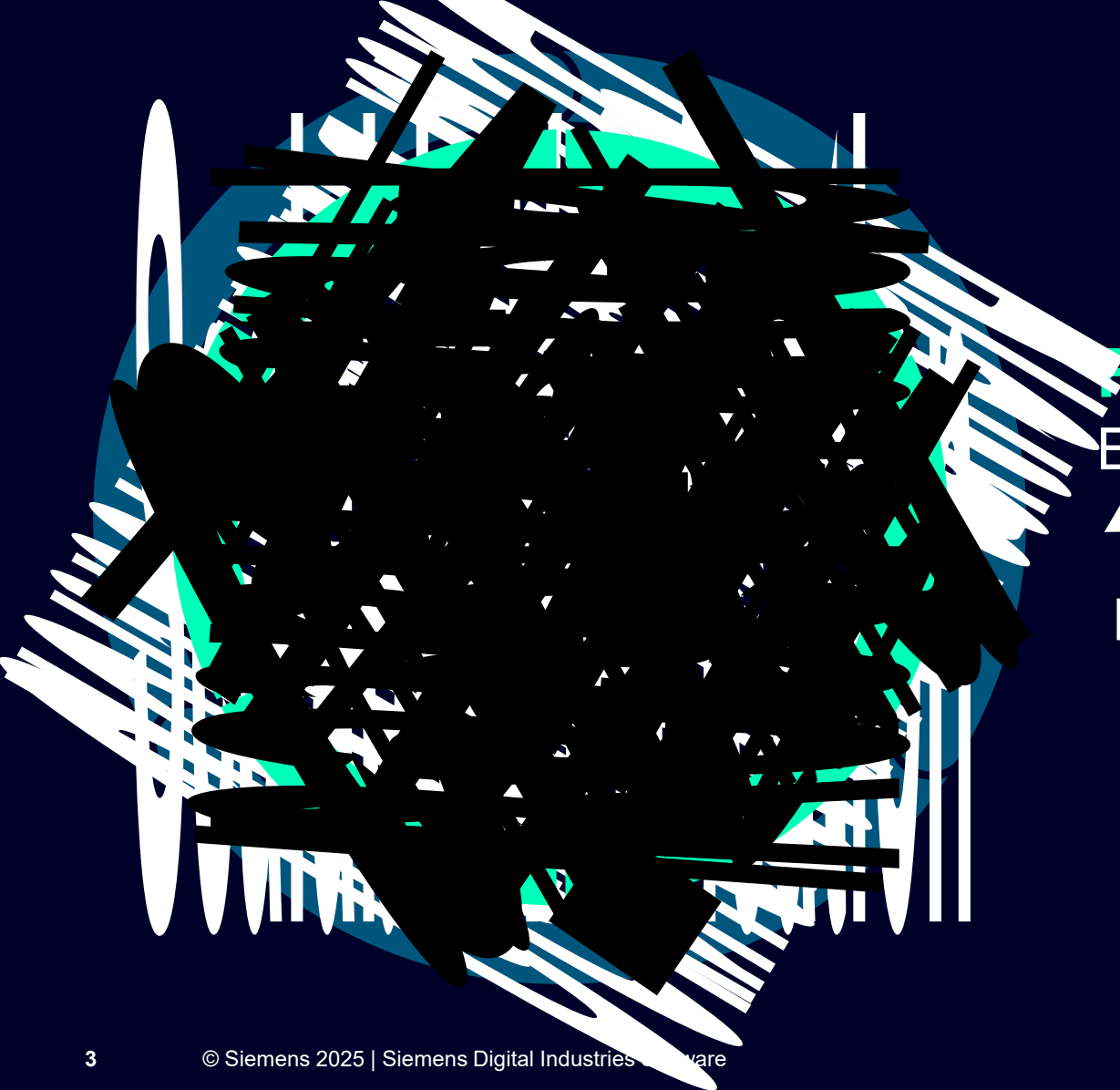
This session will highlight the new capabilities and new advanced High-Performance Compute protocols we introduced in 2025 as part of **Questa One Avery Verification IP** launch.

These new Verification IP protocol models and Compliance Test Suites for **Ultra Accelerator Link (UALink)**, **Ultra Ethernet (UEC)**, and **PCIe Gen7**, are needed by any AI/ML design in 2025.

In addition, we describe our new **Questa One** productivity tools including **Protocol Debug** for enhanced productivity during regression debug, and **Test-suite Configurator** for VIQ-based accelerated coverage closure of your interfaces.

# Questa One – Siemens' Smart Verification Solution enabled by AI

Improving user productivity through the collective power of technology



**Faster**  
Engines



**Faster**  
Engineers



**Fewer**  
Workloads

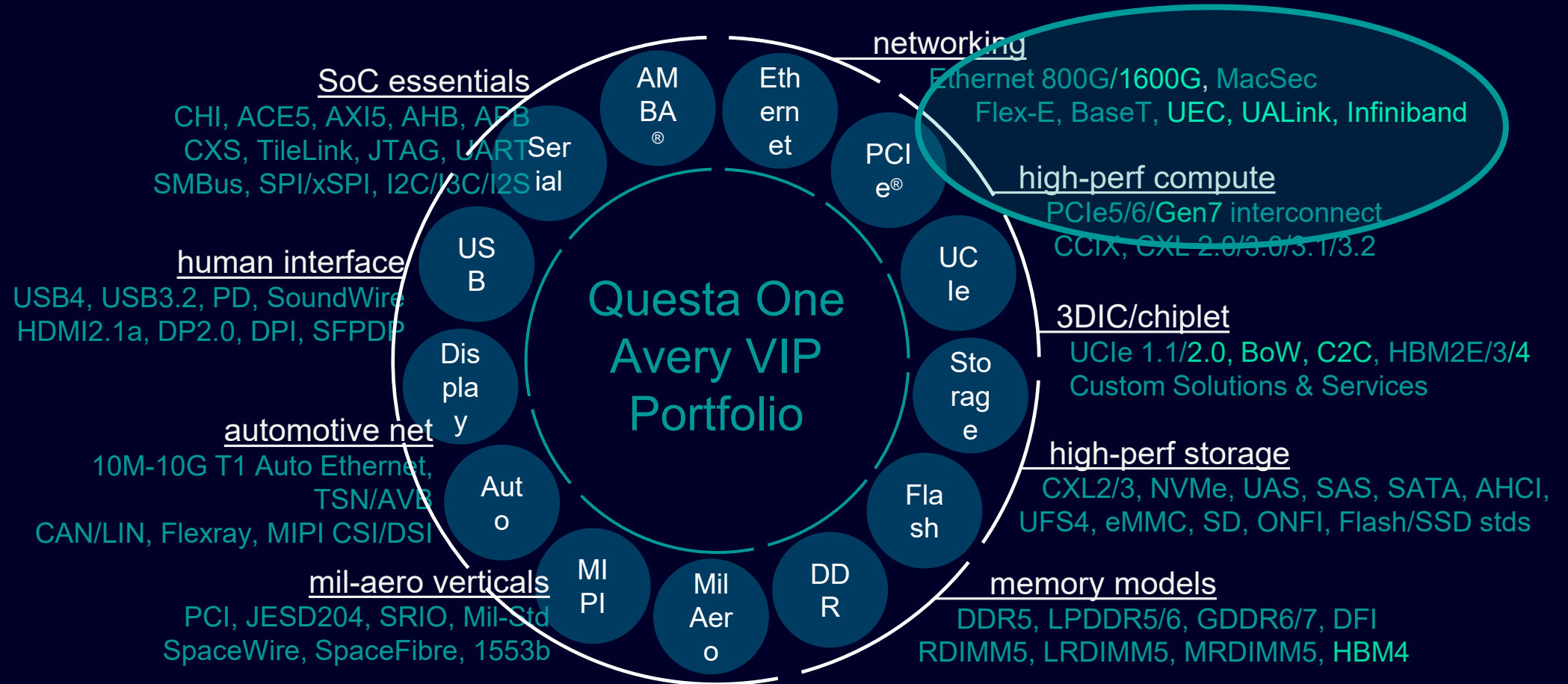


Delivering up to **5x** improved  
**Total User Productivity**



# Questa One Avery VIP - Delivering Accelerated Confidence

- First-to-market investment builds quality and depth
- Fast Architecture SV/UVM, random, runs on all engines
- Sim Acceleration on emulator and prototype system
- Software Aware co-simulation with QEMU/AFM
- Multiple IP Partner testing on many controller designs
- Finds Design Bugs that others miss by running CTS
- AI/ML Roadmap with future-proof packaging
- Broad Portfolio Verification IPs + Compliance Tests



# Questa One Avery VIP – Ethernet 1.6T 802.3dj – The Foundation

First-to-market investment builds quality and depth

Fast Architecture

Sim Acceleration

Software Aware

Multiple IP Partner

Finds Design Bugs

AI/ML Roadmap

Broad Portfolio

## Ethernet 1.6T VIP Roadmap:

- 1.6T/800G – 802.3dj – support for all lane configurations and inner FEC features
- the foundation for UEC and UALink

“you are seven months ahead of the competition”  
– Customer A

### Easy Integration with :

- Full UVM support
- Connectivity Modules & Agents

### VIP Features

- Multiple Callbacks/Analysis Port
- IOL compliance Tests –MAC, PHY & RS-FEC
- Debug
  - 100s of Assertions (Checklist)
  - Multiple Tracker files – MAC, PCS & PMA
  - Transaction Recording with Visualizer
- MACSEC Features

- IEEE 802.3 2022 & IEEE 8023df-2024.pdf & IEEE8023dj\_D1p2.pdf
- Full Speed Support from 10Mbps to 1.6T including Automotive (T1) Ethernet
- MAC: framing, addressing, Application and error detection
- RS-FEC (544,514), RS Codeword Interleaving
- Circular shift, Hamming code, BCH(CL184), Frame sequence and Padding
- RS-FEC(528,514), LL –RS-FEC
- Support a MAC data rate upto 1.6 Terabit/s
- PMD Link Training
- Auto speed resolution using Auto Negotiation
- PMA: Inner FEC, Symbol-Quartet Muxing, clock and data recovery
- Support for Ultra Ethernet in future Release

# Questa One Avery VIP – PCI Express Gen7 – The Foundation

First-to-market investment builds quality and depth

Fast Architecture

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## PCIe Gen7 1.0 Specification – June 2025 support

- Foundational for UALink, CXL
- Avery PCIe VIP and Compliance Test Suites leading the market since 2015

“you find PCIe bugs in 3<sup>rd</sup> party design IP that other VIP misses”

— Customers B, C, D

### PCIe Gen7.0r0.7/0.9/1.0 spec:

- Engaged with Early Access customers
- 128GT/s data rate
- PIPE 7.0, 160-bit Serdes Interface supported
- Full / Bypass / No equalization
- I-EIEOS supported
- TS1/TS2 update
- Complete Security Stack: SPDM,IDE KM,IDE,TDISP

### Broad customer availability TODAY

- Typically, VIP available 2 weeks after spec

# Questa One Avery VIP – Ultra Accelerator Link (UALink)

First-to-market investment builds quality and depth

Fast Architecture

Sim Acceleration

Software Aware

Multiple IP Partner

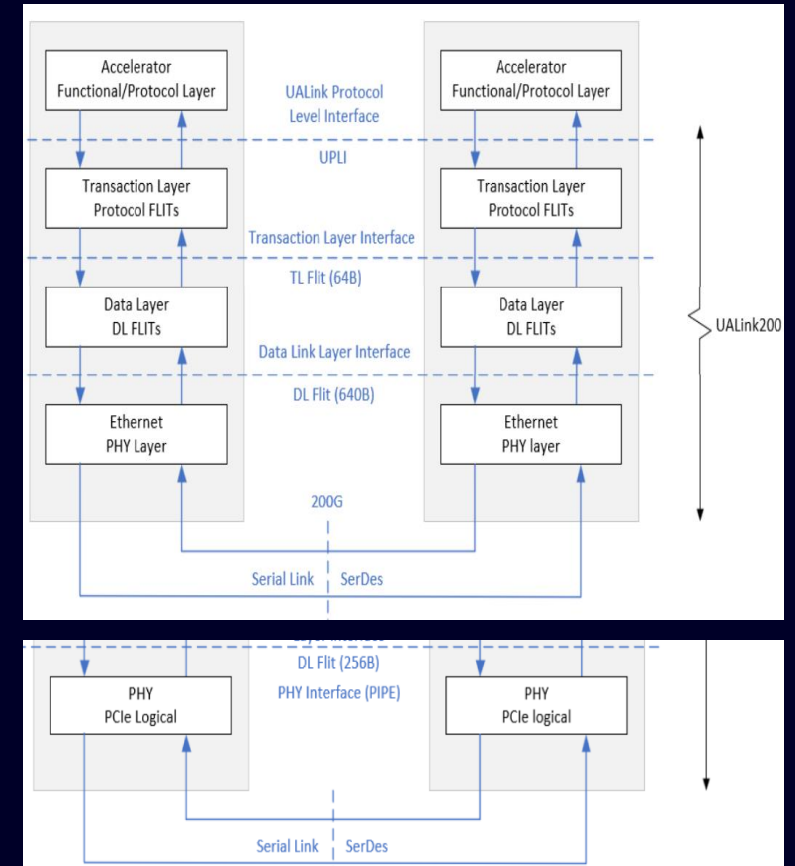
Finds Design Bugs

AI/ML Roadmap

Broad Portfolio

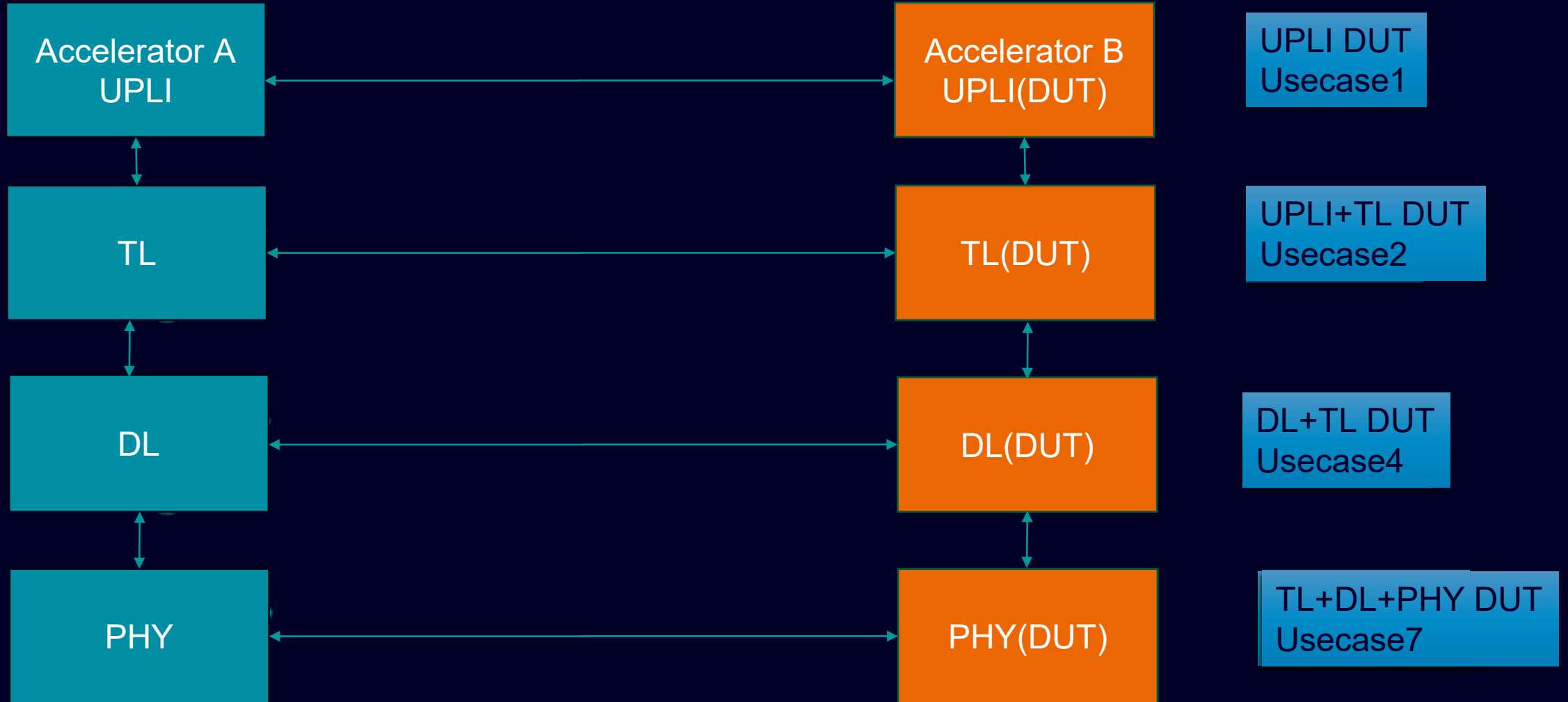
UALink enables direct, fast GPU to GPU load/store/atomic operations:

- Both Ethernet based and PCIe based transport – Infinity Fabric protocol
- Working with 4 lead customer/partners
- Full stack available with Ethernet/PCIe, which includes
  - CTS, Assertions
  - Callbacks, Error Injection
  - Trackers, Scoreboard
  - Security
  - Functional coverage
  - Layer-wise verification

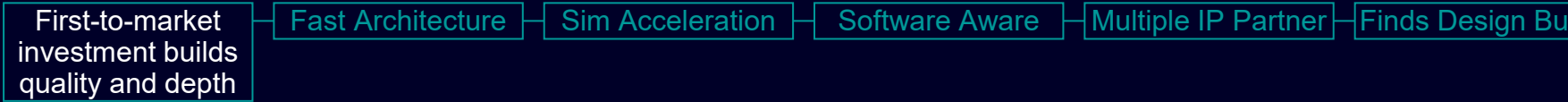


# UALINK Usecases

First-to-market investment builds quality and depth — Fast Architecture — Sim Acceleration — Software Aware — Multiple IP Partner — Finds Design Bugs — AI/ML Roadmap — Broad Portfolio



# Questa One Avery VIP – Ultra Ethernet (UEC)



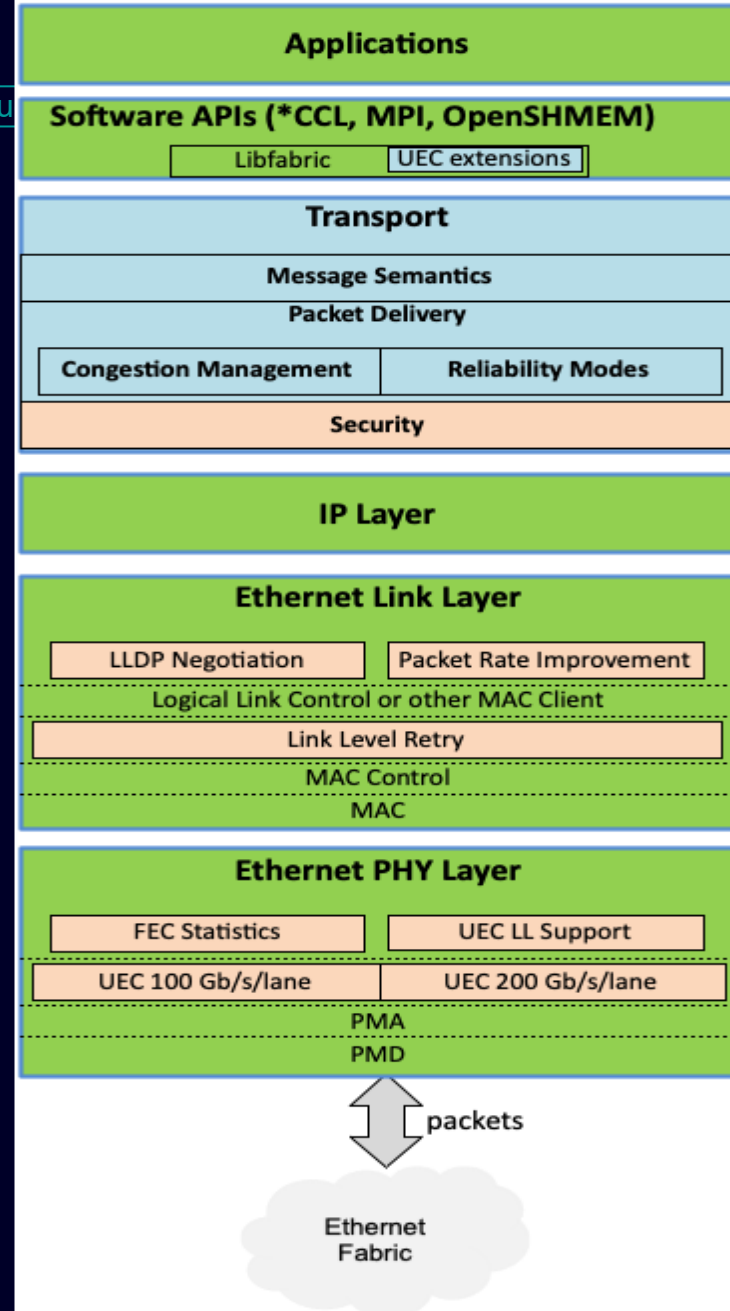
## Ultra Ethernet v1.0

- Updated Transport, link, and physical layer to meet AI workload demands.

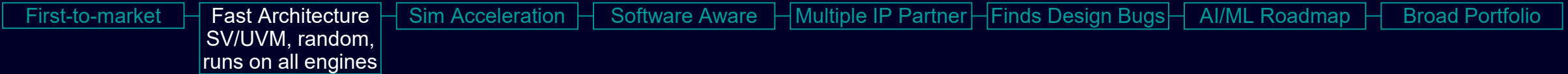
## Ultra Ethernet Transport (UET)

- Open protocol spec, purpose-built to run over IP and Ethernet
- Advanced network security with an optional security layer at transport.
- Aligns with 1.6T Ethernet scalability and energy efficiency goals

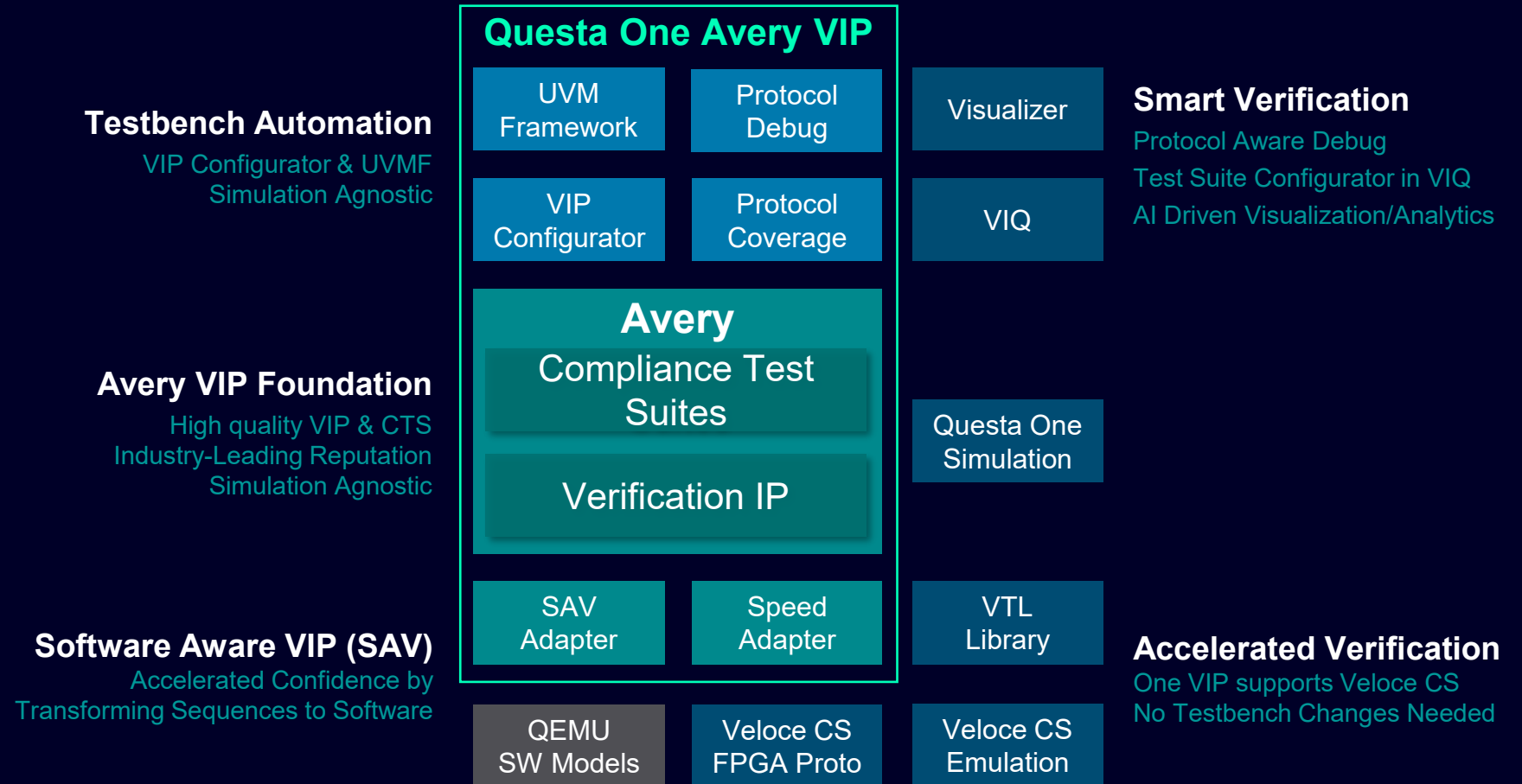
# UEC Stack



# Questa One Avery VIP - Architecture



- Simple Architecture
  - Native SV/UVM
  - Fast Implementation
  - Constrained Random
- Tool / Flow Integrations
  - Visualizer Debug
  - VIQ Plan/Coverage
- Multiple Engine Support
  - Questa, VCS, Xcelium
  - Veloce Acceleration
  - Veloce Prototyping
- Software Support
  - QEMU and AFM



# Questa One Avery VIP - Protocol Aware Debug

First-to-market

Fast Architecture  
SV/UVM, random,  
runs on all engines

Sim Acceleration

Software Aware

Multiple IP Partner

Finds Design Bugs

AI/ML Roadmap

Broad Portfolio

## Easy to Debug – Questa One Protocol-Aware Debug combines VIP and Visualizer

- Visualize the Protocol Tracker logfile
- Decoder ring for complex traffic
- Waveform window protocol support
- View transactions alongside signals
- Protocol State Machine view
- visualize BFM state / memory state

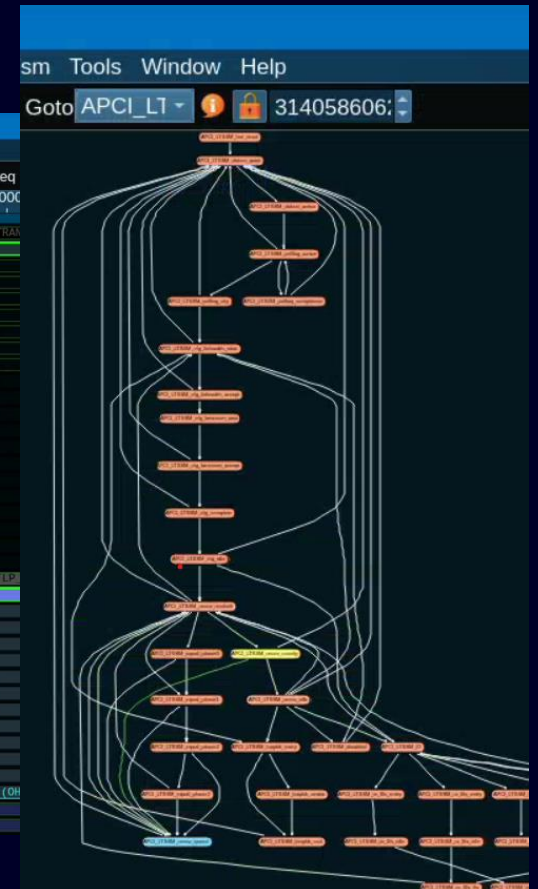
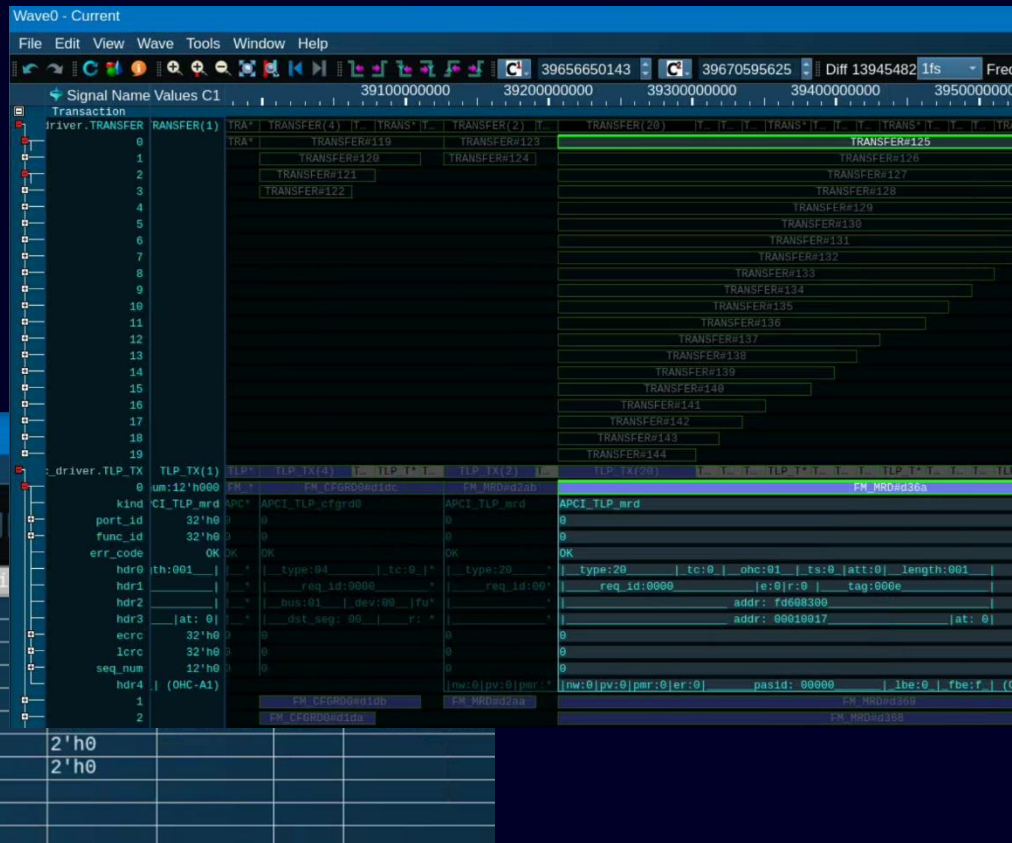
Composition - CM\_TRANSFER

File Edit View Tools Window Help

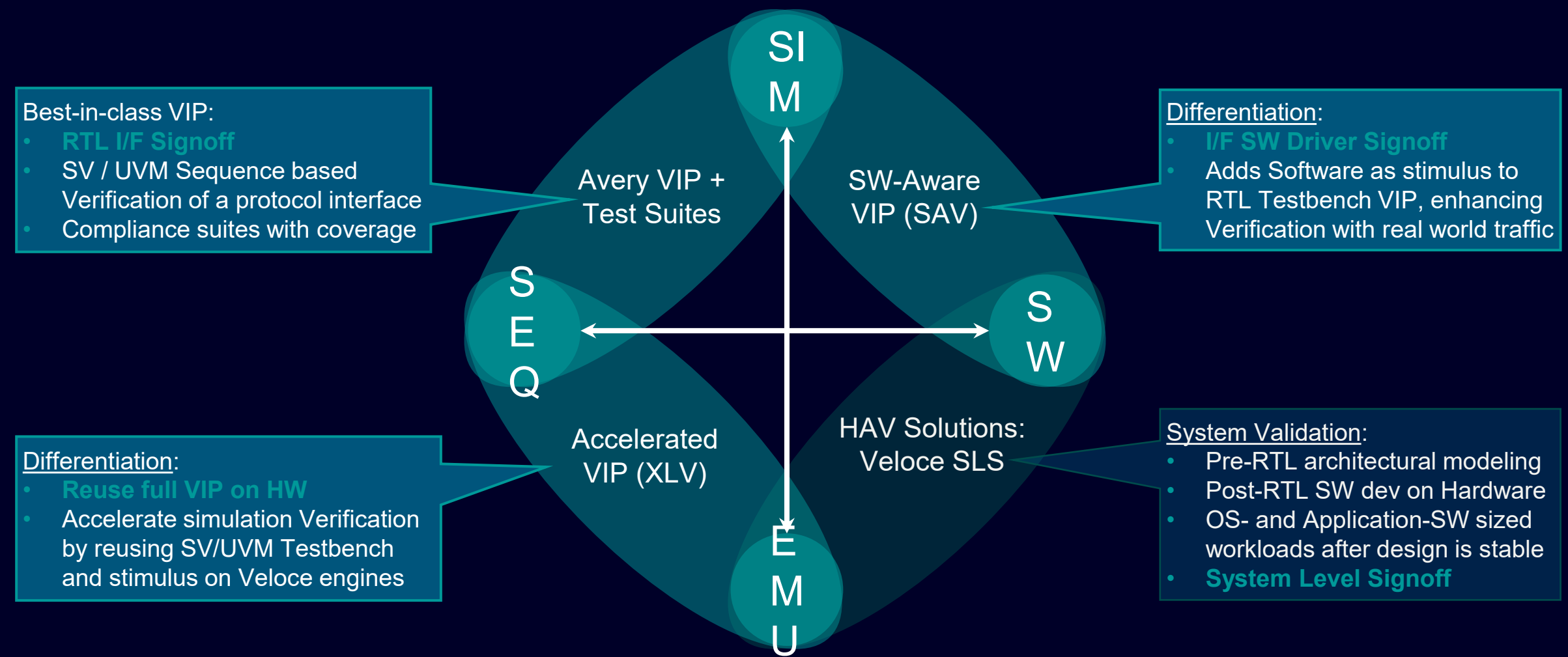
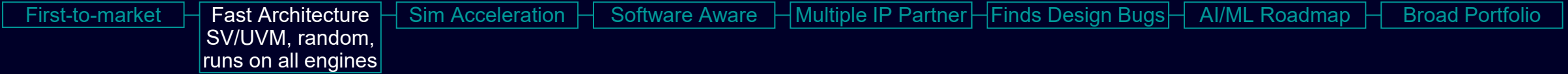
Expr:

Time: Show Transactions with time After Before Filter Search

Time (1fs)	Stream	valid	SnpType	MetaF1
42195096625 - 42331095625	CM_TRANSFER			
42195096625 - 42331095625	ACXL_MSG_m2s_req_TX	1'h1	3'h3	2'h0
42323591000 - 42331094625	ACXL_MSG_s2m_nldr_RX	1'h1		2'h0
42323591000 - 42331095625	ACXL_MSG_s2m_drs_RX	1'h1		2'h0
42195106625 - 42331101625	CM_TRANSFER			
42195106625 - 42331101625	ACXL_MSG_m2s_req_TX	1'h1	3'h3	2'h0
42323591000 - 42331096625	ACXL_MSG_s2m_nldr_RX	1'h1		2'h0
42323591000 - 42331101625	ACXL_MSG_s2m_drs_RX	1'h1		2'h0
42195116625 - 42331098625	CM_TRANSFER			
42195126625 - 42347094625	CM_TRANSFER			
42195136625 - 42347098625	CM_TRANSFER			



# Questa One Avery VIP - Beyond VIP



# Questa One Avery VIP - Compliance Test Suites (CTS)

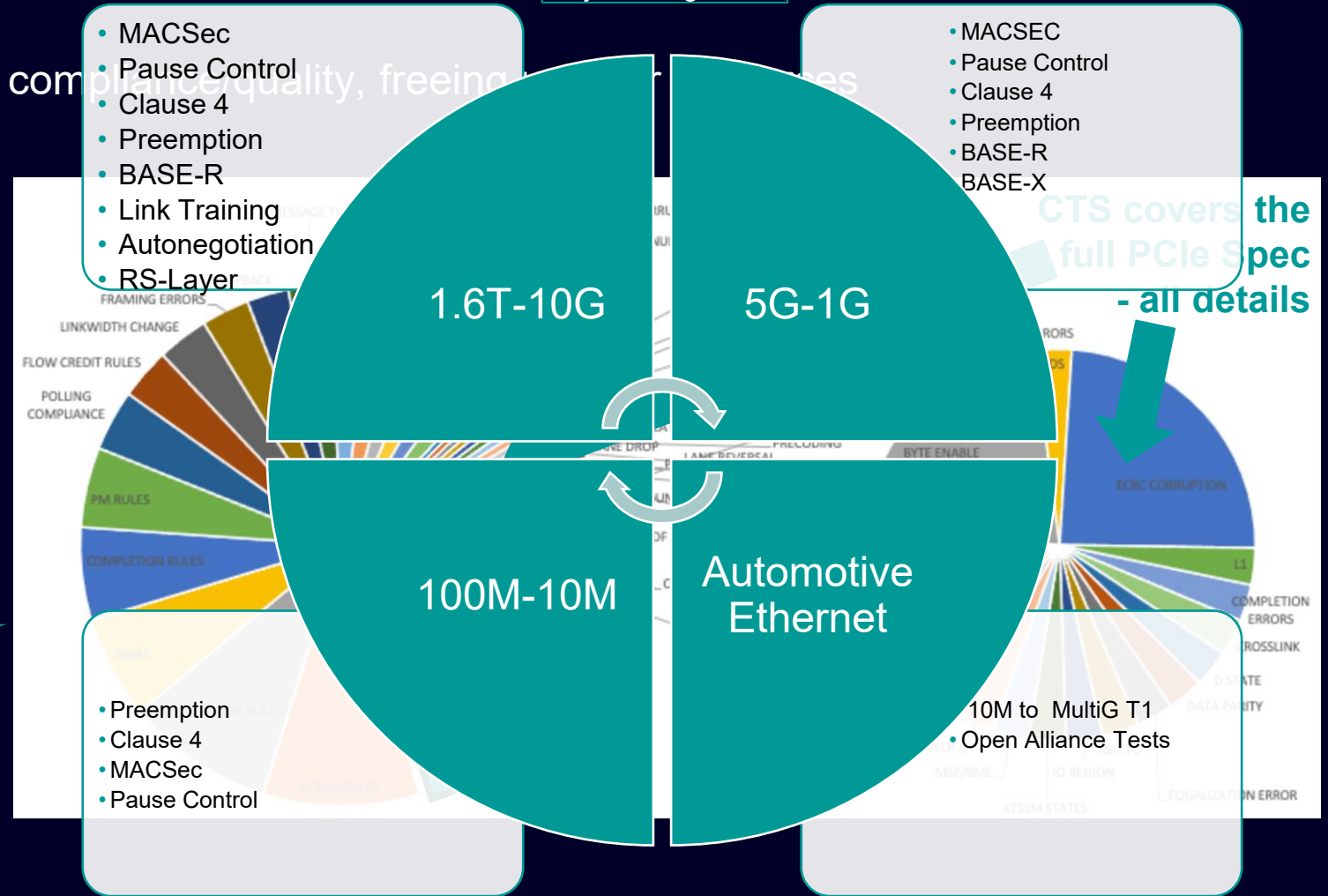
- First-to-market
- Fast Architecture
- Sim Acceleration
- Software Aware
- Multiple IP Partner
- Finds Design Bugs that others miss by running CTS
- AI/ML Roadmap
- Broad Portfolio

Build vs Buy? Rely on Avery VIP+CTS for compliance quality, freeing resources

## Avery Compliance Test Suites:

- Covers whole spec, not just std tests
- Constrained-random SV/UVM code
- Full test plan and coverage model
- Still finding PCIe5 bugs in IP configs
- Industry's signoff VIP / test suite

“you found an IP bug the IP vendor VIP did not catch – with just ONE test”  
– HPC customer



CTS covers the full PCIe Spec - all details

# Questa One Avery VIP - Coverage Closure with Verification IQ

First-to-market

Fast Architecture

Sim Acceleration

Software Aware

Multiple IP Partner

Finds Design Bugs that others miss by running CTS

AI/ML Roadmap

Broad Portfolio

ethernet

- Insight
- Testplan Author
- Regression Navigator
  - Regressions
    - ETH\_800G
    - Ethernet 1.6T
    - Ethernet 800G
    - Ethernet 100G
    - Ethernet 100G Live
    - Ethernet 100G Test
    - Ethernet 800G MAC**
  - Testlists
  - Rules
  - Rank Test Configuration
  - Coverage Analyzer

## Ethernet 800G MAC

**Latest Run**

Run#: 42

Date: 2024-09-02 - 10:03:19

Status: Passed

Actions: 96

Tests: 83

Passed: 83

Failed: 0

Failure Signatures: 0

Result Analysis: 0 messages

Regression Flow: Regression Navigator

Regression Time: 11m 45s (-1s)

Total Coverage: 10.93%

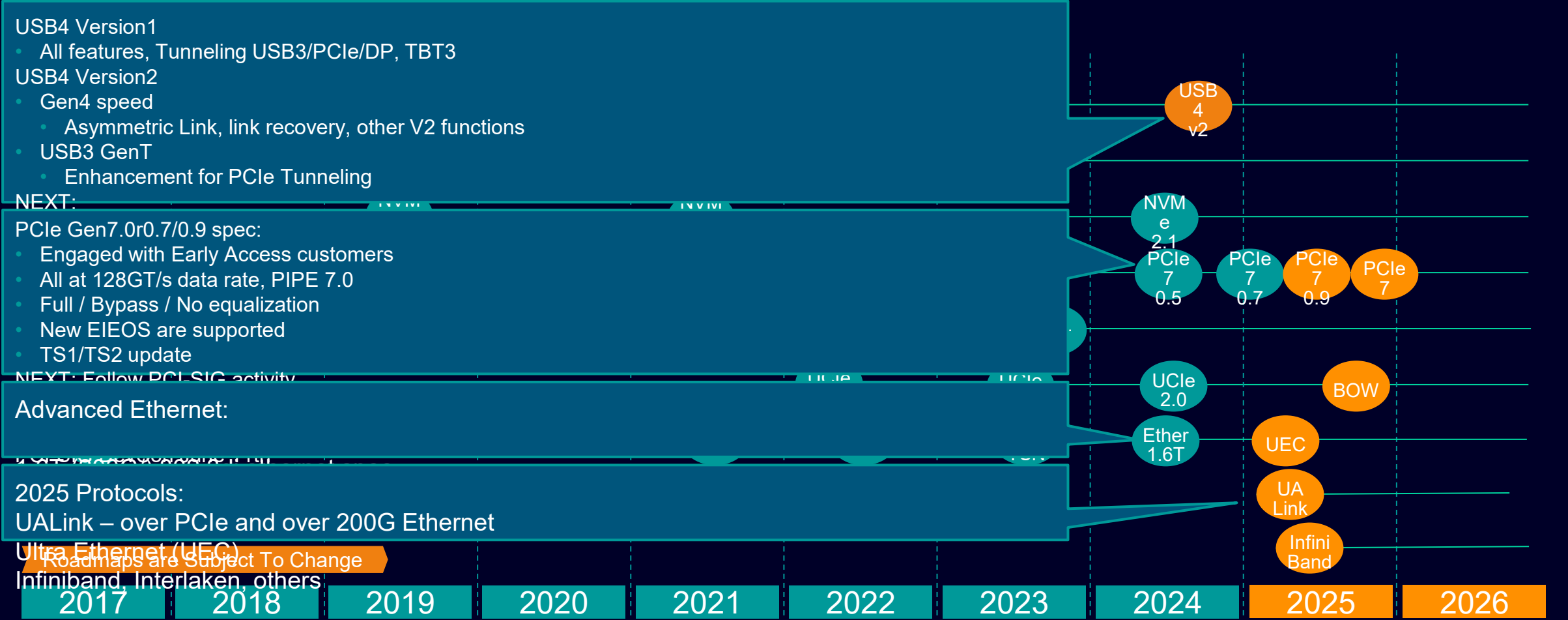
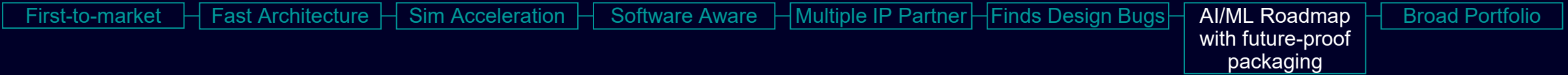
**Tests**

Legend: Total (blue), Passed (green), Failed (red), Failure Signatures (purple)

**Regression Runs**

Run #	Status	Actions	Total Tests	Passed Tests	Failed Tests	Failure Signatures	Not Run	Coverage	Testplan	Duration	End Time	Source Control Revision
42	Passed	96	83 (0)	83 (0)	0 (0)	0	0 (0)	10.93% 0.00%	97.14% 0.00%	11m 45s (-1s)	3d 5h ago	-
41	Passed	95	83 (-)	83 (-)	0 (-)	0	0 (-)	10.93% (-)	97.14% (-)	11m 46s (-)	3d 5h ago	-
40	Launch Failed	0	0 (-)	0 (-)	0 (-)	0	0 (-)	-	-	-	-	-
39	Passed	90	83 (+31)	83 (+83)	0 (0)	0	0 (0)	0.9% (-)	0% (-)	51s (-)	9d 1h ago	-
38	Terminated	53	52 (-)	0 (-)	0 (-)	0	0 (-)	-	-	-	-	-
37	Launch Failed	0	0 (-)	0 (-)	0 (-)	0	0 (-)	-	-	-	-	-
36	Launch Failed	0	0 (-)	0 (-)	0 (-)	0	0 (-)	-	-	-	-	-
35	Passed	97	83 (0)	83 (0)	0 (0)	0	0 (0)	10.95% +0.02%	93.5% +3.93%	11m 46s (0ms)	31d 1h ago	-

# Questa One Avery VIP - Product Roadmaps



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