

Real-Time Handwriting Detection using an AI Model running on HAPS-200

Nilesh Shilankar and Kailas Senan
Product Engineer
Synopsys



Kailas Senan is Principal Engineer at Synopsys with 20 years of experience. His expertise is in FPGA Design and Prototyping.

Nilesh Shilankar is working at Synopsys as Product Engineer and responsible for different feature deployment for FPGA based prototyping and Implementation of users worldwide.

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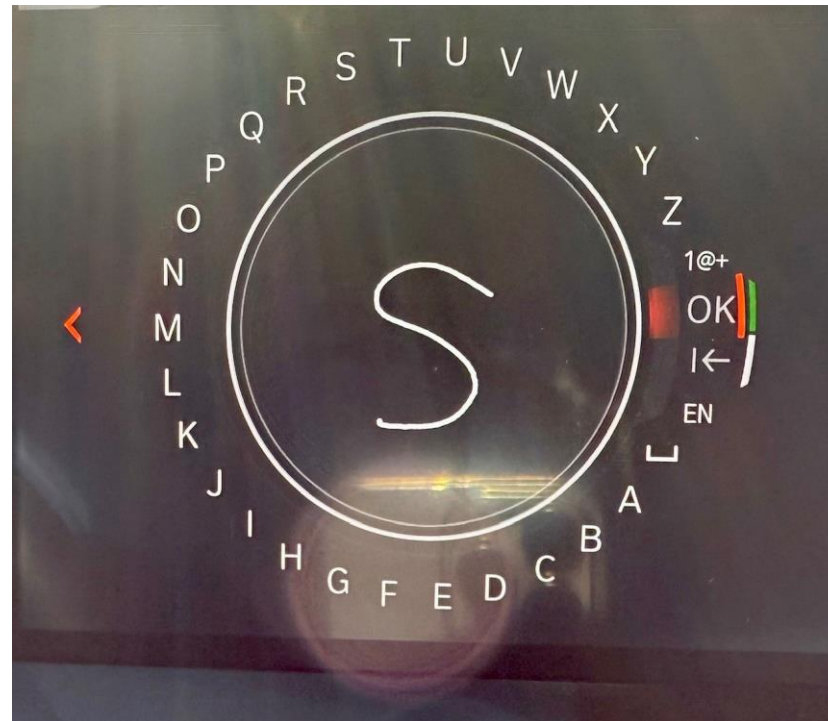
AGENDA

- What is LeNet Handwriting Application ?
- ASIC Prototyping Challenges and Synopsys Solution
- LeNet Design on HAPS-200
- HAPS real-time AI inferencing demo
- Key Takeaways
- QA

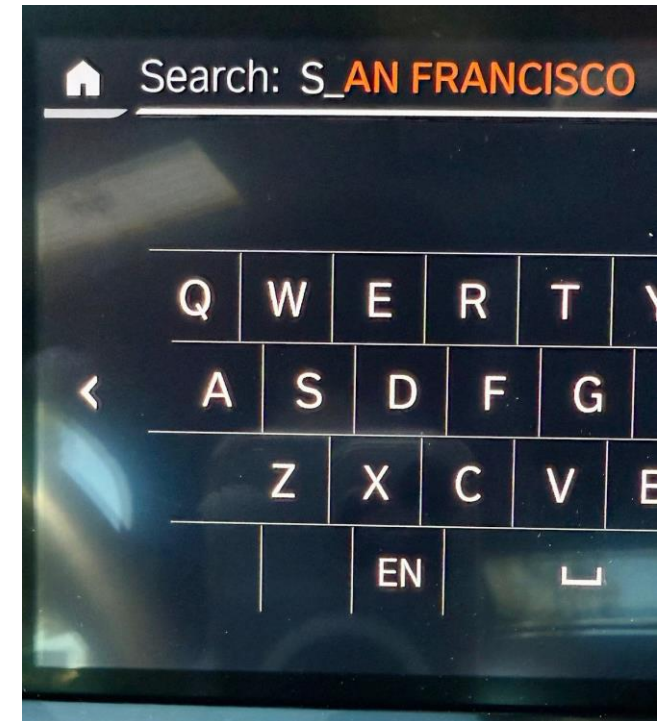
Handwriting In Today's Products



**Touch
Input**

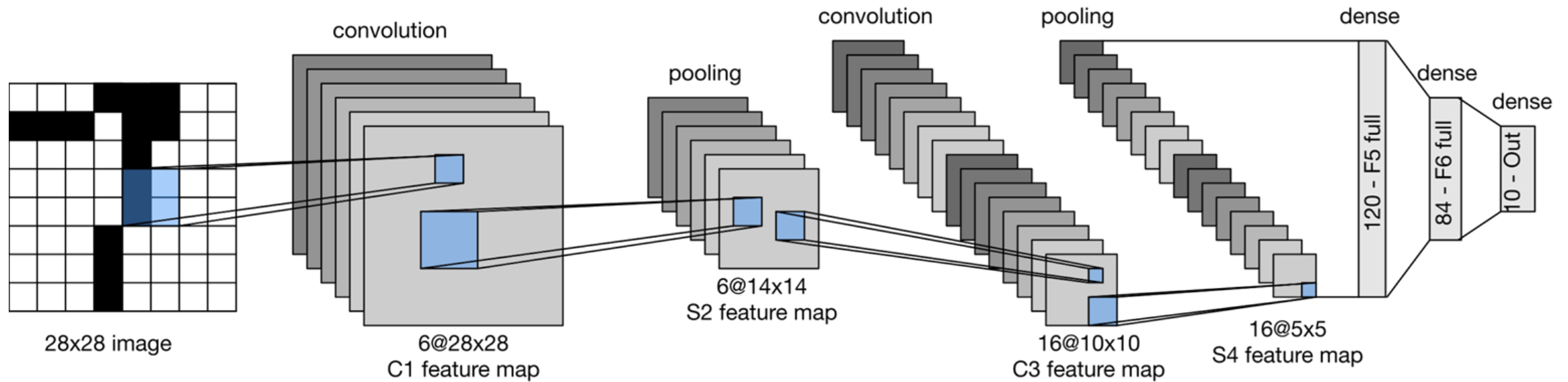


Display



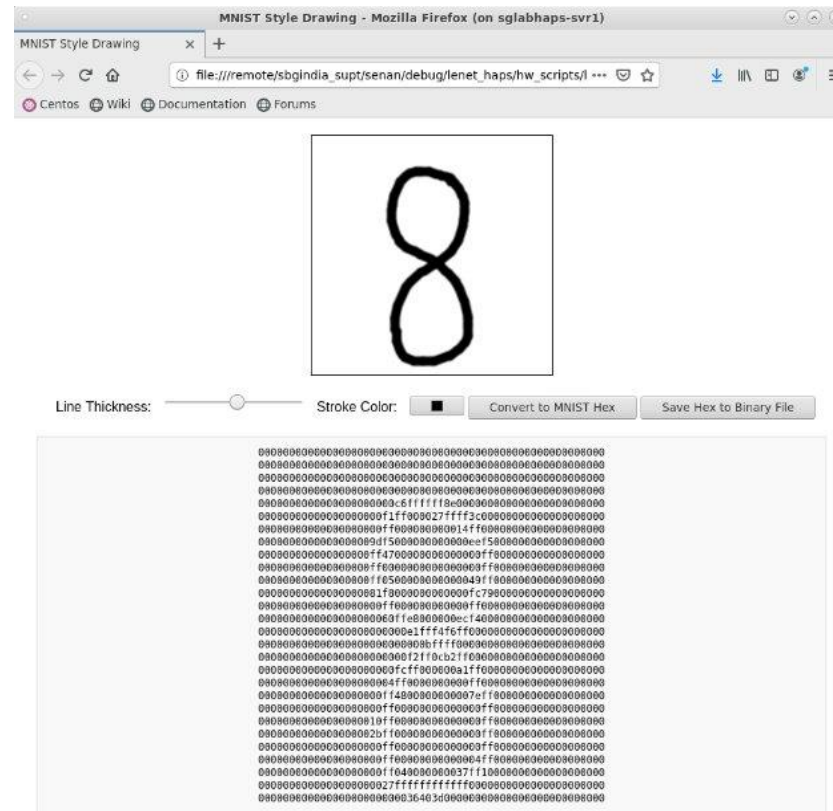
“S” recognized

LeNet Application



LeNet Application

- LeNet, handwritten numerical character recognition
- lenet.html (hex_data.bin)

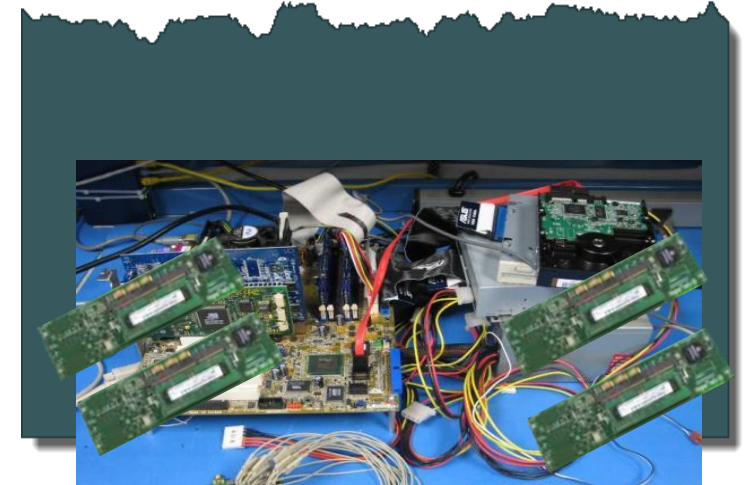
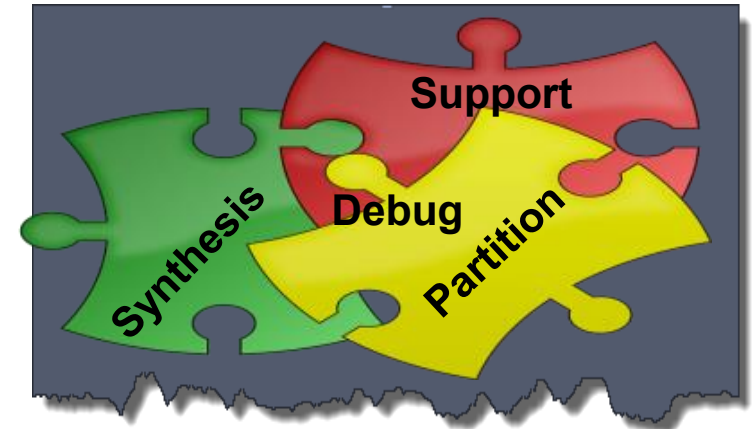


FPGA Prototyping Challenges

- How to fast bring up your design?
- How to easily resolve FPGA timing closure?
- How to test/confirm your FPGA environment ?
 - FPGA
 - Extension boards
- How to debug your design on FPGA ?
- How to partition your design ?
- How to analysis timing budgeting for multi-FPGAs ?

Lack of Integration/Examples Leads to Problems

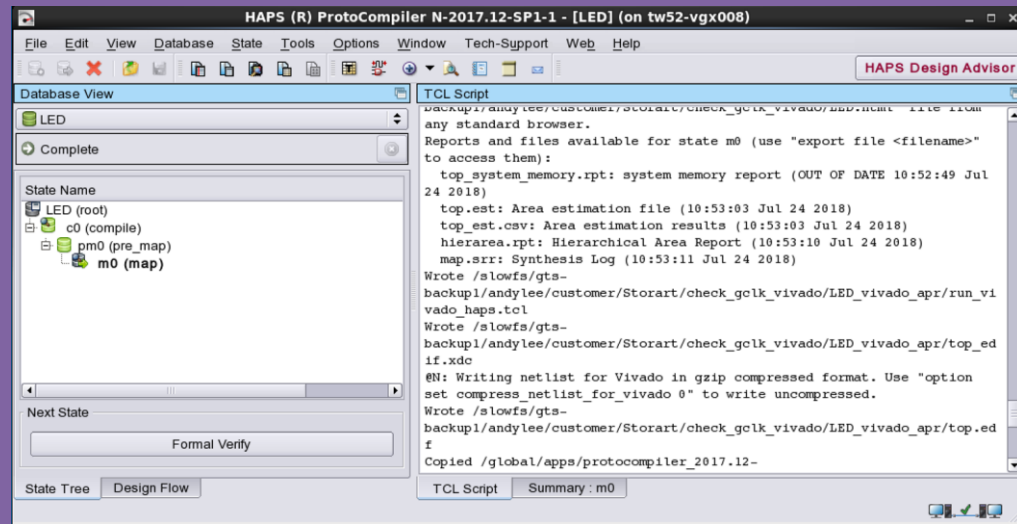
Tools



Hardware

How Synopsys Solves Challenges ?

HAPS Prototyping System



ProtoCompiler



HAPS-200

Synopsys HAV Product Family

Highest-performance and Most Versatile HAV Systems

ZeBu	ZeBu Server 5 	Highest Capacity-Scalable Emulation Platform (>60BG with Modular HAV Methodology)
	New: ZeBu-200 ZeBu EP1/EP2 	Highest Performance Emulation Platform (up to 15.4 BG)
HAPS	New: HAPS-200 HAPS-100 4F/12F 	Highest Performance Prototyping Platform (Up to 10.8 BG)
	HAPS-100 1F 	IP Prototyping Platform (<100 MG)

EP-Ready HW

EP SW Transition

New HAPS-200 Prototyping

Highest Scalability, Best Density

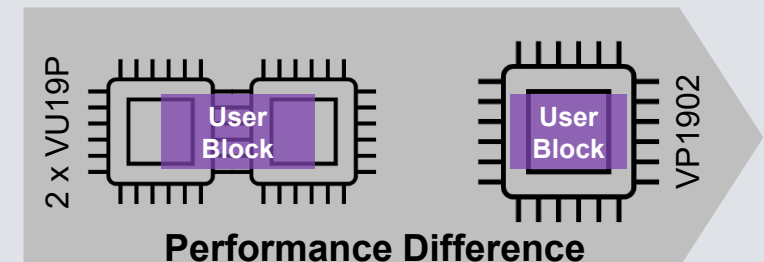
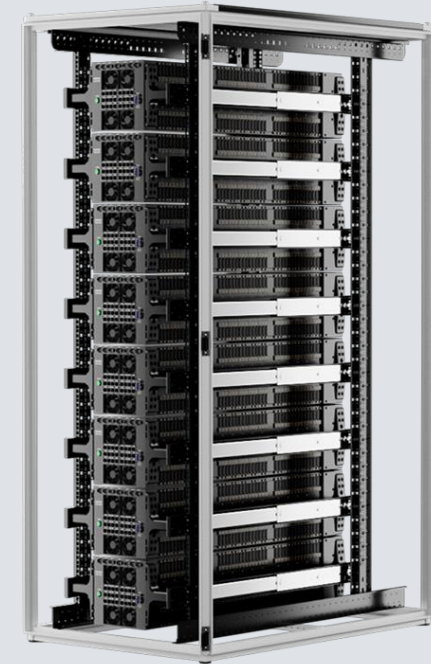


Highest Performance, **EP-Ready Hardware**

HAPS-200 Prototyping

NEW

- HAPS-200
- Latest AMD Versal™ Premium VP1902 adaptive SoC
- Industry-leading runtime performance up to 2X over prior generation HAPS-100
- Same compile time for larger FPGA
- Improved debug performance
- Leverages HAPS ecosystem
Support of HAPS-200/HAPS-100 Connections
- Scalable from single FPGA to multi-rack setups
Scales up to 10.8 BG



HAPS-200 vs HAPS-100 Comparison

Description	HAPS-200 6F	HAPS-100 4F
Module/ Capacity	6x AMD Versal Premium VP1902, 336 MG	4x AMD Virtex UltraScale+ VU19P, 112 MG
Dimensions / Weight	219mm (W) x 990mm (L) x 218mm (H) / 40 kg	449mm (W) x 680mm (L) x 106mm (H) / 21.5 kg
Modules per Rack	8 modules in 19" 42U rack	8 modules in 19" 42U rack
IO Connector	Field-replaceable HT3 Connector left/right	HT3 Connector on the top
Transceivers	8x GT per user FPGA	6x GT per user FPGA
Host Interface	Bandwidth: 4x, 6 hosts for 6 FPGAs for multi-user	Bandwidth: 1x, 2 hosts for 4 FPGAs for multi-user
Debug	192 GB total trace buffer, 4x DTD, 10x GSV bandwidth	32 GB total trace buffer, 1x DTD, 1x GSV bandwidth
User Memory	DDR5/DDR4 Daughter Card	DDR5/DDR4 Daughter Card
Embedded Processor	Yes	N/A



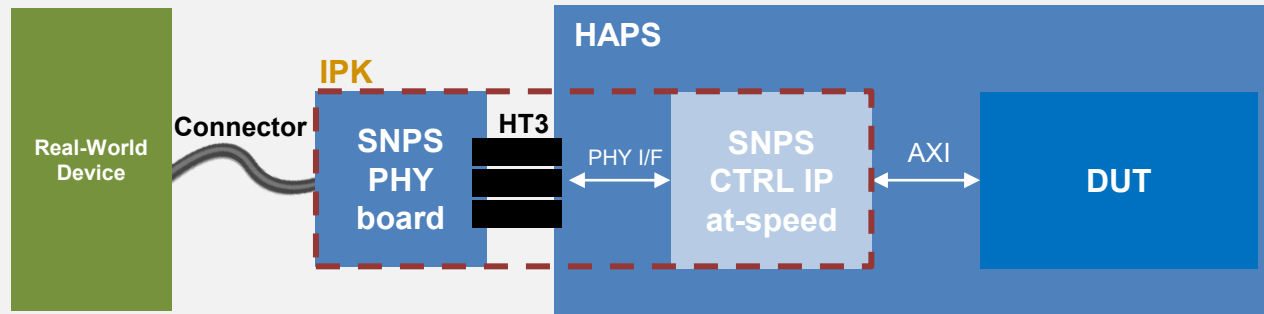


Protocol Solutions for HAPS

Protocol Connectivity and Compliance Testing is a Key Use Case for Prototyping

IP Prototyping Kit IPK

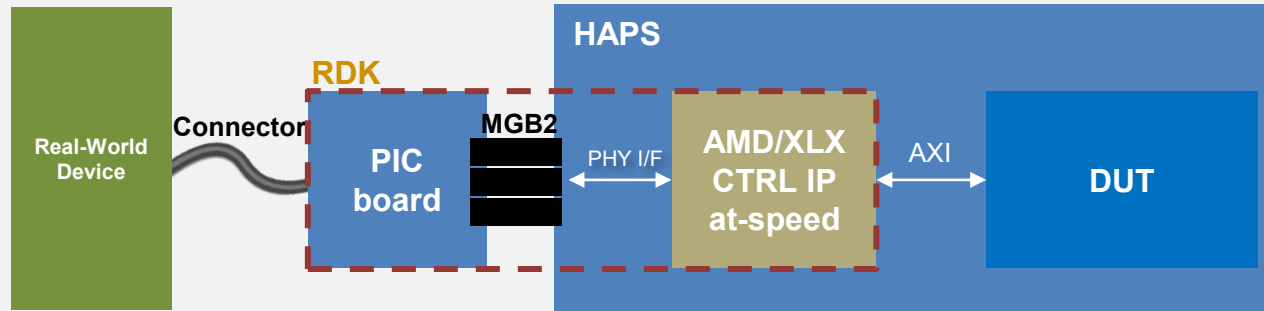
When DUT has SNPS Interface IP and closes timings at-speed



- SNPS CTRL IP Prototyping Reference design
- SNPS PCIe IP PHY Test Chip Board
- CTRL IP runs at-speed w/ reduced FPGA config

Reference Design Kit RDK

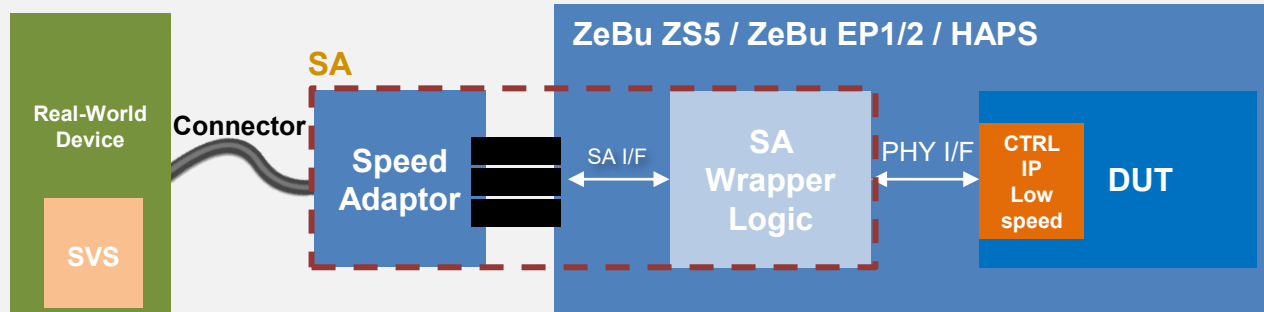
When DUT has 3rd party Interface IP and closes timings at-speed



- SNPS PIC Card with PCIe connector
- AMD/Xilinx CTRL+PHY IP
- CTRL IP runs at-speed w/ AMD/XLX config

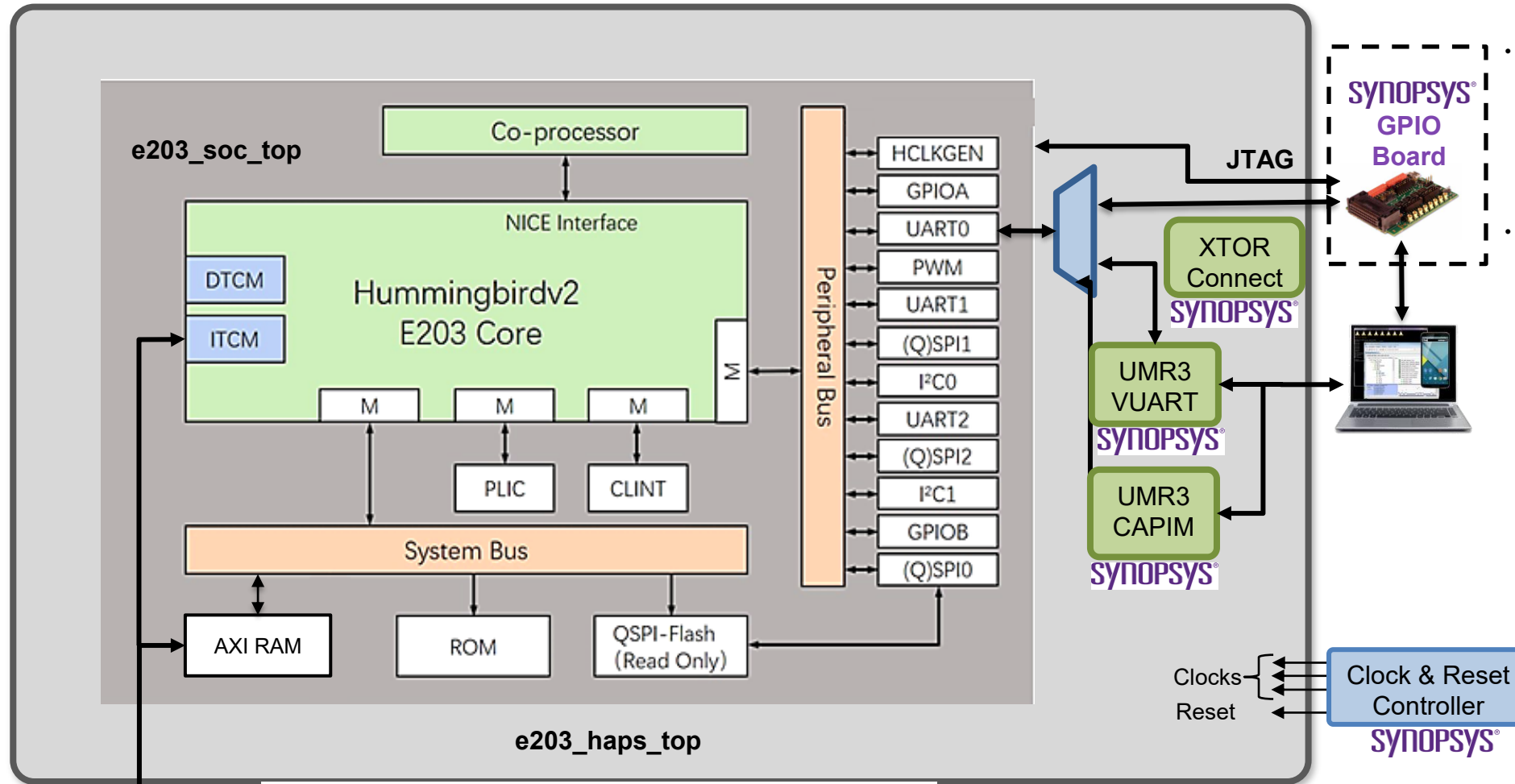
Speed Adaptor SA

When DUT Interface IP cannot close timings at-speed

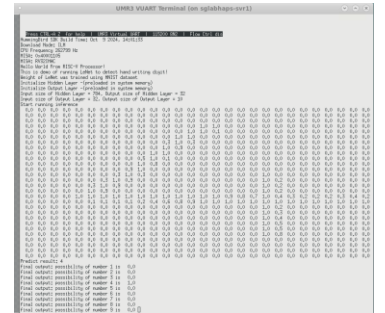


- DUT PHY IP replaced by a SA Wrapper Logic
- Real-world devices connect to the SA
- SA rate adapts DUT ↔ Real-world device
- DUT runs at ZeBu / HAPS speed
- DUT CTRL IP runs at slow-speed, but ASIC config can be used

LeNet Design on HAPS-200



- Addition of modules**
- Virtual UART alternative for Physical UART
 - CAPIM for UART Selection
 - Dynamic Force to load boot and application memory
- Addition of HAPS Daughter Boards**
- GPIO for UART to Host PC
 - CPU JTAG Debug



Dynamic Force
SYNOPSYS

- Dynamic Force**
- ← **serv_sim_ram**
 - ← boot_mem.haps (ITCM boot memory)
 - ← **axi_ram**
 - ← hidden_layer_weight_f_final_infer_only.txt
 - ← output_layer_weight_f_final_infer_only.txt
 - ← hex_data.hex (Application data, generated from lenet.html)
- } Inference weight data

Clock, Configuration and Reset

- Clocks used in HAPS-200
 - HF Clock – 50 MHz, LF Clock – 10 MHz, AXI RAM Clock – 150 MHz, JTAG Clock – 10 MHz
 - Configured through constraints/board.tss – FB1.uA Clocks
 - Loaded through runtime/system/targetsystem.tsd
 - Active low reset, reset_n is generated from USR_LOCAL_RESET of FB1.uA

UMR3 CAPIM & Virtual UART

- CAPIM for selecting between VUART and Physical UART
 - Bit 0 in CAPIM is set to 0 to select Virtual UART
 - Configured through hw_scripts/capim.tcl
- Virtual UART Configuration
 - UMR3 Clock Frequency – 125 MHz, Baud Rate – 115200, Parity – Disabled, Stop bits – 2

HAPS-200 Resource/Area and Timing Constraints

- Resource Utilization

Netlist Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Registers	134334	24	0	16920576	0.79
Register as Flip Flop	134326	24	0	16920576	0.79
Register as Latch	8	0	0	16920576	<0.01
CLB LUTs	138274	0	0	8460288	1.63
LUT as Logic	127166	0	0	8460288	1.50
LUT as Memory	11108	0	0	4230144	0.26
LUT as Distributed RAM	9416	0	0		
LUT as Shift Register	1692	0	0		
Variable Length SRL	1296	0	0		
Fixed Length SRL	396	0	0		
LOOKAHEAD8	1410	0	0	1057536	0.13

Block RAM

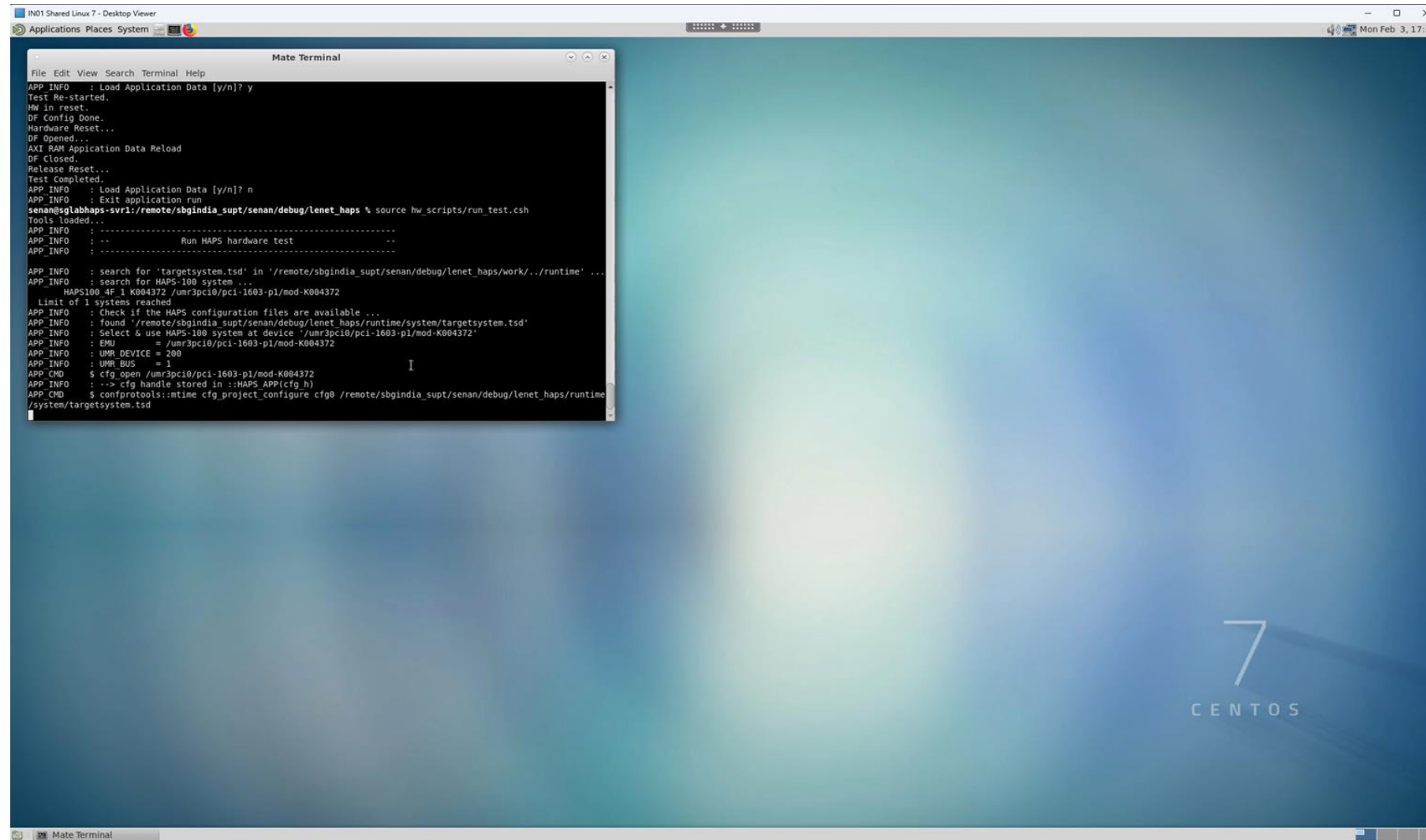
Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	60.5	0	0	6808	0.89
RAMB36E5	58	0	0	6808	0.85
RAMB18E5*	5	0	0	13616	0.04
Block RAM Imux registers	0	0	0		
Pipelining	0	0	0		
URAM	20	0	0	2200	0.91
URAM Imux registers	0	0	0		
Pipelining	0	0	0		

WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints
 1.049 0.000 0 174736

WPWS(ns) TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints
 0.504 0.000 0 64952

– Constraint to HF Clock – 50 MHz, LF Clock – 10 MHz, AXI RAM Clock – 150 MHz, JTAG Clock – 10 MHz

Lenet HAPS-200 Demo



```
IN01 Shared Linux 7 - Desktop Viewer
Applications Places System
Mate Terminal
File Edit View Search Terminal Help
APP INFO : Load Application Data [y/n]? y
Test Re-started.
HW in reset.
DF Config Done.
Hardware Reset...
DF Opened...
AXI RAM Application Data Reload
DF Closed.
Release Reset...
Test Completed.
APP INFO : Load Application Data [y/n]? n
APP INFO : Exit application run
senan@sgLabhaps-svr1:/remote/sbgindia_supt/senan/debug/Lenet_haps % source hw_scripts/run_test.csh
Tools loaded...
APP INFO : -----
APP INFO : -- Run HAPS hardware test --
APP INFO : -----
APP INFO : search for 'targetsystem.tsd' in '/remote/sbgindia_supt/senan/debug/lenet_haps/work/./runtime' ...
APP INFO : search for HAPS-100 system ...
HAPS100_4F_1_K004372 /umr3pci0/pci-1603-p1/mod-K004372
Limit of 1 systems reached
APP INFO : Check if the HAPS configuration files are available ...
APP INFO : found '/remote/sbgindia_supt/senan/debug/lenet_haps/runtime/system/targetsystem.tsd'
APP INFO : Select & use HAPS-100 system at device '/umr3pci0/pci-1603-p1/mod-K004372'
APP INFO : EMU = /umr3pci0/pci-1603-p1/mod-K004372
APP INFO : UMR_DEVICE = 200
APP INFO : UMR_BUS = 1
APP CMD $ cfg_open /umr3pci0/pci-1603-p1/mod-K004372
APP INFO : --> cfg handle stored in ::HAPS_APP(cfg_h)
APP CMD $ confprotocols:runtime cfg_project_configure cfg0 /remote/sbgindia_supt/senan/debug/lenet_haps/runtime/system/targetsystem.tsd
```

Summary

- HAPS-200 is a state-of-the-art, scalable, high-performance integrated Prototyping System
- Protocol Interface support is a key component for prototyping use cases
- LeNet Demo runs at 50 MHz system clock enabling fast verification of SW and HW

Thank You