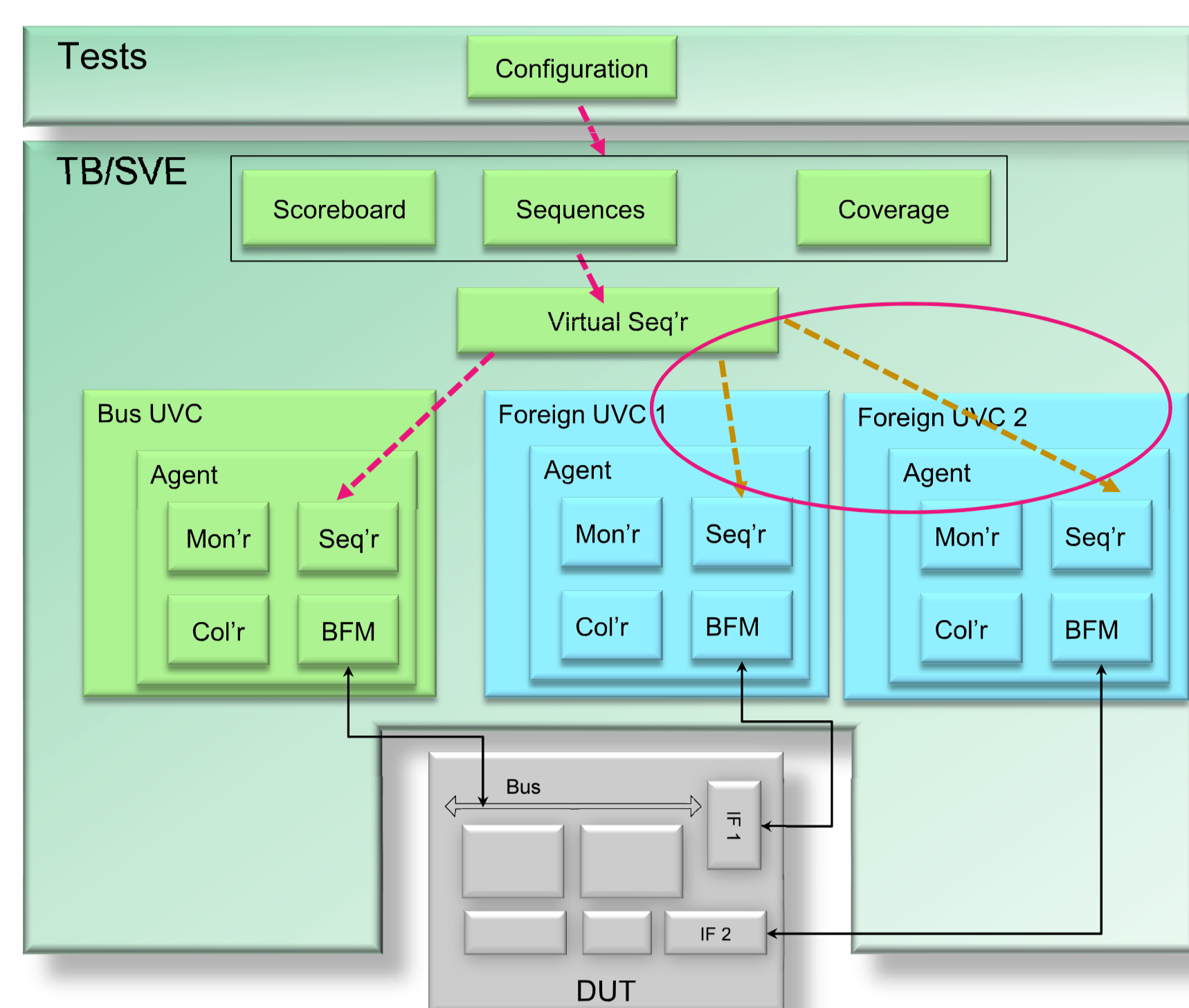


## Sequence Reuse in multi-language Verification Environments



How can it be done?

## UVM-ML Open Architecture Library

Cadence has provided a broad UVM-ML solution since 2009

- + Provided on OVM first, and then on UVM
- + Enables integration of 3 languages (SV, e, SC)
- Part of Cadence® Incisive® Functional Verification Platform

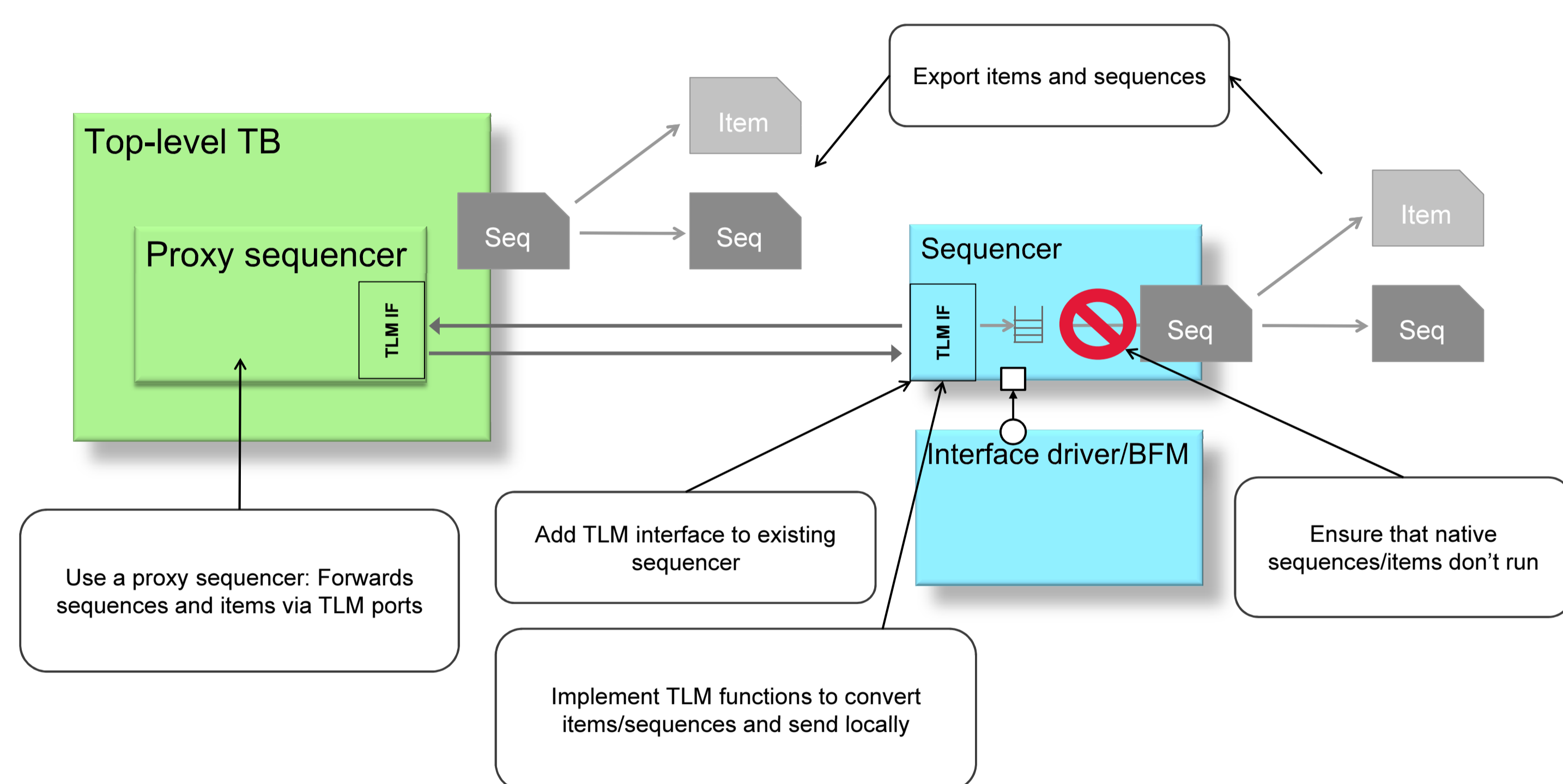
In 2013, Cadence (w/ AMD) expand multi-language offering significantly  
**UVM-ML Open Architecture (UVM-ML OA)**

- Open source, standardization ready (submitted to MLV-WG for consideration)
- Simulator independent
- Available on Accellera download
- Main features
  - Modular and extensible architecture
  - TLM communication (TLM1 and TLM2)
  - Unified hierarchy solution
  - Multi-language configuration
  - Multi-language sequence layering
  - Coordinated initialization
  - Pre-/post-/runtime phase synchronization

## Sequence reuse – Choose Use Model that fits best

Use Model	Controllability	Integration Effort
<b>Side by Side</b> - instantiate VIPs in parallel and configure locally	<ul style="list-style-type: none"> <li>No interaction with top level sequencer</li> <li>Users need to carefully import files to make sure correct sequences are selected</li> </ul>	<ul style="list-style-type: none"> <li>Least effort</li> </ul>
<b>Unified Configuration</b> - use the UVM-ML configuration mechanism to select the default/MAIN sequence	<ul style="list-style-type: none"> <li>Only the topmost sequence can be selected =&gt; might be sufficient in some cases</li> </ul>	<ul style="list-style-type: none"> <li>Medium Effort</li> <li>Users need to use UVM-ML OA library and use unified hierarchy</li> </ul>
<b>Unified Control</b> - use UVM-ML proxy sequencer and TLM solution	<ul style="list-style-type: none"> <li>Full control for sequences and items</li> <li>Ability to integrate in virtual sequencer</li> </ul>	<ul style="list-style-type: none"> <li>High Effort</li> <li>Requires type mapping for sequences and items</li> </ul>

## Unified Control – using proxy sequencers and TLM ports



## CONCLUSIONS

Sequence reuse can be achieved in multiple ways

- + Trade off between integration effort and top-level controllability of sequences and items

UVM-ML OA library has infrastructure and features to enable users to chose different sequence reuse use models

- Multi-language configuration can be used for low controllability solution
- Multi-language TLM communication and proxy sequencer types/templates can be used to achieve fine grained control of sequence and sequence items

## REFERENCES

- [1] UVM-ML Open Architecture (Overview and download)  
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