Reset Verification using formal tool

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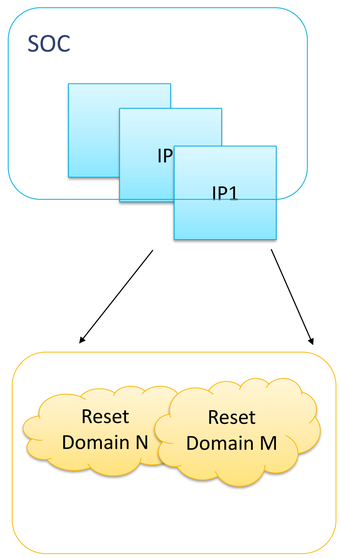
Problem Statement/Introduction

Reset verification is crucial as incorrect reset propagation leads to metastability

Modern day SOCs work on various reset and clock domains and presents extra-ordinary challenges for reset verification

Conventional approach to Reset verification is Gate Level Simulation (GLS) which itself introduces multiple challenges such as late bring up in verif-cycle, time-consuming execution etc.



Proposed Methodology

Our approach utilizes property verification capability of VC Formal tool, to ensure all the flops within the design hierarchy have been altered to their reset state, given that relevant reset is applied

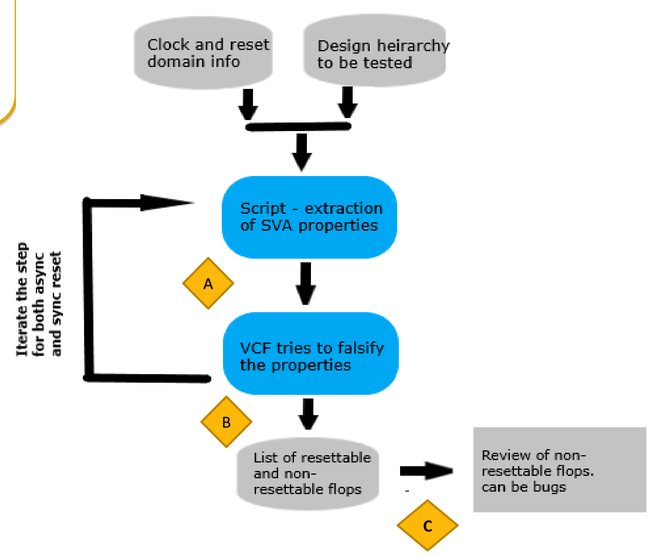
The methods works in 3 steps –
A : Script creates template based on the clock and reset domain info

B : Auto-extraction and property check for all the flops under design

C : Segregation of resettable and non-resettable flops

Non-resettable flops can be bugs!
The method is iterated twice for async. And sync. resets

Flow chart

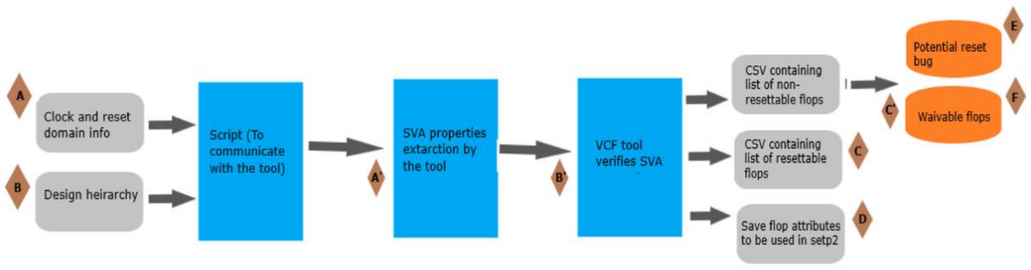


Implementation Details/Diagrams

Detailed flow or implementation is provided as follows:

Iteration – 1 or verification of async reset propagation:
Inputs – clock and reset info
Design hierarchy

Output – CSV files containing list of resettable and non-resettable flops
Flop reset attributes



A' : script provides the template for SVA property related to reset and clock and the design hierarchy to be tested

B': Auto-extarction of all flops under the intended heirarchy by tool and generation of list of SVA properties to be tested

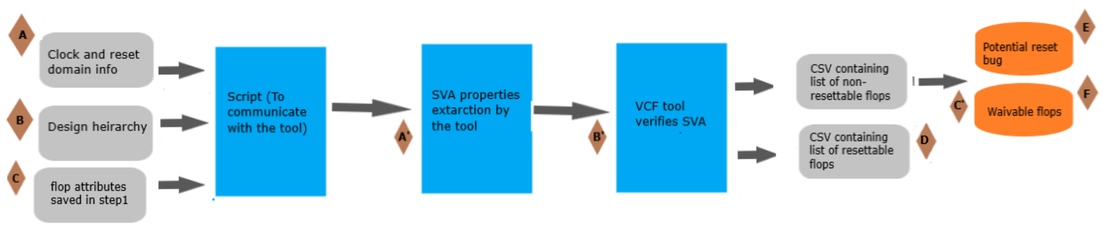
C': List of non-resettable flops needs to further review and can contain potential reset bugs

Implementation Details/Diagrams

Iteration – 2 or verification of sync reset propagation:

Inputs – clock and reset info
Design hierarchy
Reset attributes for flops

Output – CSV files containing list of resettable and non-resettable flops
Flop reset attributes



A': Script creates template for sync reset assertion

B': Auto-extarction of all flops under the intended heirarchy by tool and generation of list of SVA properties to be tested

C': List of non-resettable flops needs to further review and can contain potential reset bugs

Results/Conclusions

We produced a comparison with the conventional or legacy approach (GLS) with the new method on the following parameters:

- Time consumption (bring up and test case run)
- Early bug catch and portability (code reusability)

Results/Conclusions

The formal tool (VCF) methodology for reset verification incorporates multiple advantages. The procedure has been brought up in Video Core testbench environment for one of the key projects and contributed remarkably on the verification cycle, henceforth has been integrated in the flow for the subsequent projects.

The below table summarizes some of the key benefits the stated method:

Advantages	DV Impact
Minimal bring up time (2-3 h) whereas GLS may takes 1 week to bring up	Significant effort reduction for the DV engineer for closure of the activity
Script based mechanism coupled with standard tool	Easy portability between projects
Can be done early on verification cycle	Early bug catch
Auto generation of test vectors	Reduced DV coding effort