Pre-Silicon Validation of Production BIOS, Software Use Cases and Accelerator IP Workloads using Hybrid System Level Emulation SoC Platform

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Abstract

In this poster we present the methodology to perform validation of Software (SW) collaterals and SW use cases using custom Hybrid System Level Emulation (Hybrid SLE) Pre-Silicon SoC platform. SW collaterals include production BIOS, OS, Firmware (FW), Drivers and production Fuses. SW use cases include platform reset, power management and SW application for Core and Accelerator IP workloads. This validation at Pre-Si helps to achieve high quality for Intel products, target A0 PRQ (Production Release Qualification) and reduce Time to Market.

Keywords

BIOS, OS, SW Use Case, FW, Drivers, Accelerator IP Workloads, Hybrid SLE, Emulation, Validation, VP Simics

Introduction

During Pre-Silicon (Pre-Si) validation, pure SoC RTL simulation/emulation platform is highly used to validate synthetic and bare metal test content using synthetic BIOS. Synthetic BIOS is a bare minimum version of production BIOS which is used on Pre-Si platforms. Since these platforms don't easily support deployment of full stack software, majority of the validation doesn't involve production BIOS, OS, full stack drivers and real workloads for accelerator IP's like 5G, AI.

Enabling Pre-Si platform with the capability to validate critical SW collaterals and SW use cases will help to unearth potential bugs. These bugs, if found directly during Post-Silicon validation, requires enormous amount of debug effort, and may even harm the silicon quality. Exhaustive Pre-Si validation of workloads provides better performance validation and reduces the risk of performance bugs on the silicon. This approach saves debug time on silicon and occasionally avoids even re-spinning cost.

Hence, it becomes essential to exhaustively validate SW collaterals and SW use cases at Pre-Si stage itself to shift left the validation, improve validation coverage matrix, and target high quality A0 PRQ. To achieve this goal, we created custom Hybrid SLE platform, which combines cores from Virtual Platform (VP) Simics [1] testbench and rest of SoC (also known as Uncore) [2] from RTL Emulation. VP Simics is a system simulator, which will provide the required acceleration to execute BIOS, CentOS, and SW content. Whereas the RTL Uncore provides the apt platform for Pre-Si validation.

Problem Statement

To target alpha readiness of the SW content and improved validation of SW use cases, following objectives were identified for Pre-Si platform:

i. Create an accelerated Hybrid SLE platform, which provides the required acceleration
ii. Validation of production BIOS, CentOS, and production Fuses
iii. Validation of SoC Reset sequences at BIOS and OS level
iv. Validation of Power Management flow at OS level
v. Validation of SW stack and drivers
vi. Validation of critical Core and Accelerator IP workloads

Methodology

A. Hybrid SLE SoC Platform

As shown in Figure 1, the Hybrid SLE platform comprises of two components put together – RTL of the design mapped on emulator HW and VP Simics release of the design running in SW testbench. VP Simics release is the official system simulator of the design which is used to test the production binaries. It supports the Intel core instruction set and has all the components to simulate the SoC design. The Pre-Si Hybrid SLE platform used in our project has the core majorly active in VP Simics, and Uncore majorly active in RTL. They are connected at the IDI (Intra Die Interconnect) [2] interface using a hybrid bridge and IDI transactor (xtor). The hybrid bridge plays the vital role to route the transactions from VP Simics to RTL and vice- versa, via configurable mappings. The IDI Mux provides the flexibility to switch between RTL Core and VP Simics Core during different phases at runtime.

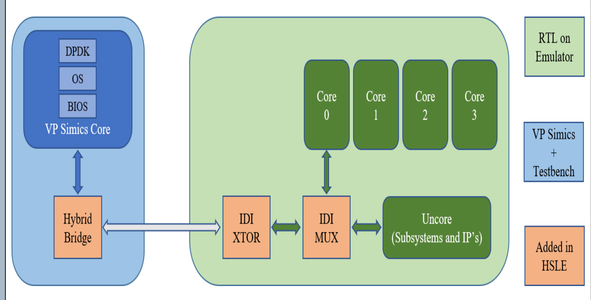

Figure 1

B. Hybrid SLE Boot Flow

In Hybrid SLE, the bootup sequence is slightly different from the regular case of pure RTL emulation, because both VP Simics and RTL need to boot in unison. As shown in Figure 2, the flow is divided into two phases..

i. Phase 1 is shown by sequence 1 and 2. During this phase, the VP Simics, hybrid bridge and IDI Mux are configured by the testbench. Meanwhile, the RTL core is active, and the SoC undergoes reset sequence which is similar to pure RTL emulation. The sequence continues till the reset vector fetch is initiated by the RTL core. When IDI mux receives the fetch request, it triggers Phase 2.

ii. Phase 2 is shown by sequence 3, 4 and 5. During this phase, IDI mux switches the control from RTL core to the VP Simics core for the execution of production BIOS binary. The production BIOS is loaded from the official release IFWI (Integrated Firmware Image) [3], which additionally contains all the FW required by the system. The configuration done by BIOS and FW is routed to the RTL uncore by the hybrid bridge. This means that production configurations are applied to the actual RTL IP's like Memory Controller, Power Management IP, IO Ports and PCIe devices. This closely mimics the actual configuration which will happen on the silicon chip after production. After execution of BIOS completes, user shall get control of the UEFI (Unified Extensible Firmware Interface) [4] shell which can be used to execute platform validation like reset flow.

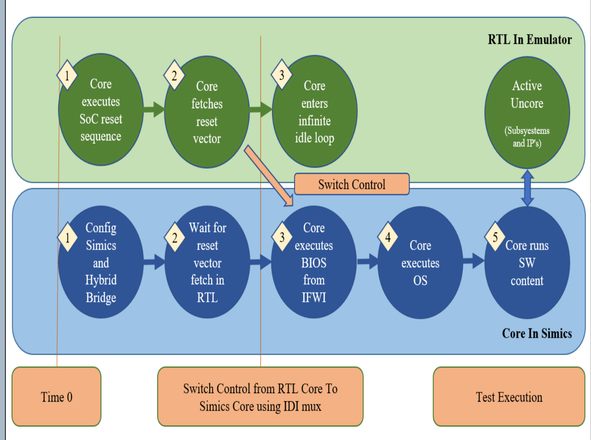

Figure 2

Methodology

C. CentOS Bring-up

After execution of BIOS completes, the VP Simics core boots up the CentOS image. In the process, it loads the Linux kernel, configures the memory resources, network and other peripherals connected to the SoC in RTL. After completion, it provides the Linux shell window where the user executes the SW content validation.

D. Platform Reset

As part of our validation goals, the platform reset validation was successfully done from both UEFI shell and Linux shell. On receiving reset request, the production BIOS triggers the system reset flow. It causes the Hybrid SLE Platform to undergo warm reboot or cold reboot, depending on the choice of reset.

E. SW Content Validation

SW content validation is a major focus area among all our validation goals. Using the Pre-Si Hybrid SLE platform, we successfully validated diverse SW use cases like enabling Virtualization, execution of Accelerator IP workloads, validation of FW, Drivers and PCIe devices. Validation of workloads in Pre-Si is crucial because it does stress testing of memory, interconnect, and the IP's. It exercises end-to-end flow of data and control paths at SoC level. The data path between IP and Memory, whereas as control path between Core and IP are validated, as explained in Figure 3

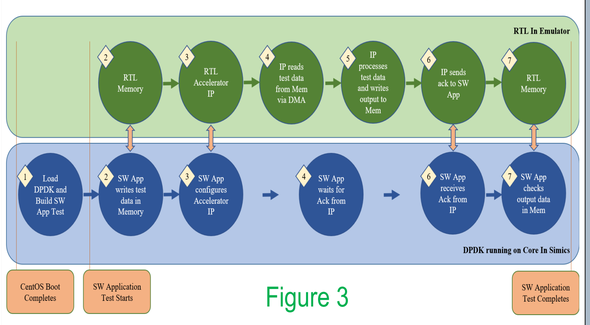

Figure 3

i. To validate Accelerator IP workloads on Pre-Si Hybrid SLE platform, we enabled the usage of SDK (Software Development Kit) after CentOS boots up. (This is shown in sequence 1). The DPDK provides the capability to create, compile and run SW application tests targeting the memory and accelerator IP in the RTL.
ii. The SW application configures memory pages and writes data in it (2).
iii. Then, it configures the accelerator IP for DMA (Direct Memory Access) transactions and required mode of operation (3).
iv. The IP initiates DMA read transactions from memory (4)
v. IP performs the required processing and writes output data back to the memory (5).
vi. After it is completed, it sends acknowledgment to the SW application (6)
vii. SW application compares the output data in memory with expected data (7)
viii. If the data matches, the workload execution successfully completes.

Results

As shown in Figure 4, close to 15 bugs were found across RTL, BIOS, VP Simics, and validation environment using Hybrid SLE platform. Debugging all these bugs during Post-Si would have been a very tedious task. The SW and BIOS bugs, 9 in total, would be very difficult to reproduce on pure emulation/simulation platforms due to lack of acceleration and limited feature in synthetic BIOS. But, with the help of Pre-Si Hybrid SLE platform, SW validation team was able to validate SW content, accelerator IP workloads and provide early feedback of SoC and SW quality before Tape-Out. Thus, ensuring that SW validation closely follows the RTL validation milestones and target A0 PRQ goals.

Results

i. **Acceleration -** Production BIOS execution time reduced to 45 mins, 100x gain than pure emulation (TABLE – I)
ii. **Left shift -** OS bring-up left shifted from Post-Si to Pre-Si validation
iii. **Test Coverage -** Reduced Bios run time enabled SW team to extensively validate drivers, end-to-end use cases
iv. **BIOS Coverage -** Executing production BIOS provides significantly better code coverage than synthetic BIOS
v. **Crucial use cases -** SW driven reset flow to catch global clock, reset and power management issues .

TABLE – I

Production BIOS & OS Boot Time in different Pre-Si Platforms

Pre-Si Platform	Hybrid SLE	Pure Emulation	Pure simulation
Production BIOS Boot Time	~45 Mins	75 Hours +	Not Feasible
OS Boot Time	~60 Mins	Not Feasible	Not Feasible

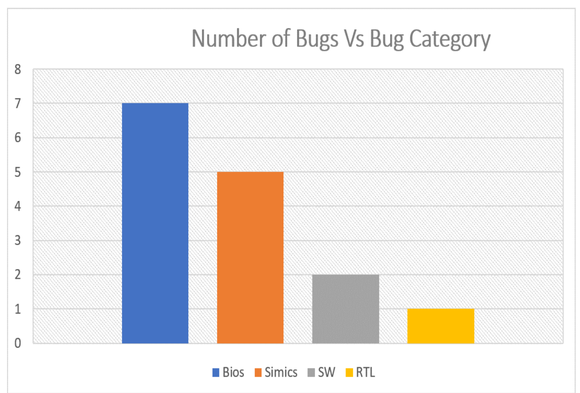

Figure 4

Future Scope

In the current program, certain validation goals have been marked for future scope. Pre-Si Hybrid platform would be ideal to run SPEC (Standard Performance Evaluation Corporation) [5] benchmark workloads for core. In addition, validation of Power Management flows from SW application would be an impactful use case.

Conclusion

The proposed methodology provides faster execution of SW collaterals and SW use cases. It empowers the Pre-Si validation team to complete crucial SW validation before the Tape-Out. As a result, any bug fixes needed in RTL or SW are carefully accounted for before Tape-Out of the design.

Acknowledgment

1. BIOS Team - For Supporting during Production Bring-up on Hybrid SLE and resolving the issues
2. OS Team - For Helping to boot Cent-OS on Hybrid SLE platform
3. VP Simics Team - For providing infrastructure support to integrate the VP Simics Core

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