



Pragmatic Formal Verification Methodology for Clock Domain Crossing

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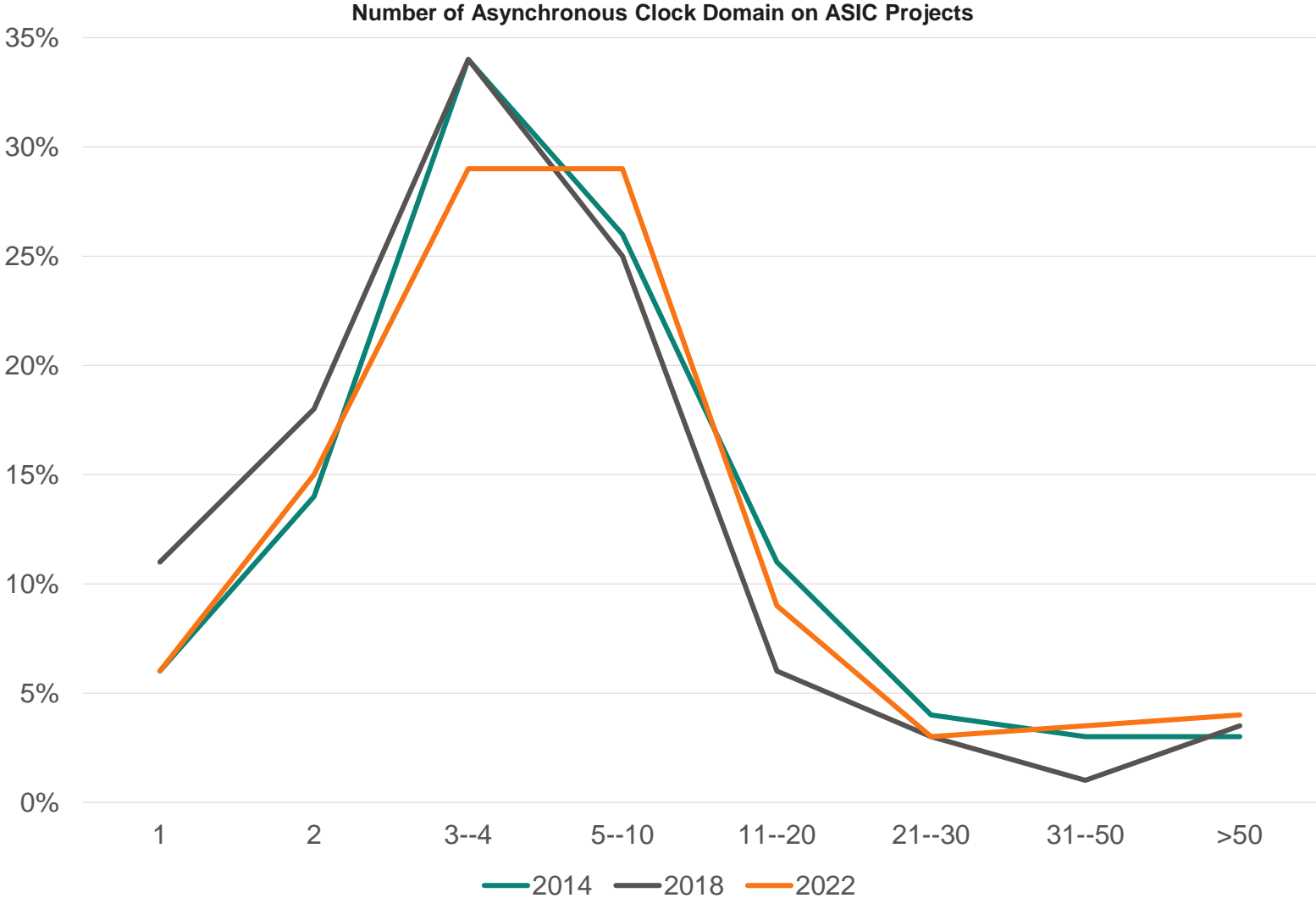
Agenda

1	Verification challenges	3
2	Technical background	6
3	Methodology development & implementation	10
4	Results and summary	18

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Clock domains are increasing with increasing complexity

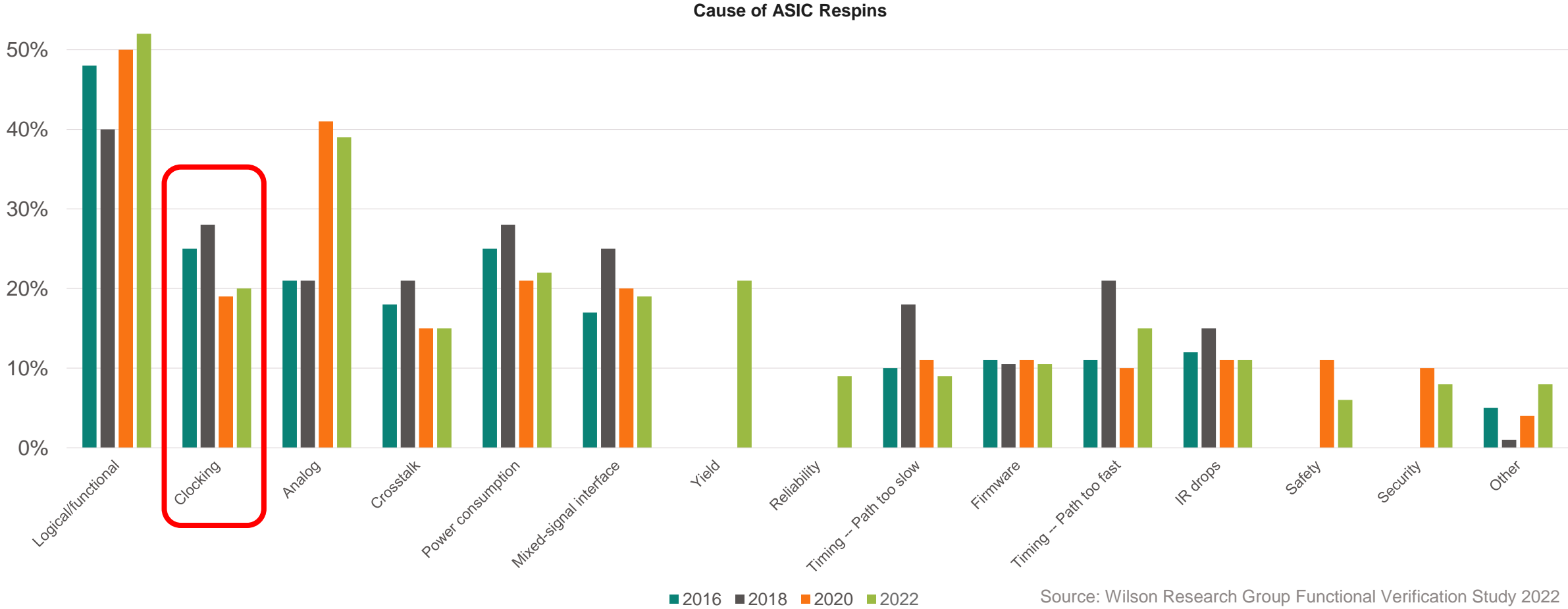


3 – 4

Average number of clock domains on ASIC designs

Source: Wilson Research Group Functional Verification Study 2022

CDC issues are a major reason for expensive respins



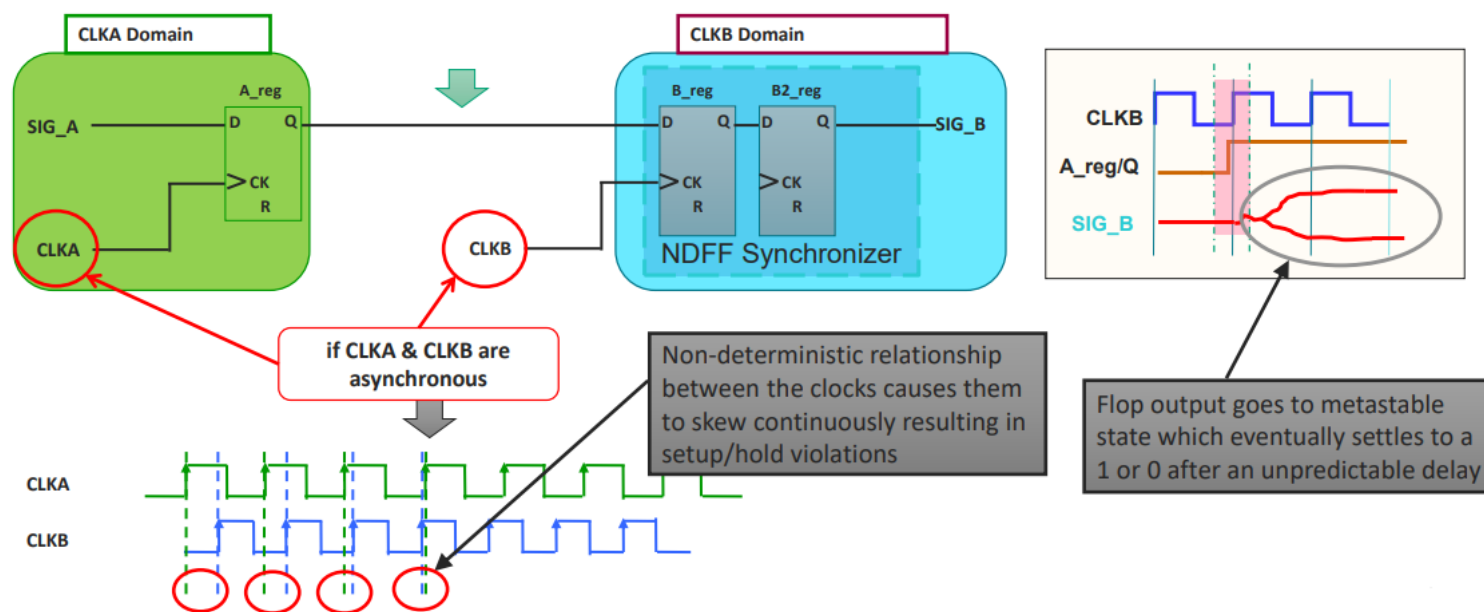
– CDC issues are 3rd major reason for Silicon respins

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Clock domain crossing and metastability

- A clock domain (CD) is a region of synchronous logic with exactly one clock
- Most real-life designs operate on multiple clocks (for power and performance reasons)
- A clock domain boundary arises when the clocks change

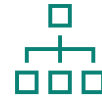


Source: Cadence JasperGold CDC user guide

- Signals crossing clock domains must be synchronized to avoid metastability effects!
- Metastability modeling → creating setup/hold violations

CDC issues

Structural violations



- Missing synchronizers
- Combinational logic on CDC path
- Structural glitch

CDC protocol violations

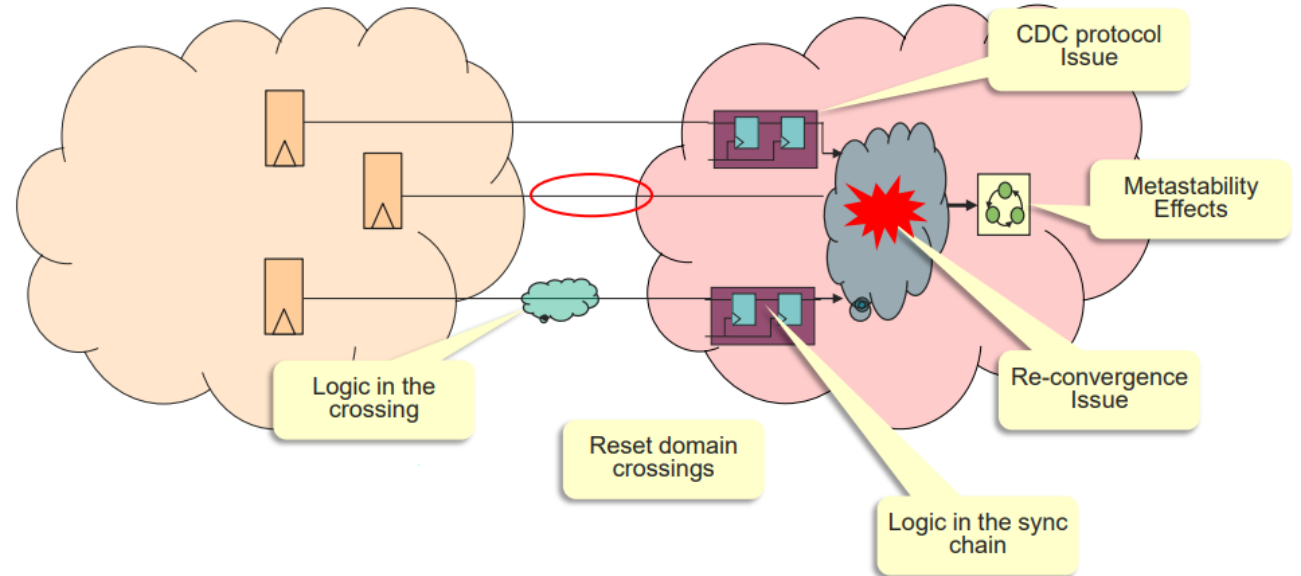


- Standard synchronization scheme-specific transfer protocol related issues
- Custom synchronization scheme-specific issues

Data coherency issues



- Convergent/divergent/re-convergent design structures

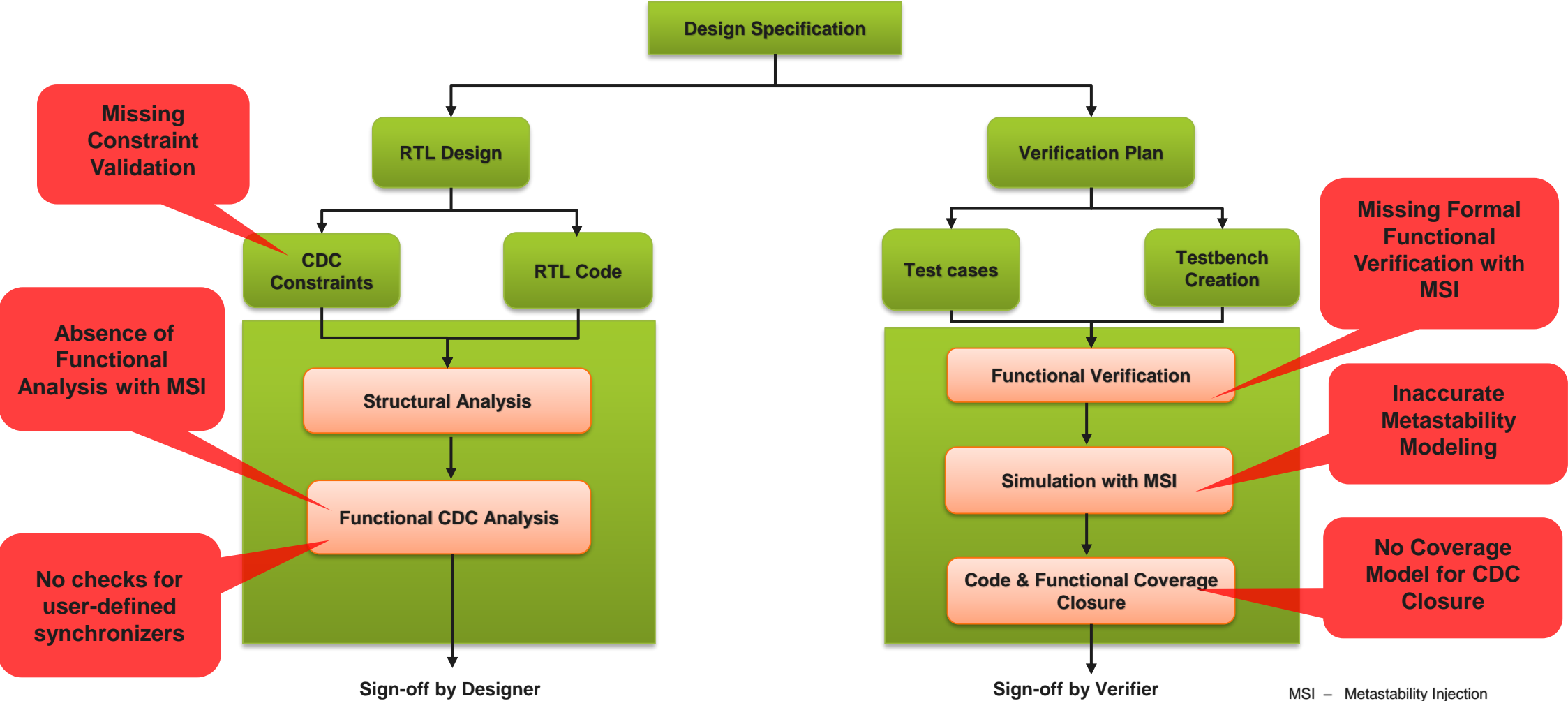


Reset domain crossing



- Reset related violations

Conventional CDC verification

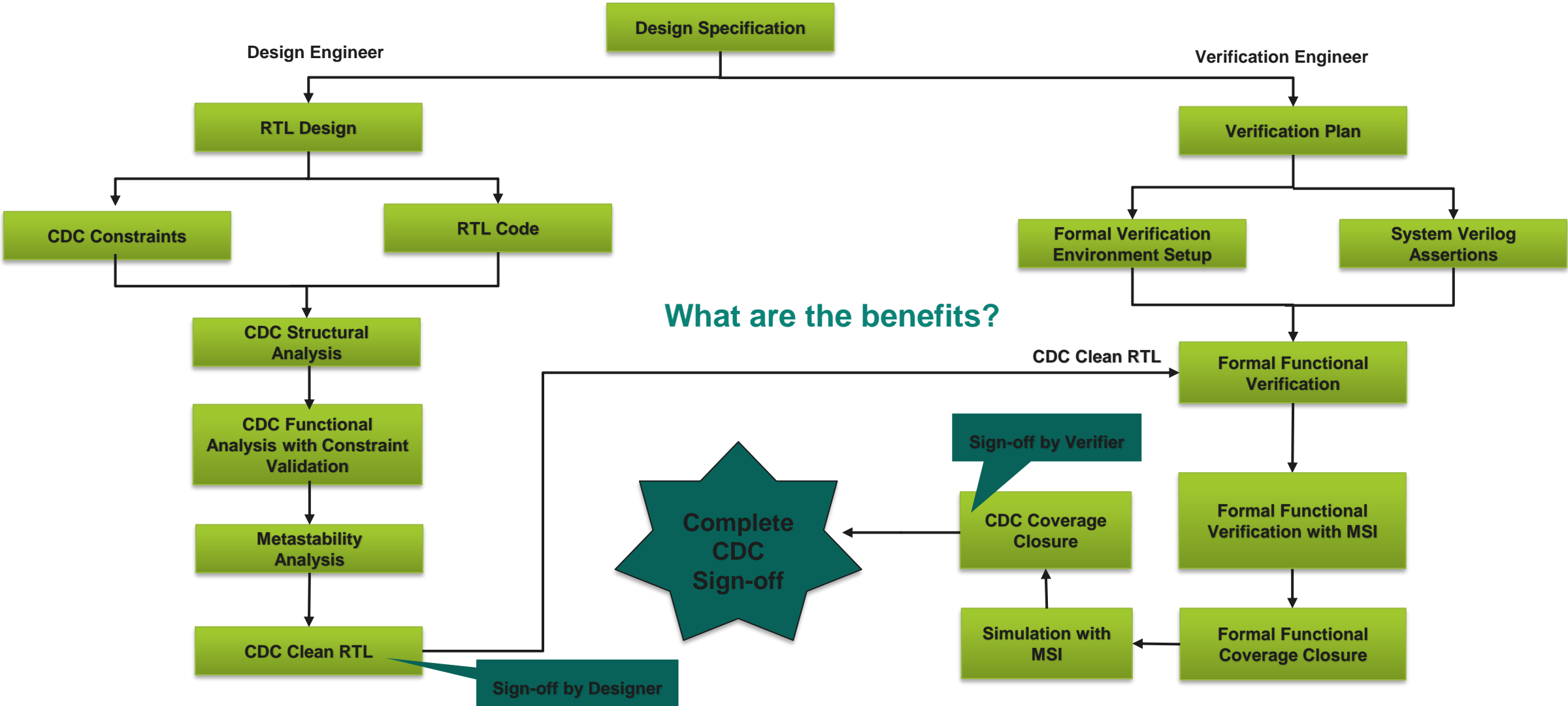


MSI – Metastability Injection
 CDC – Clock Domain Crossing

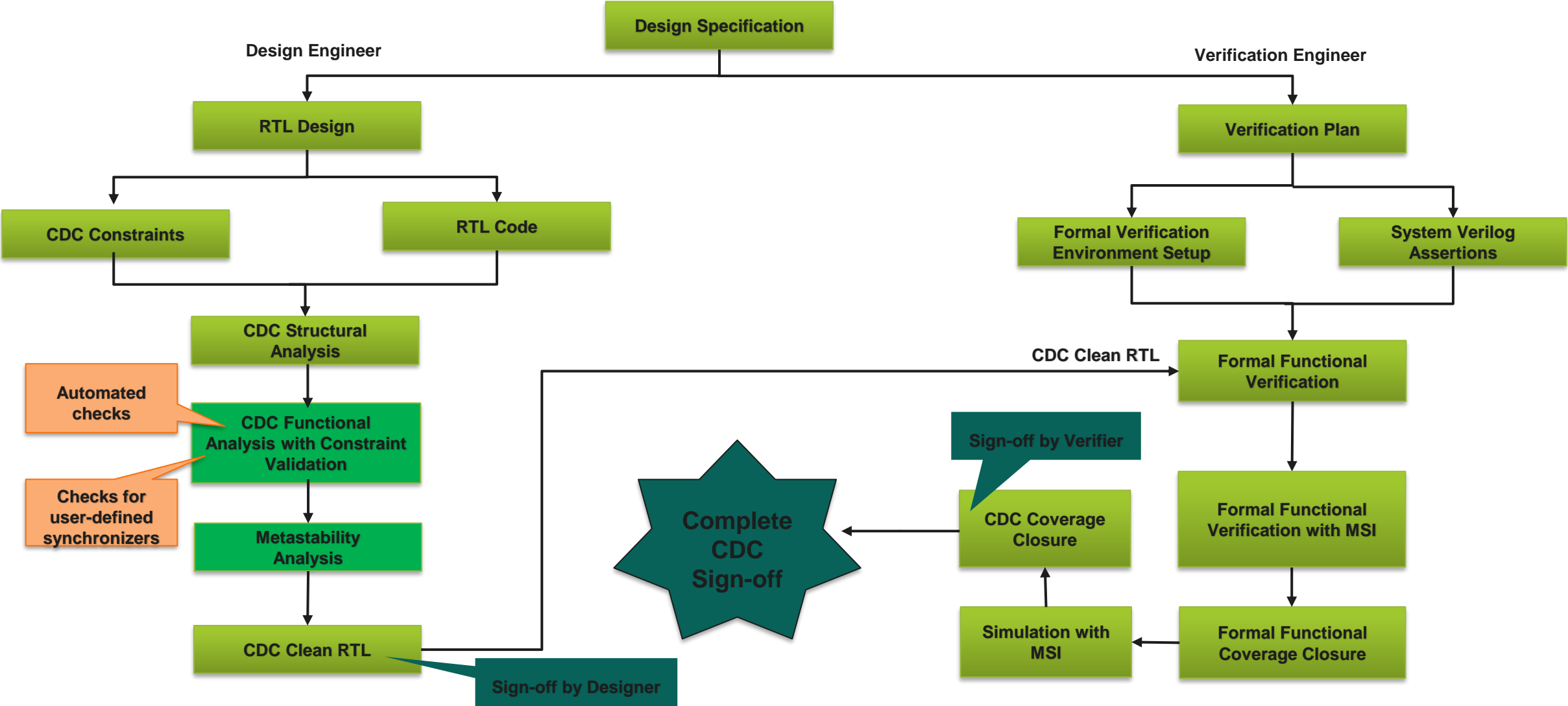
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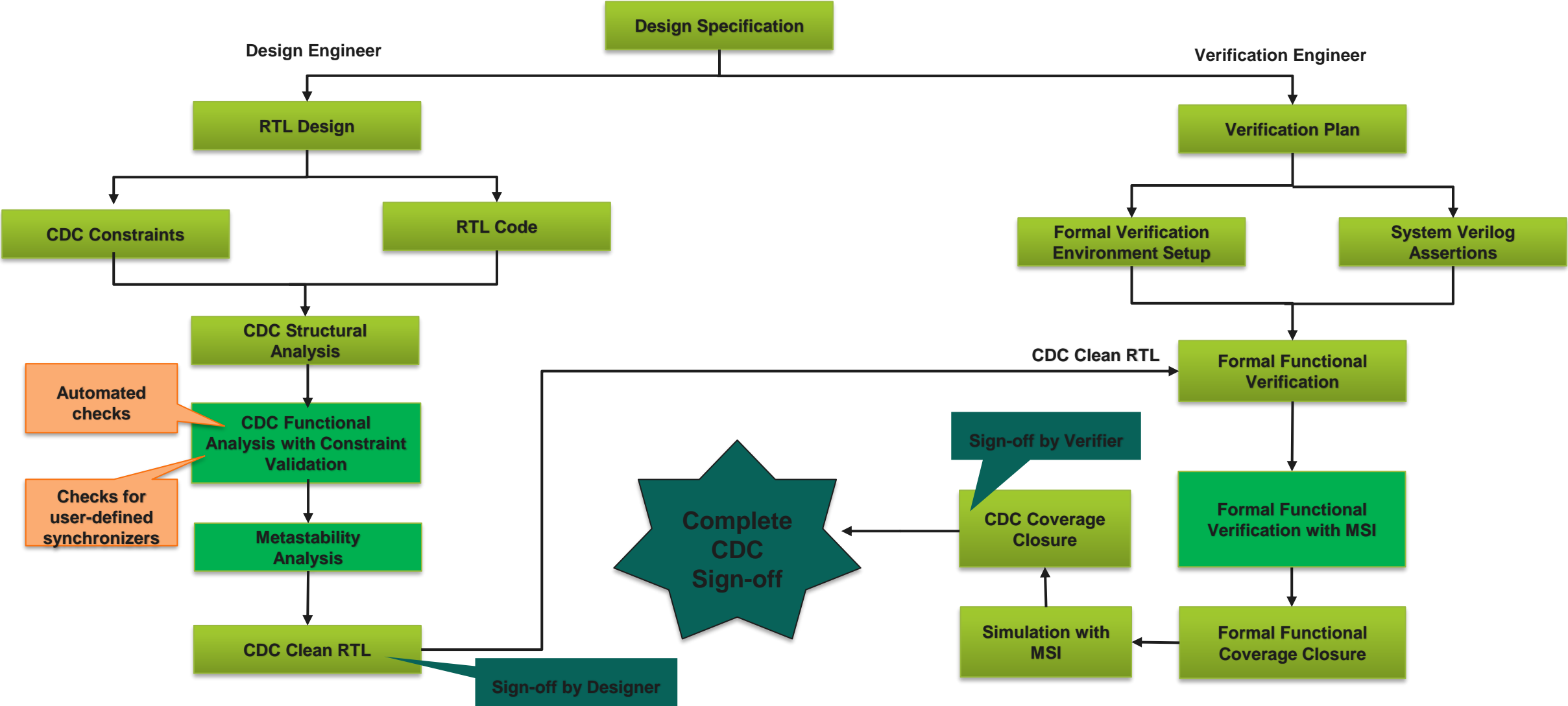
Proposed CDC verification flow



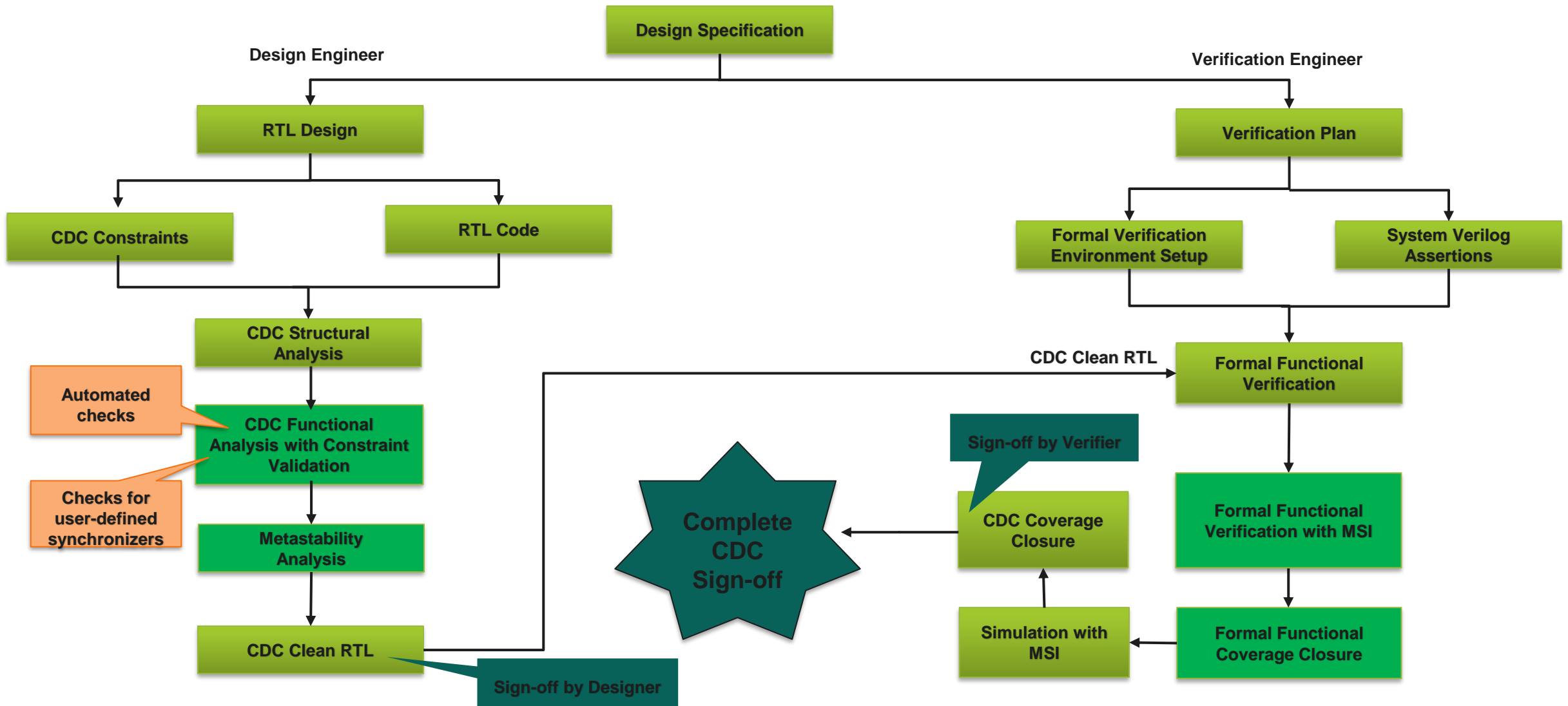
Proposed CDC verification flow



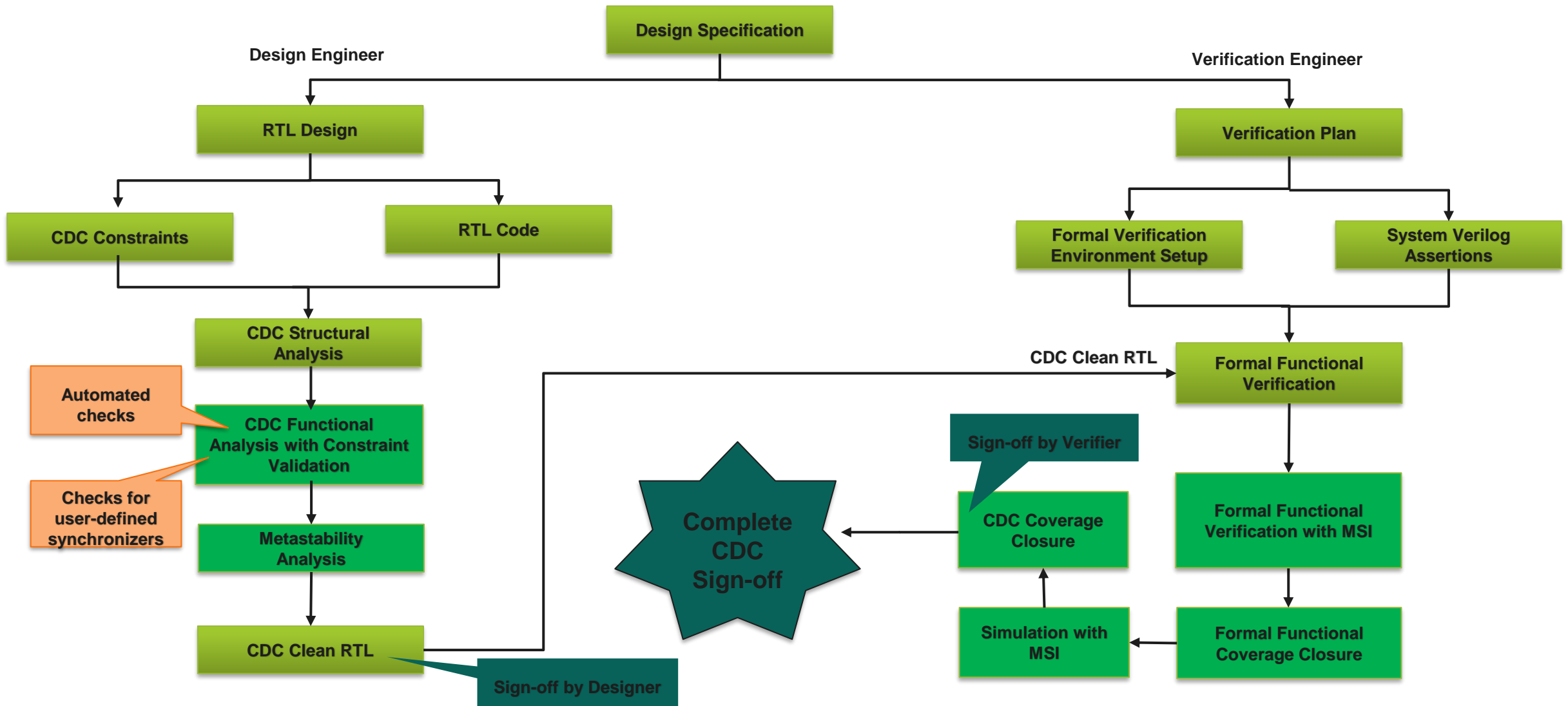
Proposed CDC verification flow



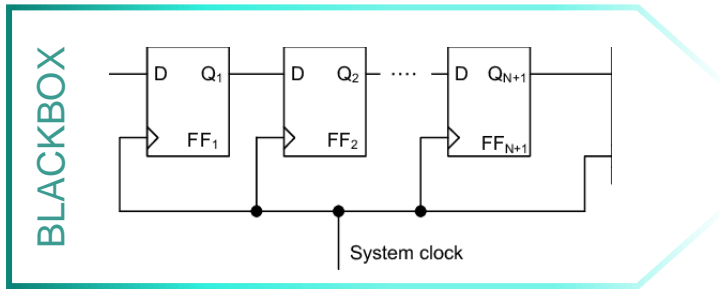
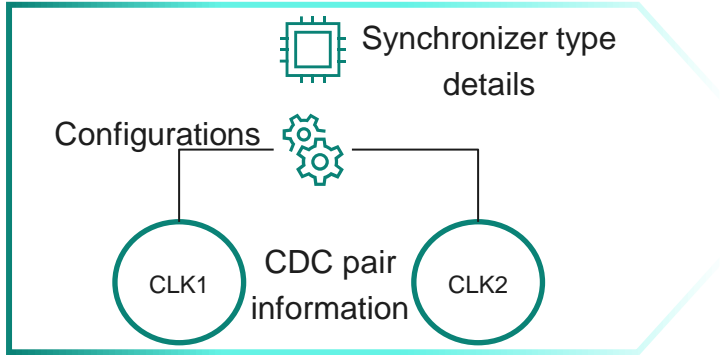
Proposed CDC verification flow



Proposed CDC verification flow



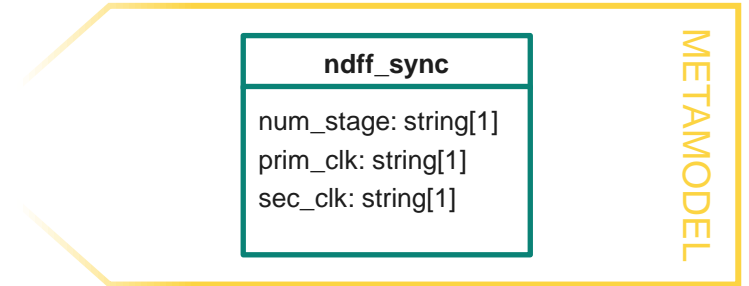
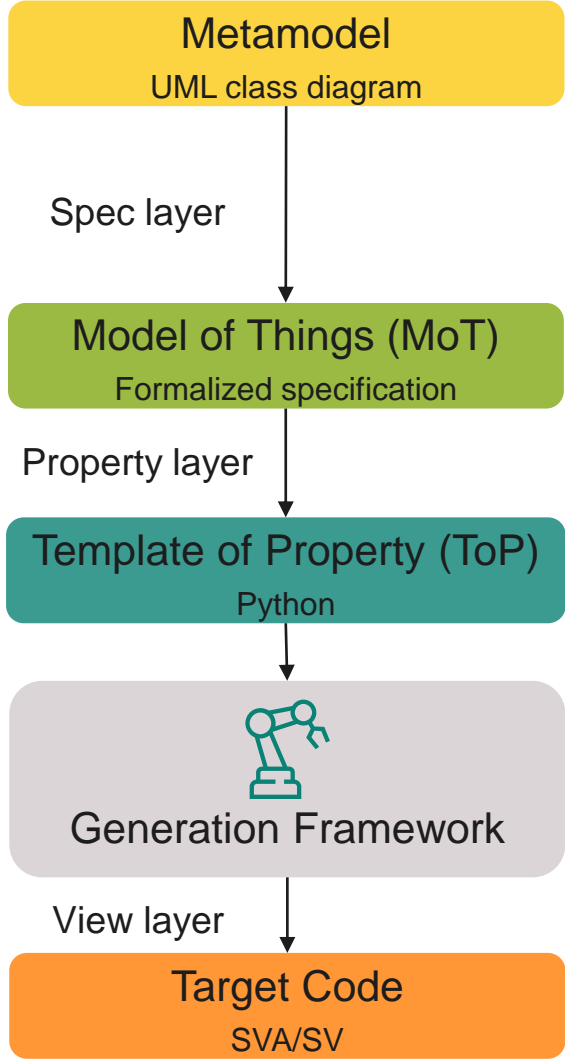
Metamodeling



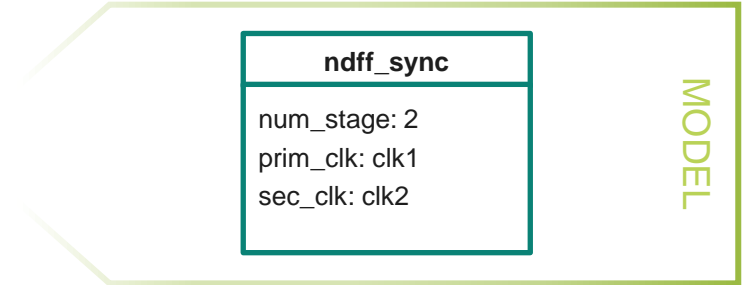
PROPERTIES

```

property data_stable;
  @(posedge clk1) disable iff (!rst_n)
    $stable(data_i) [*2];
endproperty
  
```



METAMODEL



MODEL

COVERAGE

```

covergroup cg @(posedge clk)
  cp_src: coverpoint sig_src
  cp_dest: coverpoint sig_dest
  cp_cdc_pair: cross cp_src, cp_dest
  
```

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Bugs detected

Type	Analysis Used	Bug Description
RTL bug	Structural analysis	Missing synchronizer for CDC signal
RTL bug	Structural analysis	Missing synchronizer for RDC signal
RTL bug	Structural analysis	Combinational logic on the CDC path
RTL bug	Structural analysis	Combinational logic on the RDC path
RTL bug	Structural analysis	Reset signal converged before reaching the destination unit
RTL bug	Functional analysis	Wrong signal configuration (signal not static)
RTL bug	Functional analysis	Signal not stable enough to be captured correctly by destination unit
Testbench bug	Functional analysis	Input pulse was more than 1 cycle wide (pulse synchronizer)
Testbench bug	Functional analysis	Data loss because of incorrect clock frequencies
Testbench bug	Metastability analysis	Assertion didn't handle the extra delay due to metastability propagation
Tool bug	MSI model generation	MSI model was not getting generated for simulation

The screenshot shows the 'Review Violations' window with a list of errors and a table of coverage groups.

Review Violations List:

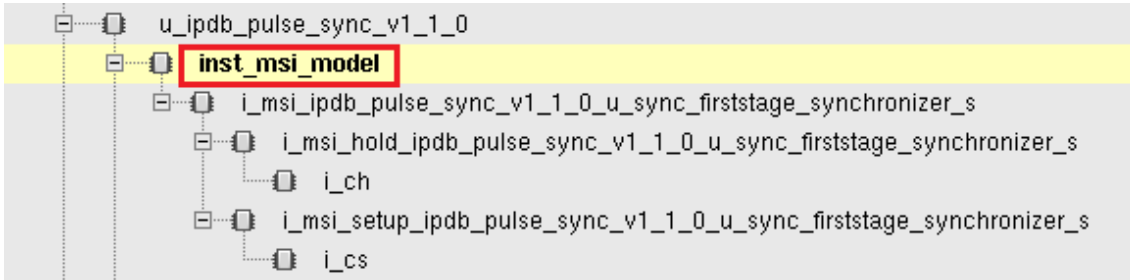
- Severity: Error (142)
- Tag: CDC_PR_LOGC (1)
 - "Combo Logic on CDC path between source unit 'i_smc_lite.i_apb_lite.control_block.control_state_r' driven by clo..."
- Tag: CNV_ST_CONV (2)
 - "Convergence at 'i_smc_lite.FSM_block.state' in destination clock domain 'hclk' after synchronization"
 - "Convergence at 'i_smc_lite.FSM_block.buffer_lsw_out' in destination clock domain 'hclk' after synchronization"
- Tag: RST_NO_SYNC (62)
 - "Missing reset synchronizer between reset signal 'n_sys_reset' driven by clock " and destination unit 'clocks_an..."
 - "Missing reset synchronizer between reset signal 'n_sys_reset' driven by clock " and destination unit 'i_smc_lite..."
 - "Missing reset synchronizer between reset signal 'n_sys_reset' driven by clock " and destination unit 'i_smc_lite..."
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Coverage Groups Table:

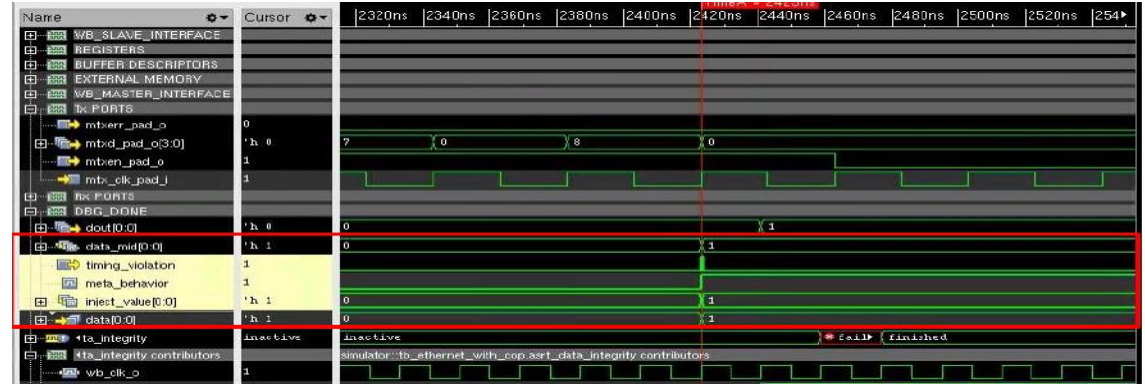
Name	Bin Name	Engine	Bound	Time	Task	Traces	CG Name	CP Name
inst_pulse_sync_sva	cp_src_3_auto11_cp_dest_3_auto11	Hp	3	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_3
cp_src_1	cp_src_3_auto11_cp_dest_3_auto0	Hp	2	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_3
cp_dest_1	cp_src_3_auto0_cp_dest_3_auto11	N	5	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_3
cp_src_2	cp_src_3_auto0_cp_dest_3_auto0	N	1	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_3
cp_dest_2	cp_src_2_auto11_cp_dest_2_auto11	Hp	3	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_2
cp_src_3	cp_src_2_auto11_cp_dest_2_auto0	Hp	2	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_2
cp_dest_3	cp_src_2_auto0_cp_dest_2_auto11	N	5	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_2
cx_cdc_pair_1	cp_src_2_auto0_cp_dest_2_auto0	N	1	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_2
cp_src_1	cp_src_1_auto11_cp_dest_1_auto11	Hp	3	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_1
cp_dest_1	cp_src_1_auto11_cp_dest_1_auto0	Hp	2	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_1
cp_src_2	cp_src_1_auto0_cp_dest_1_auto11	N	5	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_1
cp_dest_2	cp_src_1_auto0_cp_dest_1_auto0	N	1	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_1
cp_src_3	cp_src_1_auto0_cp_dest_1_auto0	N	1	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_1
cp_dest_3	cp_src_1_auto0_cp_dest_1_auto0	N	1	0.0	<embedded>		1 cdc_pair_cov	cx_cdc_pair_1
auto11	auto11	Hp	2	0.0	<embedded>		1 cdc_pair_cov	cp_src_1
auto1	auto1	Hp	3	0.0	<embedded>		1 cdc_pair_cov	cp_dest_1
auto1	auto1	Hp	2	0.0	<embedded>		1 cdc_pair_cov	cp_src_2
auto1	auto1	Hp	3	0.0	<embedded>		1 cdc_pair_cov	cp_dest_2
auto1	auto1	Hp	2	0.0	<embedded>		1 cdc_pair_cov	cp_src_3
auto1	auto1	Hp	3	0.0	<embedded>		1 cdc_pair_cov	cp_dest_3
auto0	auto0	N	1	0.0	<embedded>		1 cdc_pair_cov	cp_src_1
auto0	auto0	N	1	0.0	<embedded>		1 cdc pair cov	cp_dest_1

CDC verification on chip level

- MSI model integration to the simulation testbench



- Simulation waveform



- CDC coverage analysis

Ex	UNR	Name	Overall Average Grade	Overall Covered	Enclosing Entity
		(no filter)	(no filter)	(no filter)	(no filter)
		cg_hold_i_msi_ethmac_WillTransmit_q	100%	8 / 8 (100%)	msi_cov_ethmac
		cg_hold_i_msi_ethmac_sync_RxAbort_data_mid	0%	0 / 8 (0%)	msi_cov_ethmac
		cg_hold_i_msi_ethmac_ethreg1_SetTxClrq_sync1	0%	0 / 8 (0%)	msi_cov_ethmac
		cg_hold_i_msi_ethmac_wishbone_ReadTxDataFro...	0%	0 / 8 (0%)	msi_cov_ethmac
		cg_hold_i_msi_ethmac_wishbone_ReadTxDataFro...	0%	0 / 8 (0%)	msi_cov_ethmac
		cg_hold_i_msi_ethmac_wishbone_WriteRxDataTo...	0%	0 / 8 (0%)	msi_cov_ethmac

Ex	UNR	Name	Overall Average Grade	Overall Covered
		(no filter)	(no filter)	(no filter)
		d_hold	100%	2 / 2 (100%)
		inj_hold	100%	2 / 2 (100%)
		A*B d_cross_inj_hold	100%	4 / 4 (100%)

Ex	UNR	Name	d_hold	inj_hold	Overall Average Grade
		(no filter)	(no filter)	(no filter)	(no filter)
		d_0,di_0	d_0	di_0	100%
		d_0,di_1	d_0	di_1	100%
		d_1,di_0	d_1	di_0	100%
		d_1,di_1	d_1	di_1	100%

Summary

1



Early detection of CDC bugs

- Detection of bugs at the pre-silicon verification phase
- Less effort/time to fix the bug
- Saves money by avoiding costly re-spin

2



Features

- Uses both formal & simulation techniques
- High-quality design ensured with coverage analysis
- Automated assertion checks

3



Design & verification linkage

- Bridges the gap between structural and functional analysis
- Defines a CDC sign-off flow for both design and verification

4



Future work

- Detection of more synchronizer schemes
- Automated testbench generation for MSI in simulation
- Application in power-aware

Pragmatic CDC formal verification

