Pragmatic Formal Verification Methodology for Clock Domain Crossing

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Agenda

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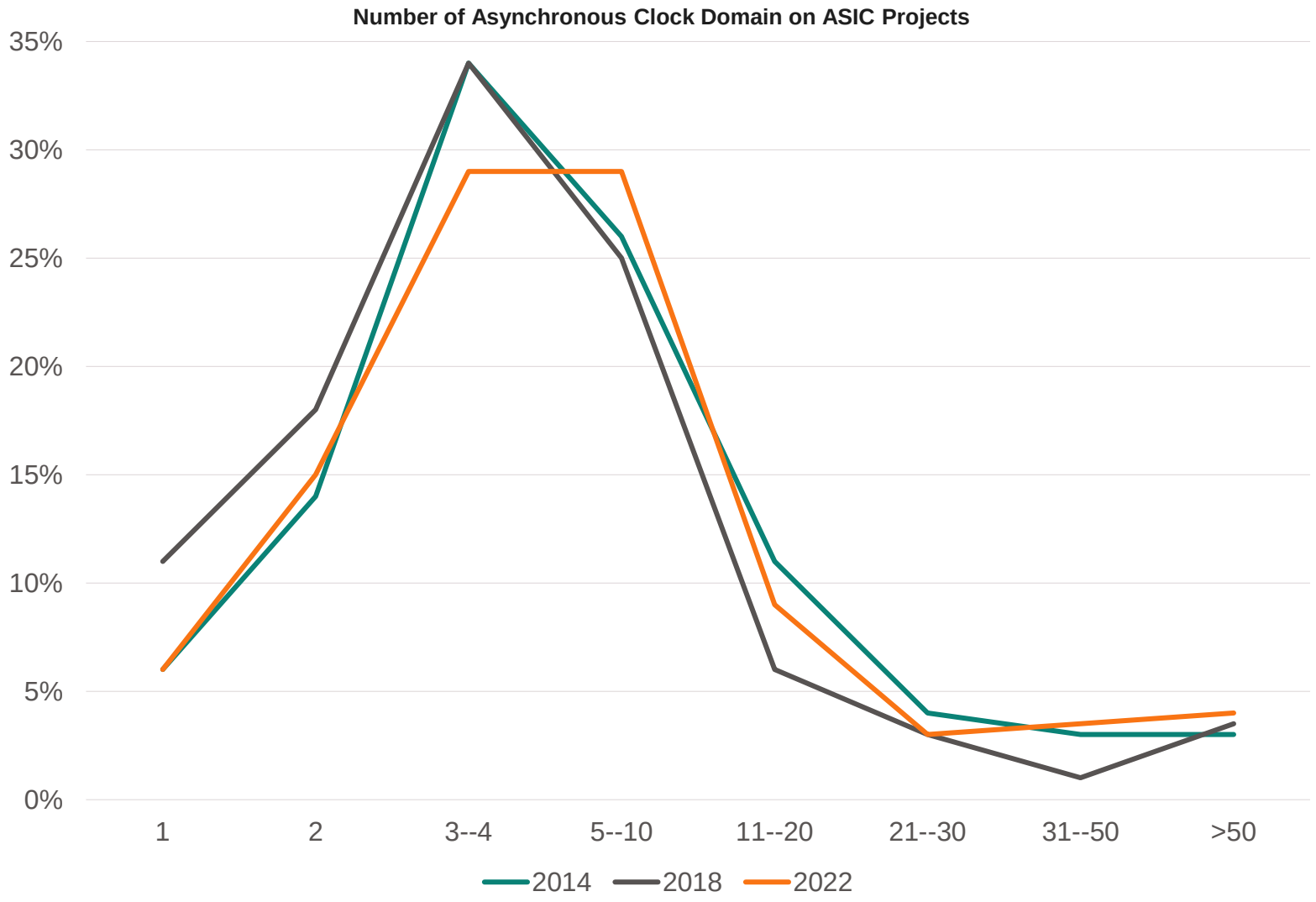
Clock domains are increasing with increasing complexity

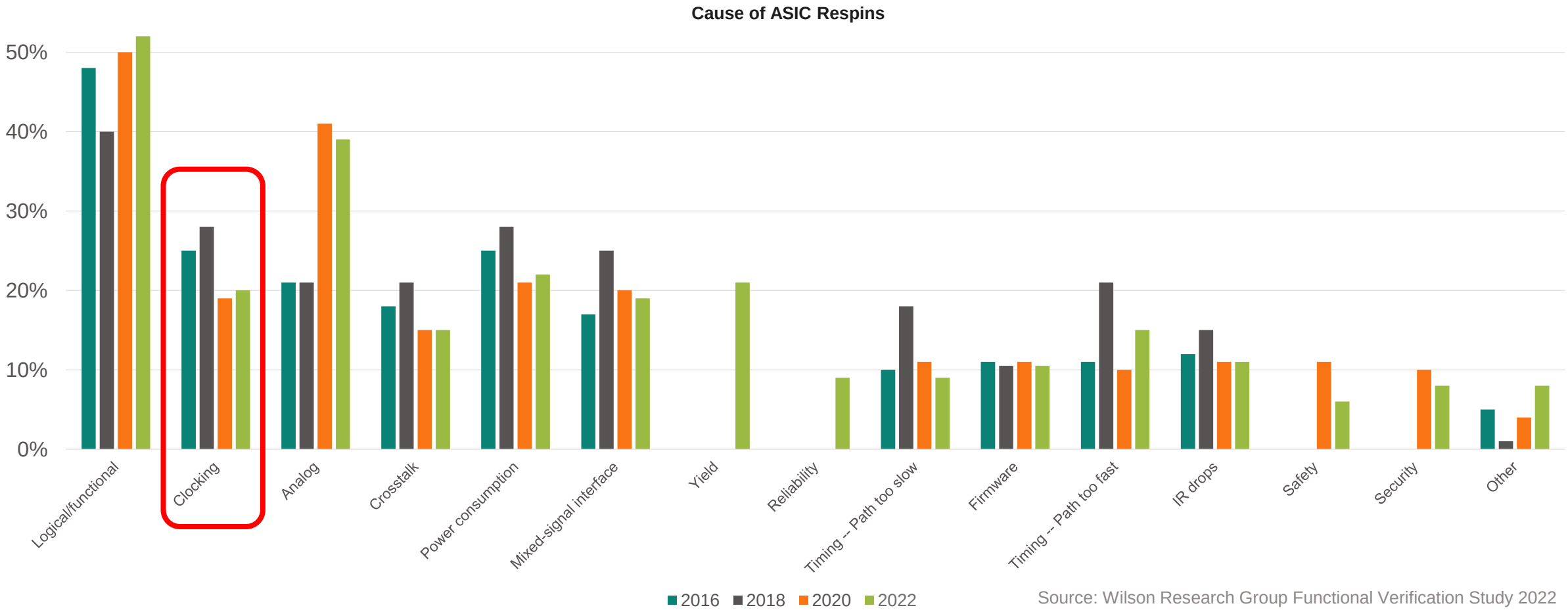


Source: Wilson Research Group Functional Verification Study 2022

3 – 4

Average number of clock domains on ASIC designs

CDC issues are a major reason for expensive respins



Source: Wilson Research Group Functional Verification Study 2022

– CDC issues are 3rd major reason for Silicon respins

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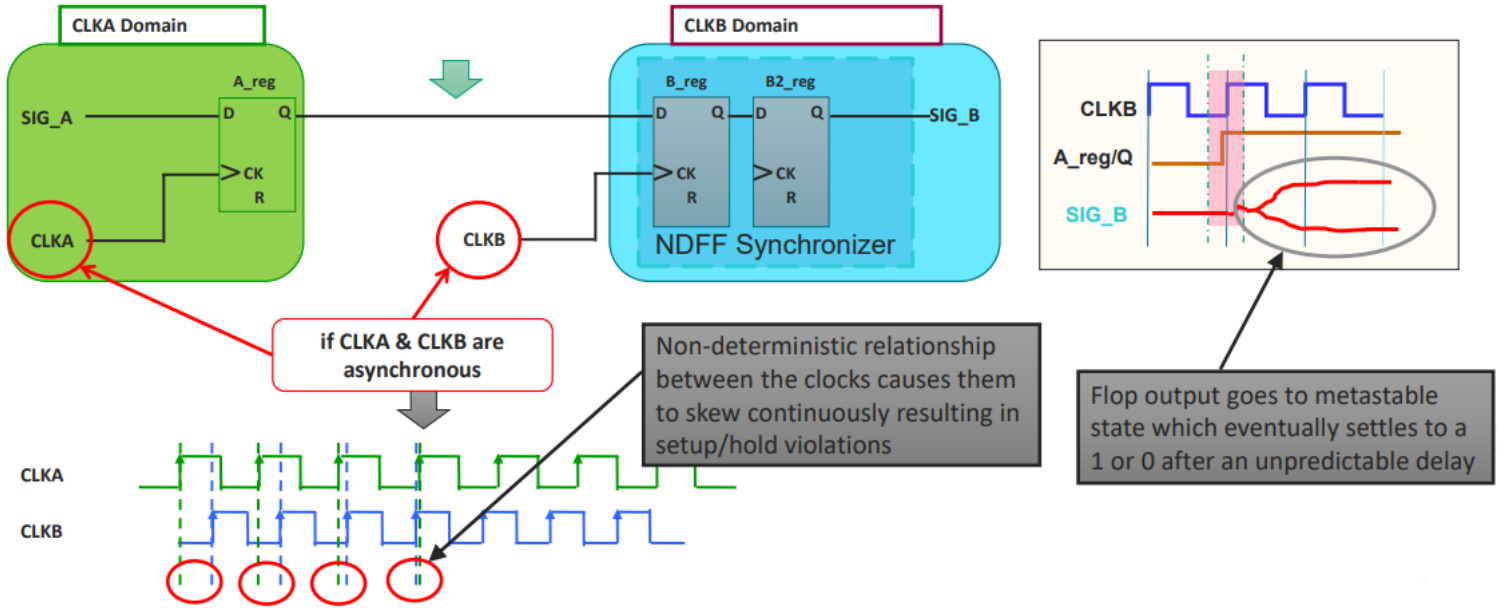
Clock domain crossing and metastability

- A clock domain (CD) is a region of synchronous logic with exactly one clock
- Most real-life designs operate on multiple clocks (for power and performance reasons)
- A clock domain boundary arises when the clocks change



Source: Cadence JasperGold CDC user guide

- Signals crossing clock domains must be synchronized to avoid metastability effects!
- Metastability modeling → creating setup/hold violations

CDC issues

Structural violations

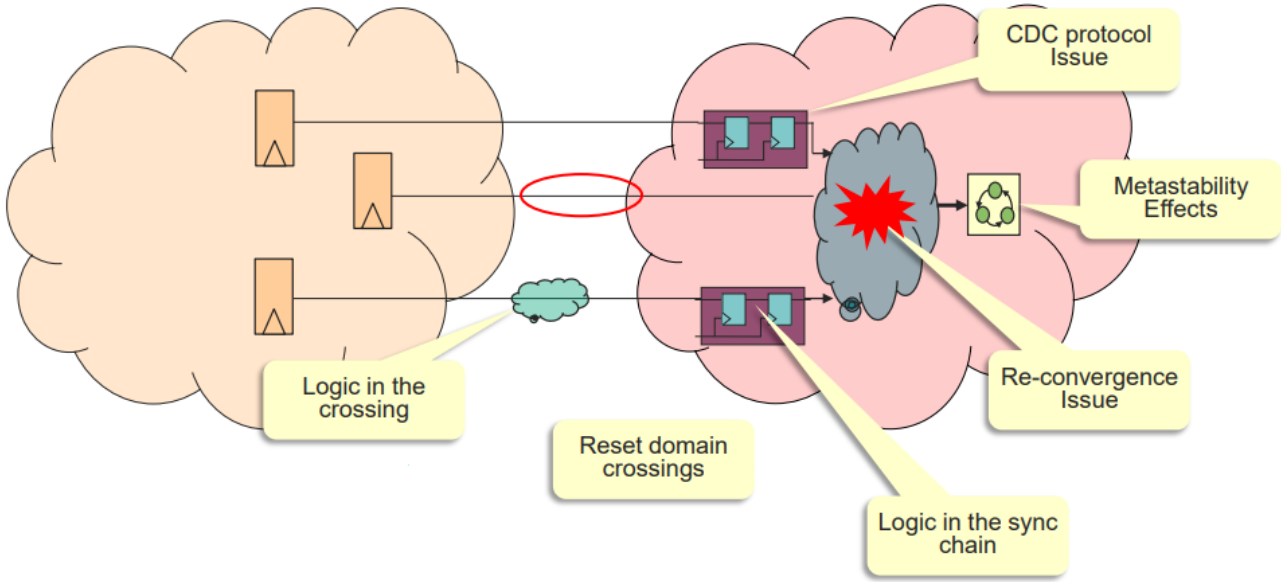
- Missing synchronizers
- Combinational logic on CDC path
- Structural glitch

CDC protocol violations

- Standard synchronization scheme-specific transfer protocol related issues
- Custom synchronization scheme-specific issues

Data coherency issues

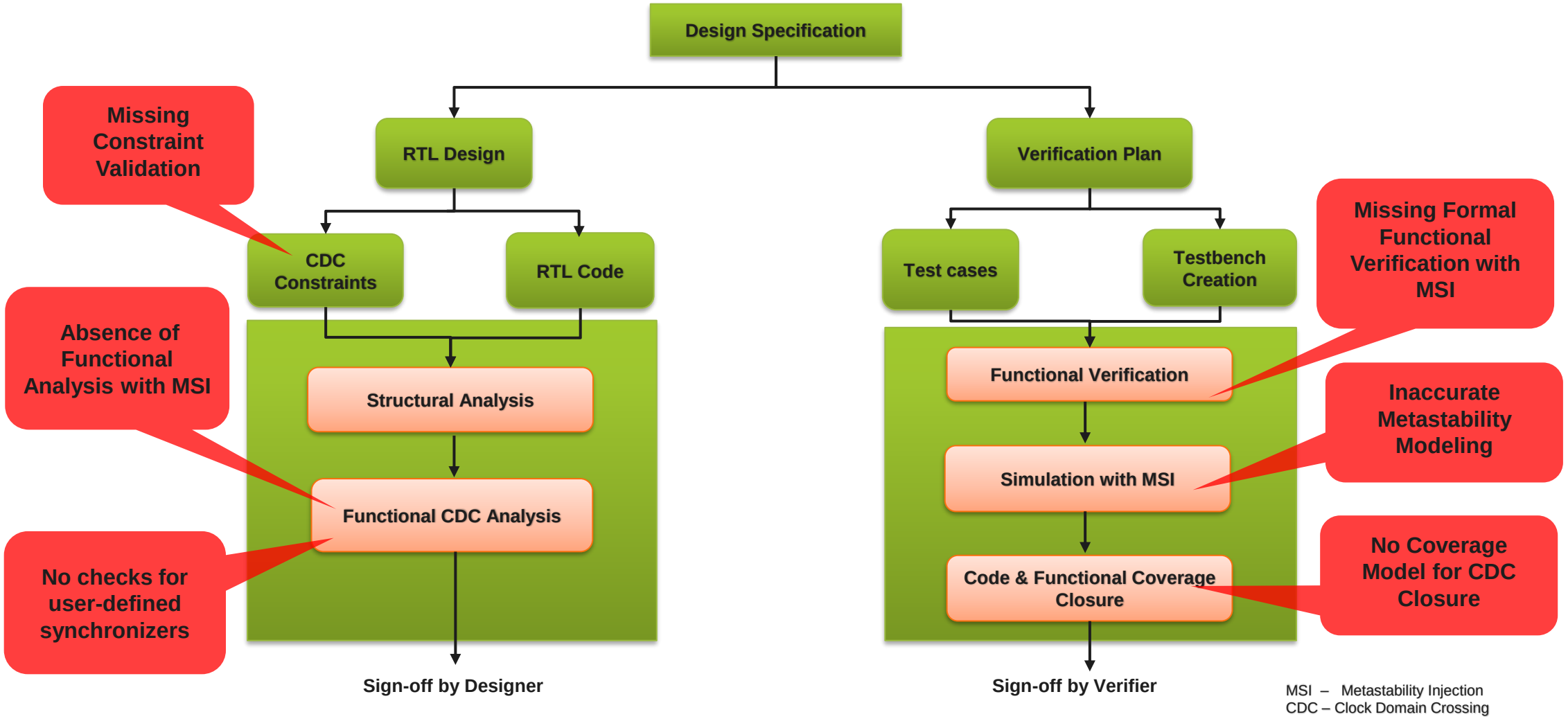
- Convergent/divergent/re-convergent design structures



Reset domain crossing

- Reset related violations

Conventional CDC verification



MSI – Metastability Injection
CDC – Clock Domain Crossing

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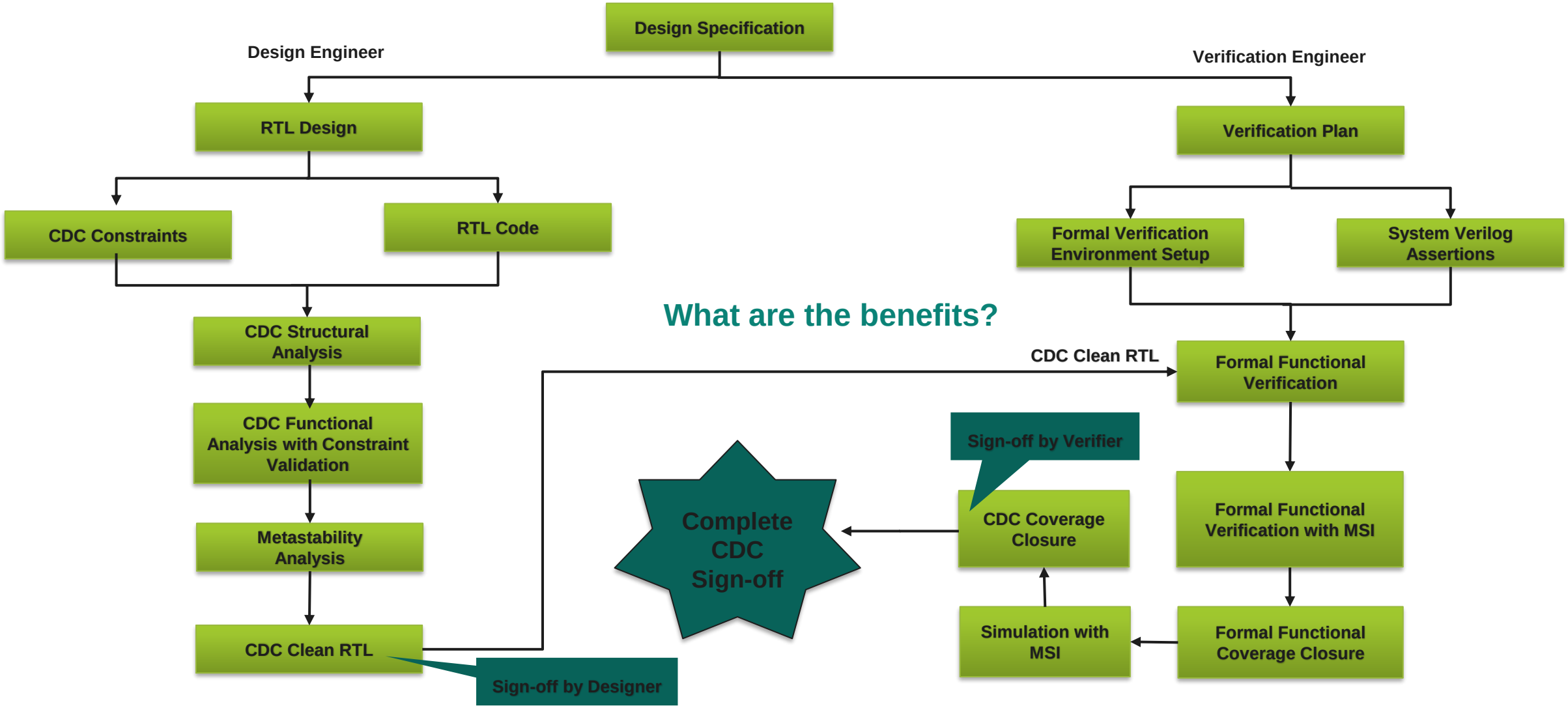
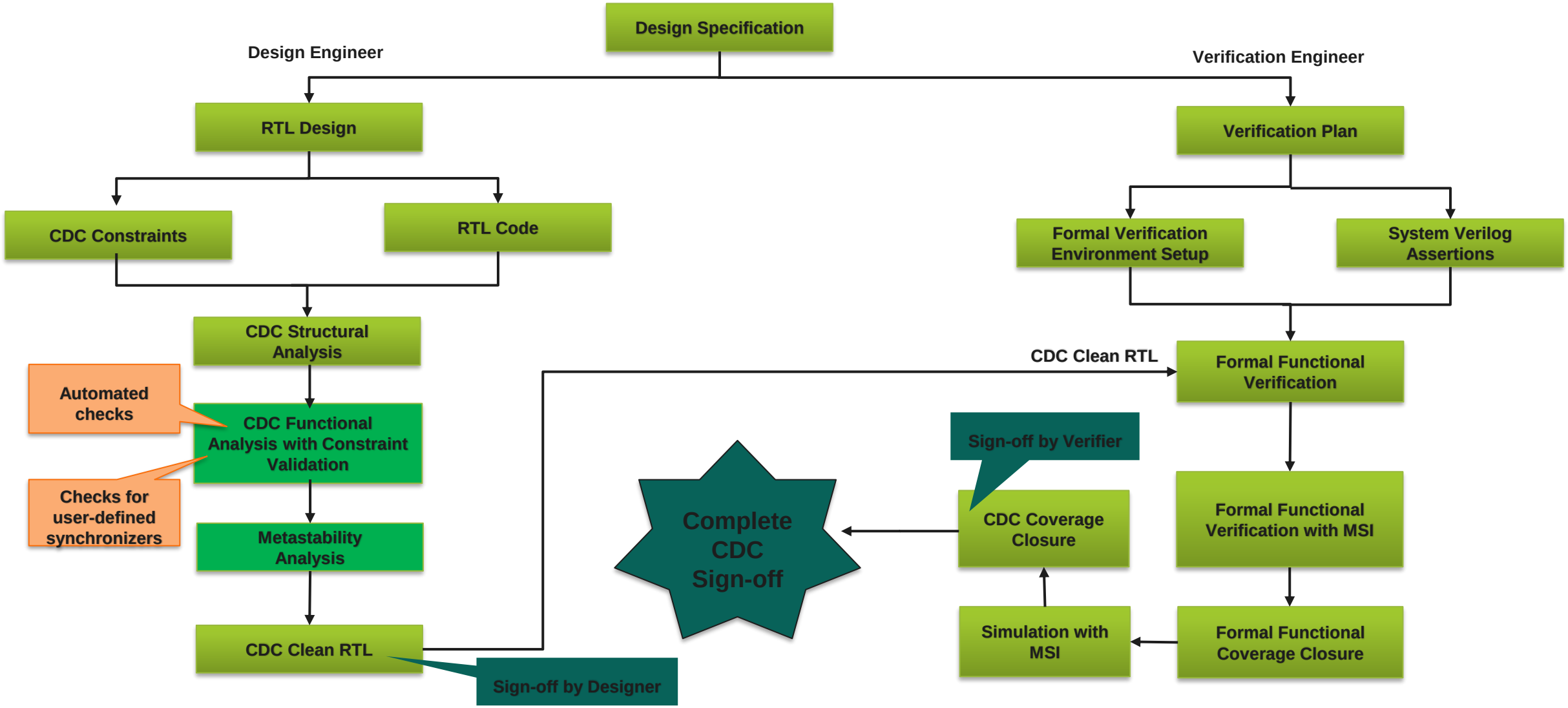
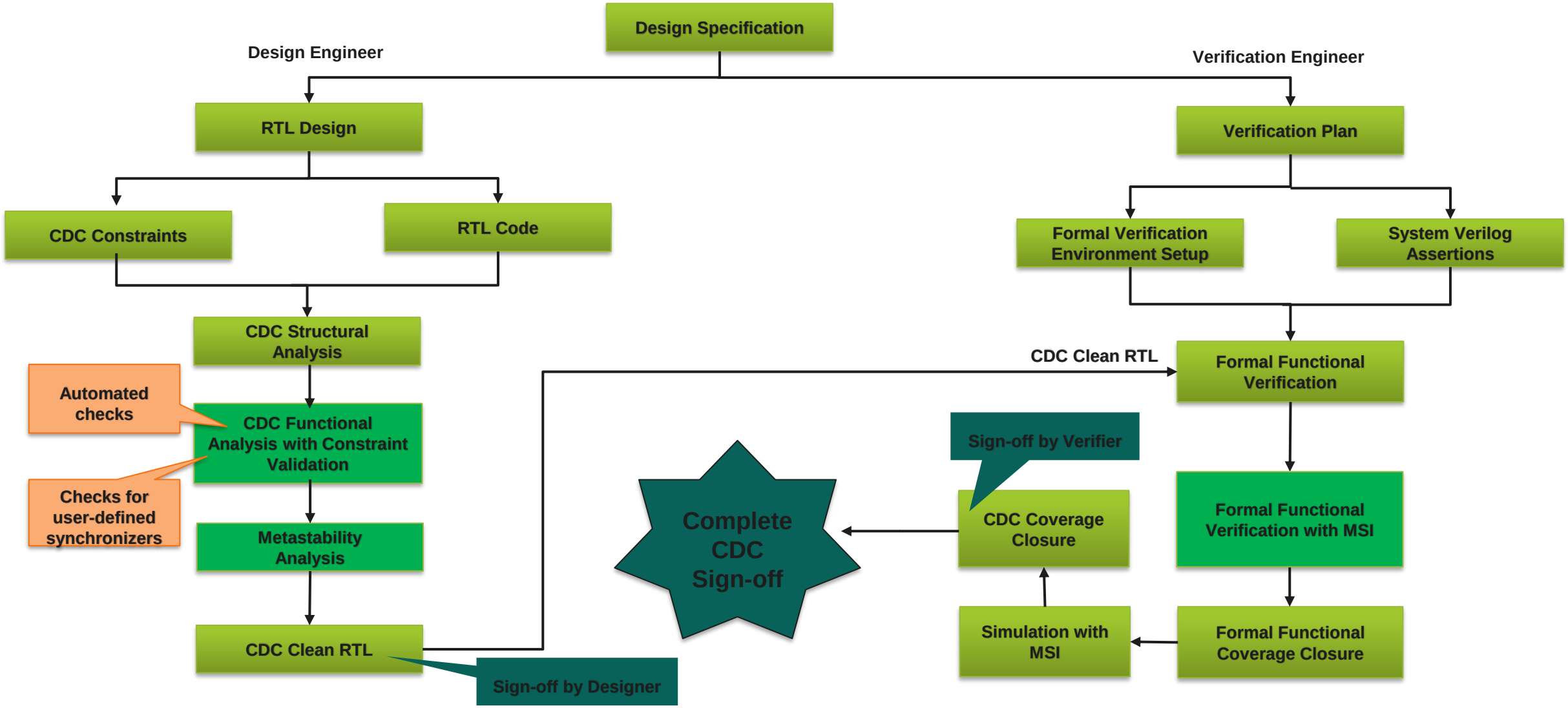
Proposed CDC verification flow



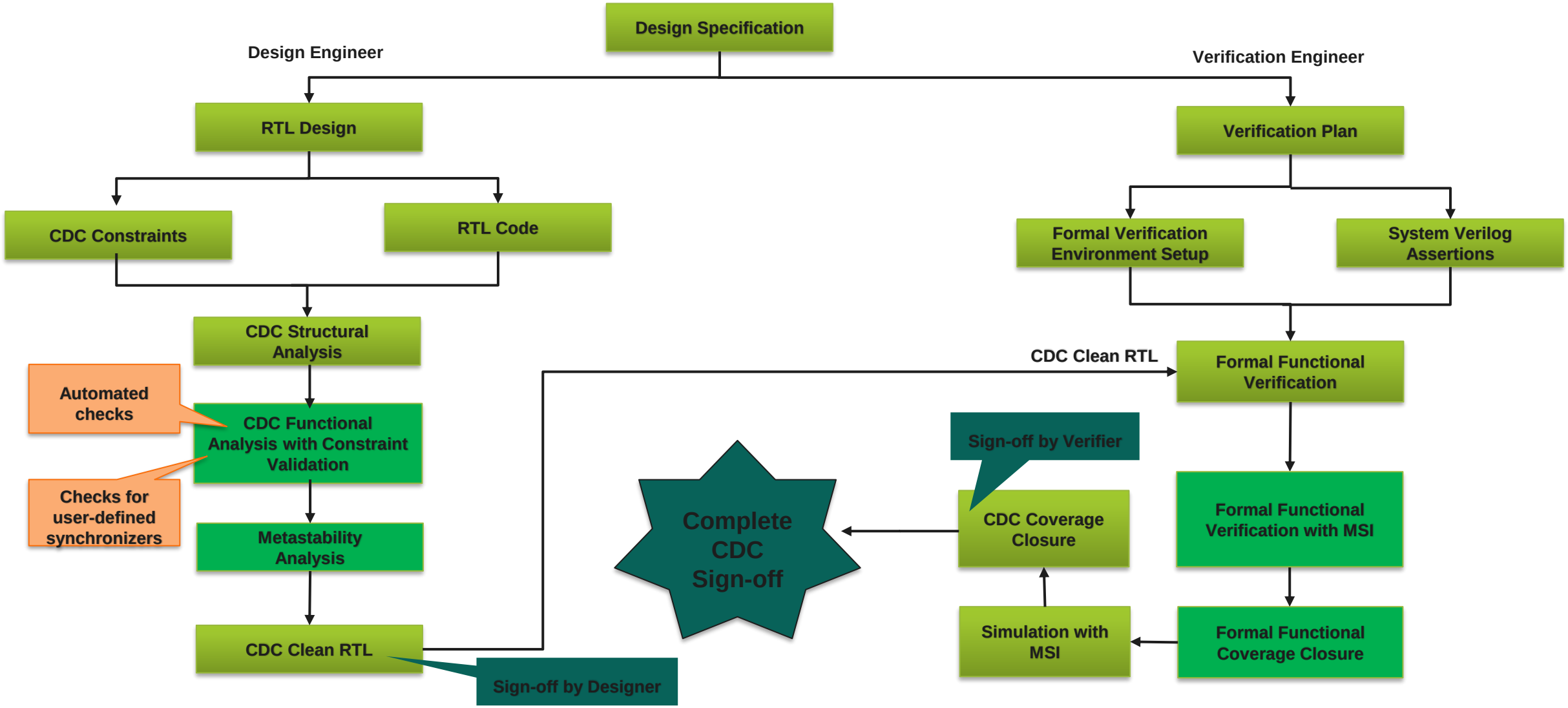
Proposed CDC verification flow



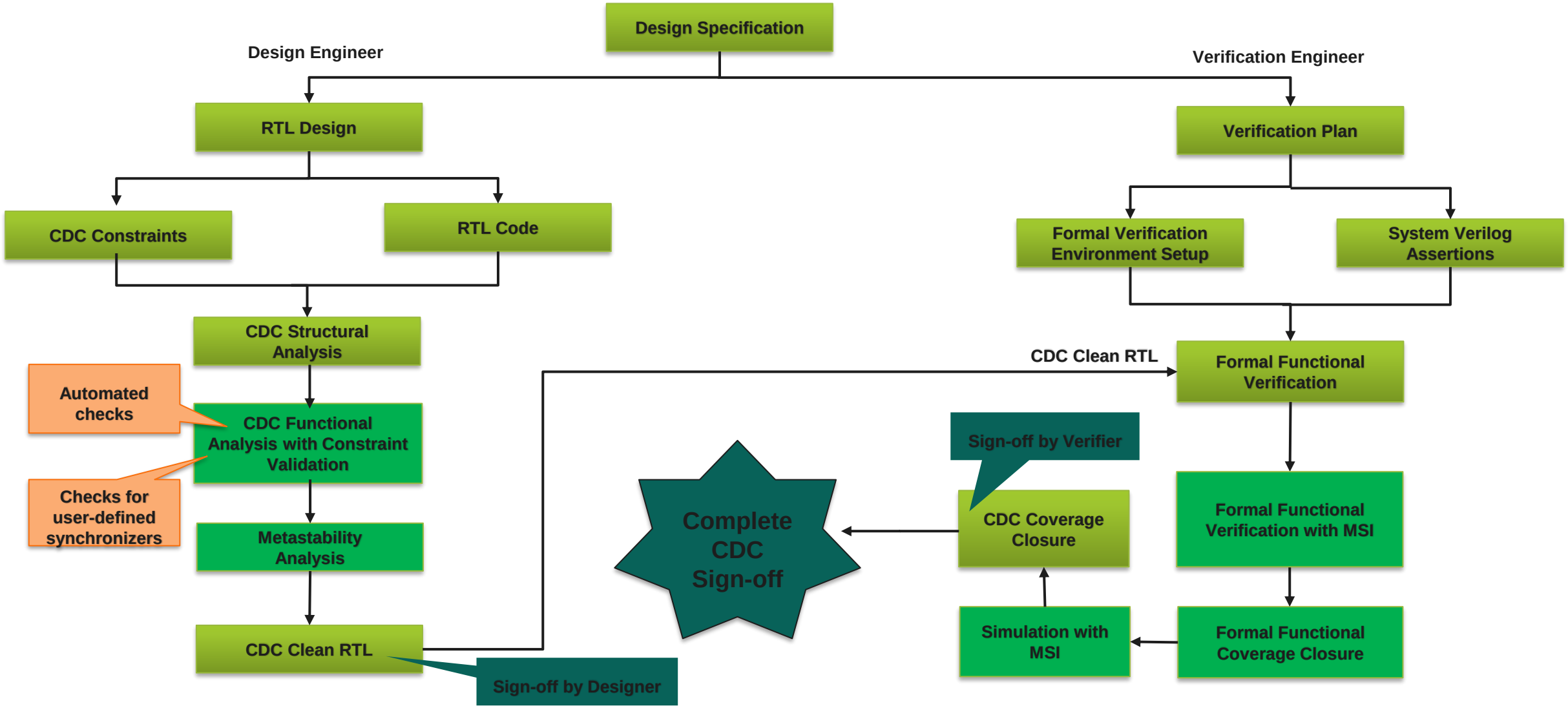
Proposed CDC verification flow



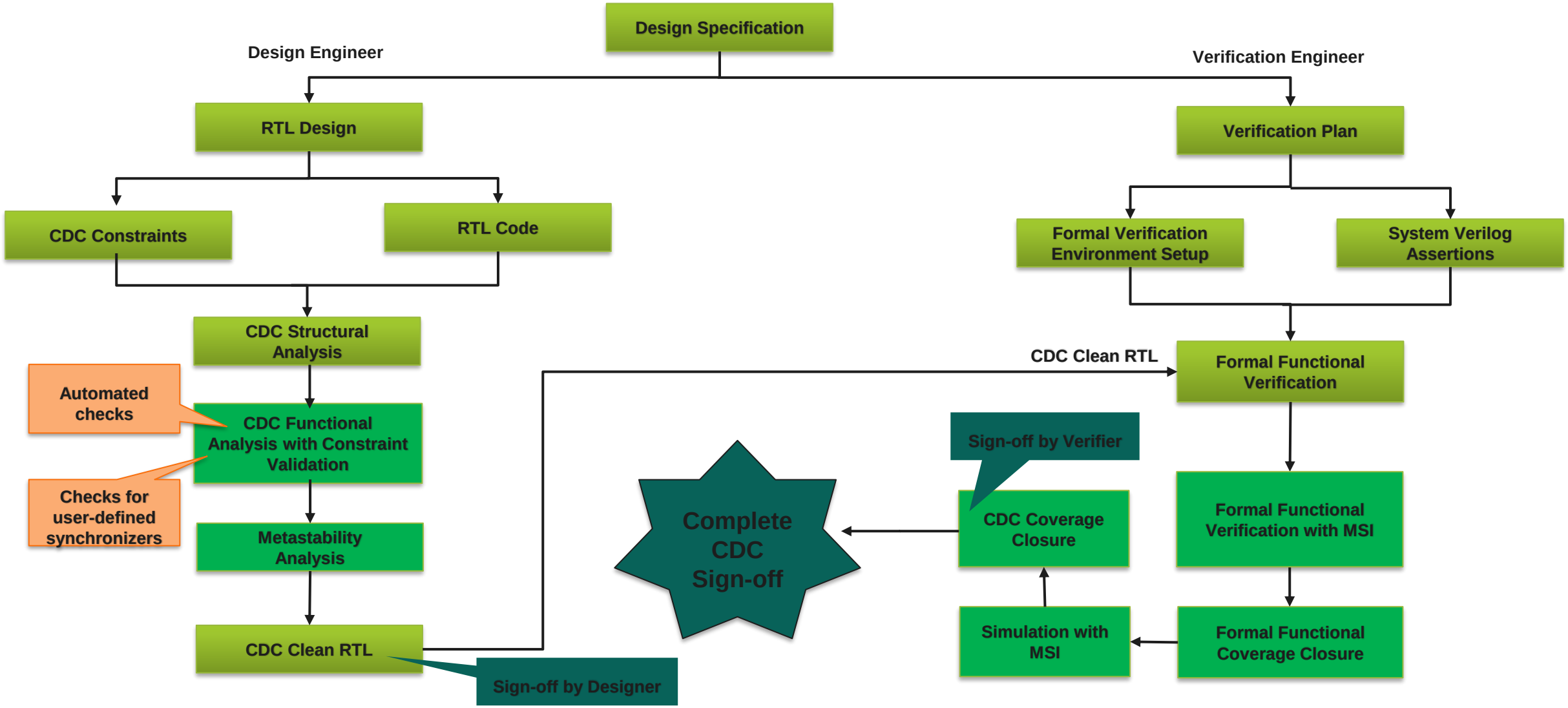
Proposed CDC verification flow



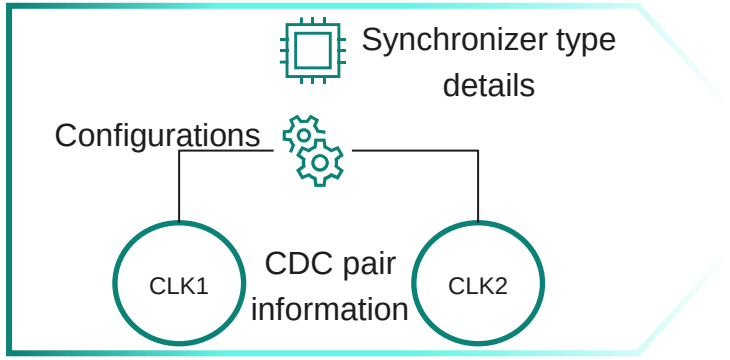
Proposed CDC verification flow



Proposed CDC verification flow



Metamodeling



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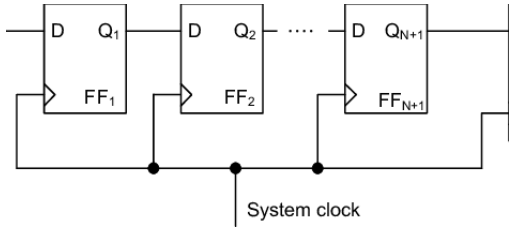


PROPERTIES

```
property data_stable;
 @(posedge clk1) disable iff (!rst_n)
  $stable(data_i) [*2];
endproperty
```

Metamodel
UML class diagram

Spec layer

Model of Things (MoT)
Formalized specification

Property layer

Template of Property (ToP)
Python

Generation Framework

View layer

Target Code
SVA/SV

METAMODEL

ndff_sync
num_stage: string[1] prim_clk: string[1] sec_clk: string[1]

MODEL

ndff_sync
num_stage: 2 prim_clk: clk1 sec_clk: clk2

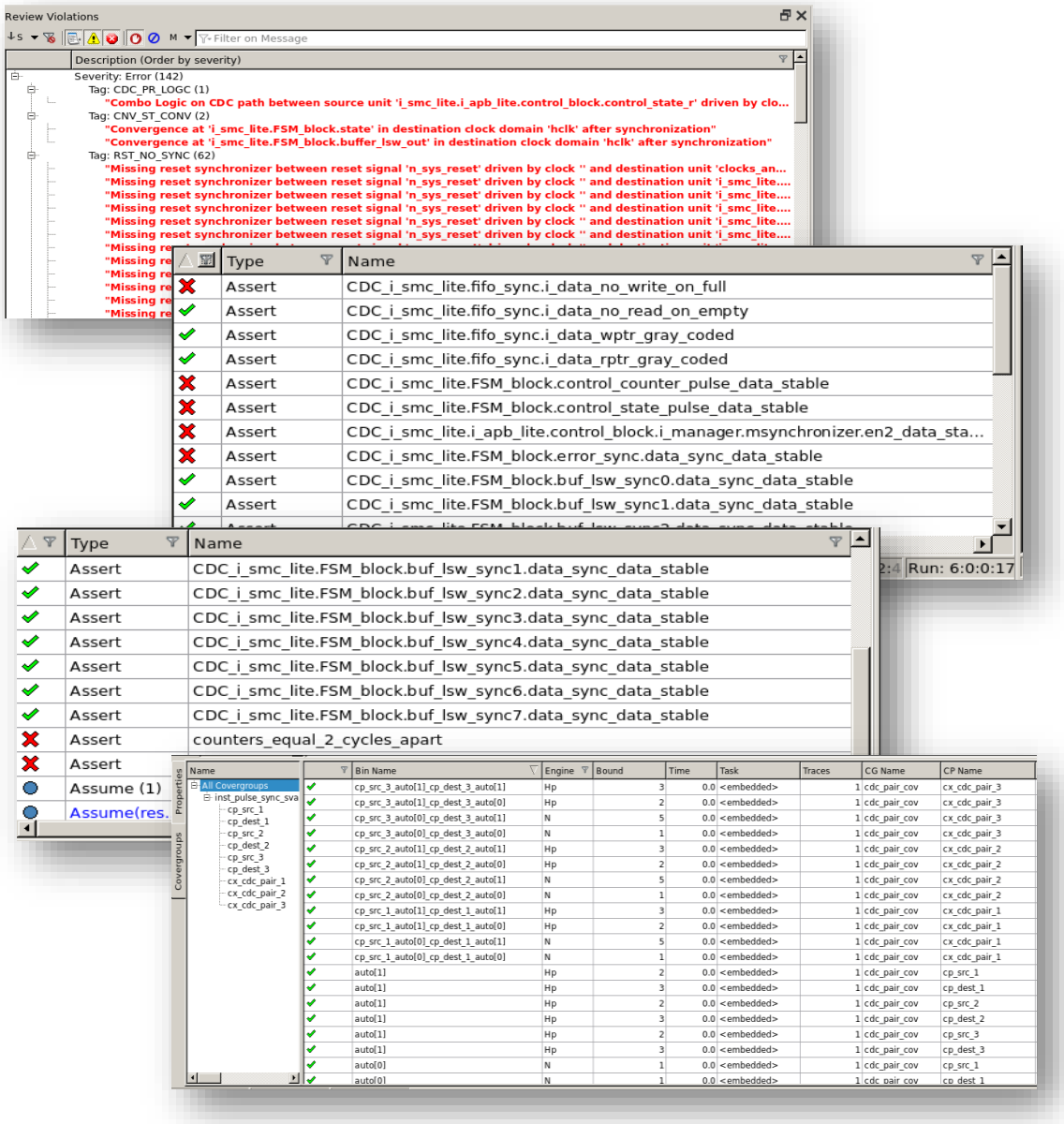
COVERAGE

```
covergroup cg @(posedge clk)
  cp_src: coverpoint sig_src
  cp_dest: coverpoint sig_dest
  cp_cdc pair: cross cp_src, cp_dest
```

Agenda

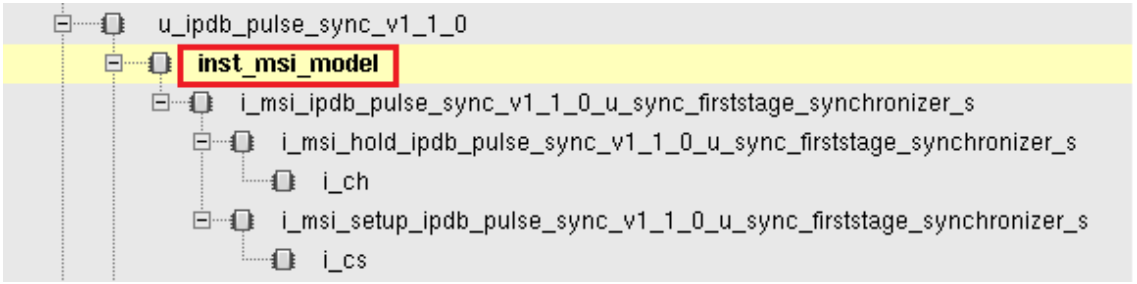
Bugs detected

Type	Analysis Used	Bug Description
RTL bug	Structural analysis	Missing synchronizer for CDC signal
RTL bug	Structural analysis	Missing synchronizer for RDC signal
RTL bug	Structural analysis	Combinational logic on the CDC path
RTL bug	Structural analysis	Combinational logic on the RDC path
RTL bug	Structural analysis	Reset signal converged before reaching the destination unit
RTL bug	Functional analysis	Wrong signal configuration (signal not static)
RTL bug	Functional analysis	Signal not stable enough to be captured correctly by destination unit
Testbench bug	Functional analysis	Input pulse was more than 1 cycle wide (pulse synchronizer)
Testbench bug	Functional analysis	Data loss because of incorrect clock frequencies
Testbench bug	Metastability analysis	Assertion didn't handle the extra delay due to metastability propagation
Tool bug	MSI model generation	MSI model was not getting generated for simulation

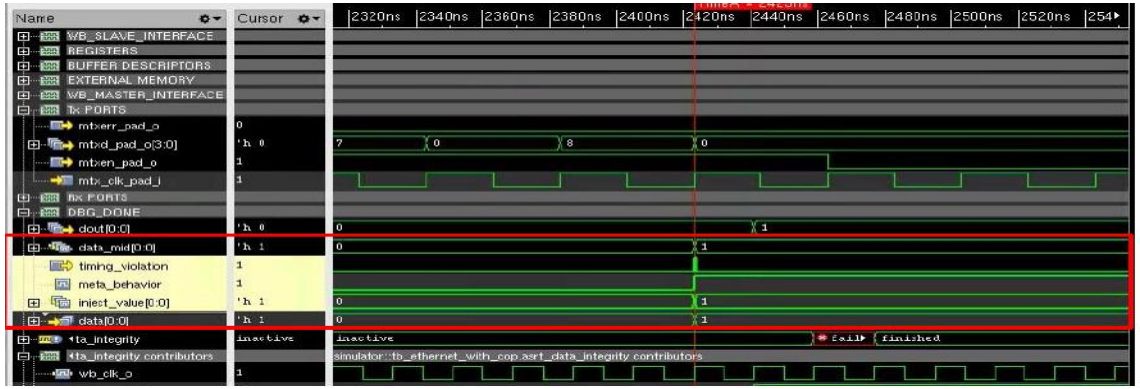


CDC verification on chip level

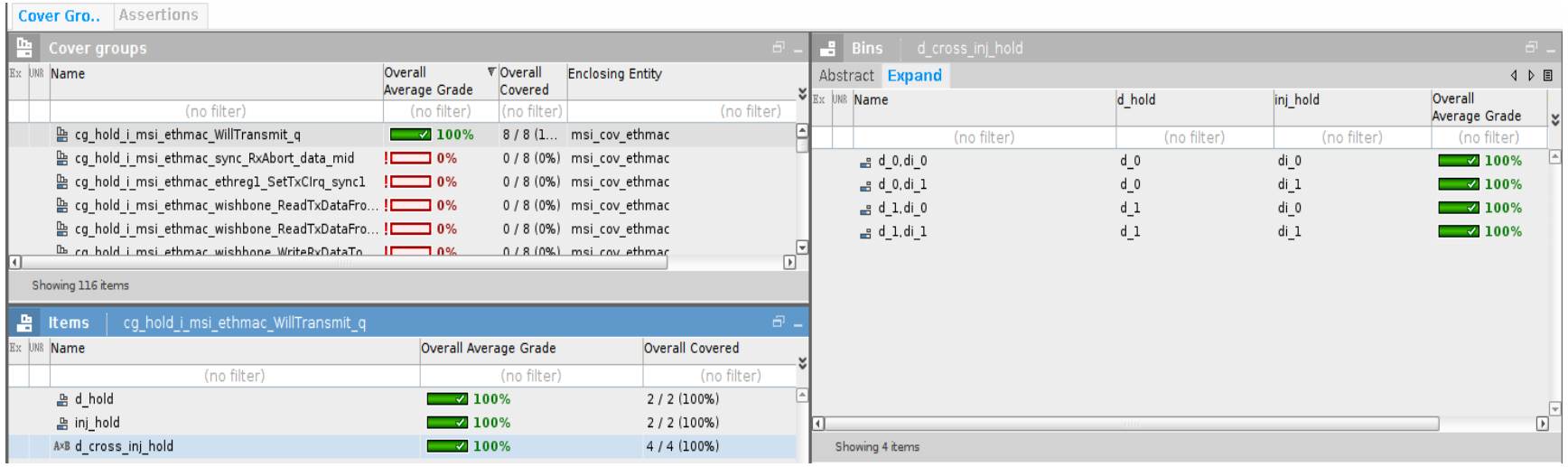
– MSI model integration to the simulation testbench



– Simulation waveform



– CDC coverage analysis



Summary

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Early detection of CDC bugs

- Detection of bugs at the pre-silicon verification phase
- Less effort/time to fix the bug
- Saves money by avoiding costly re-spin

2

Features

- Uses both formal & simulation techniques
- High-quality design ensured with coverage analysis
- Automated assertion checks

3

Design & verification linkage

- Bridges the gap between structural and functional analysis
- Defines a CDC sign-off flow for both design and verification

4

Future work

- Detection of more synchronizer schemes
- Automated testbench generation for MSI in simulation
- Application in power-aware

Pragmatic CDC formal verification


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