

Pragmatic Formal Verification Methodology for Clock Domain Crossing

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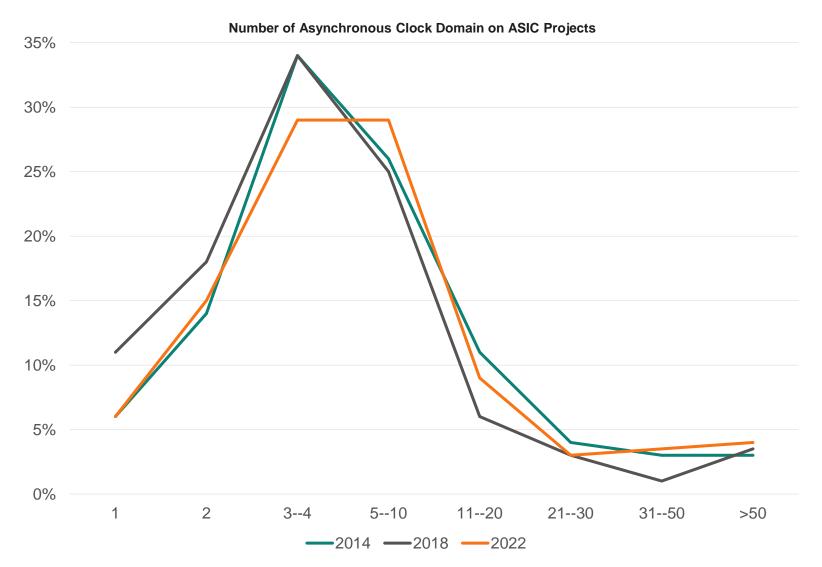
1	Verification challenges	3
2	Technical background	6
3	Methodology development & implementation	10
4	Results and summary	18



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Clock domains are increasing with increasing complexity



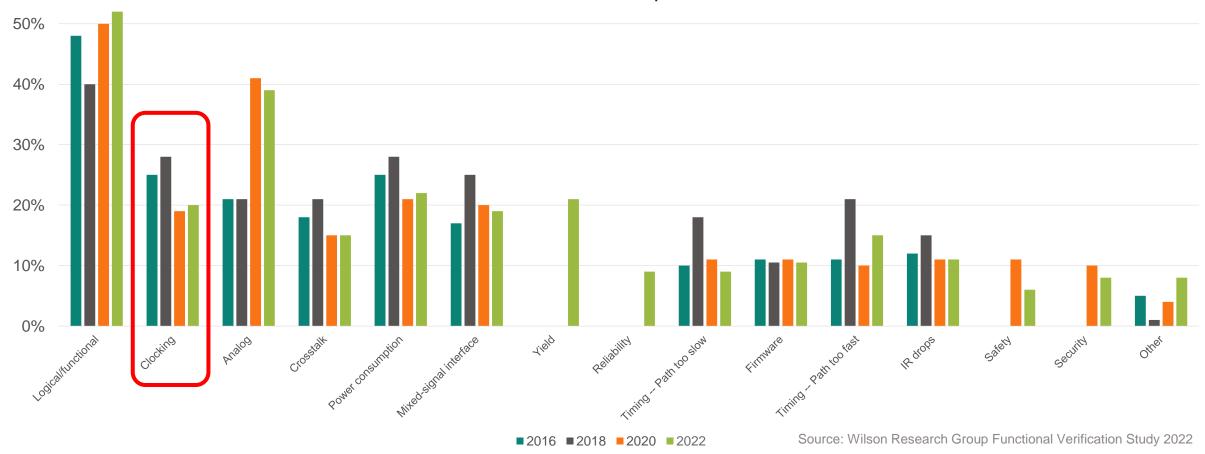
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Average number of clock domains on ASIC designs

Source: Wilson Research Group Functional Verification Study 2022



CDC issues are a major reason for expensive respins



Cause of ASIC Respins

– CDC issues are 3rd major reason for Silicon respins

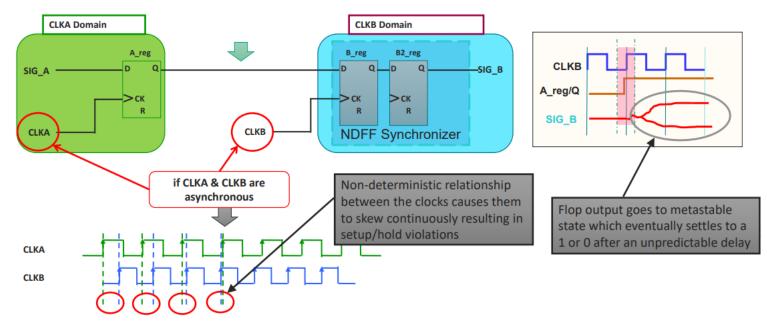


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Clock domain crossing and metastability

- A clock domain (CD) is a region of synchronous logic with exactly one clock
- Most real-life designs operate on multiple clocks (for power and performance reasons)
- A clock domain boundary arises when the clocks change



Source: Cadence JasperGold CDC user guide

- Signals crossing clock domains must be synchronized to avoid metastability effects!
- Metastability modeling \rightarrow creating setup/hold violations



CDC issues

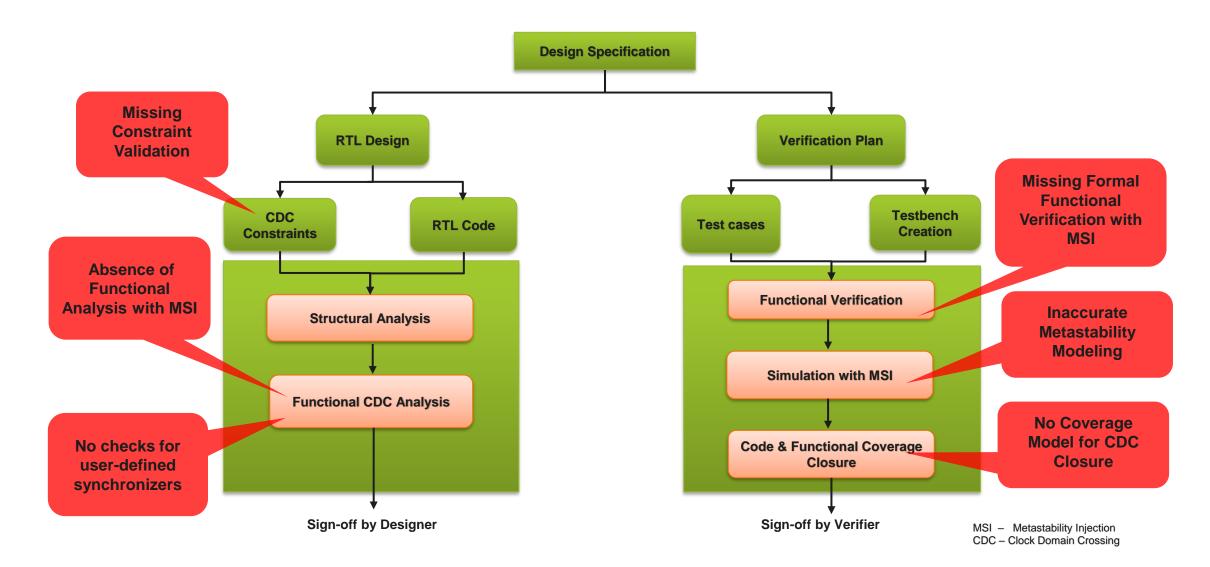
------**Structural violations** CDC protocol Issue Missing synchronizers _ Combinational logic on CDC path _ Metastability Effects Structural glitch _ X **CDC** protocol violations Re-convergence Logic in the Issue crossing Reset domain crossings Standard synchronization scheme-specific transfer _ Logic in the sync protocol related issues chain Custom synchronization scheme-specific issues — 20,00 **Data coherency issues Reset domain crossing**

Convergent/divergent/re-convergent design structures

Reset related violations



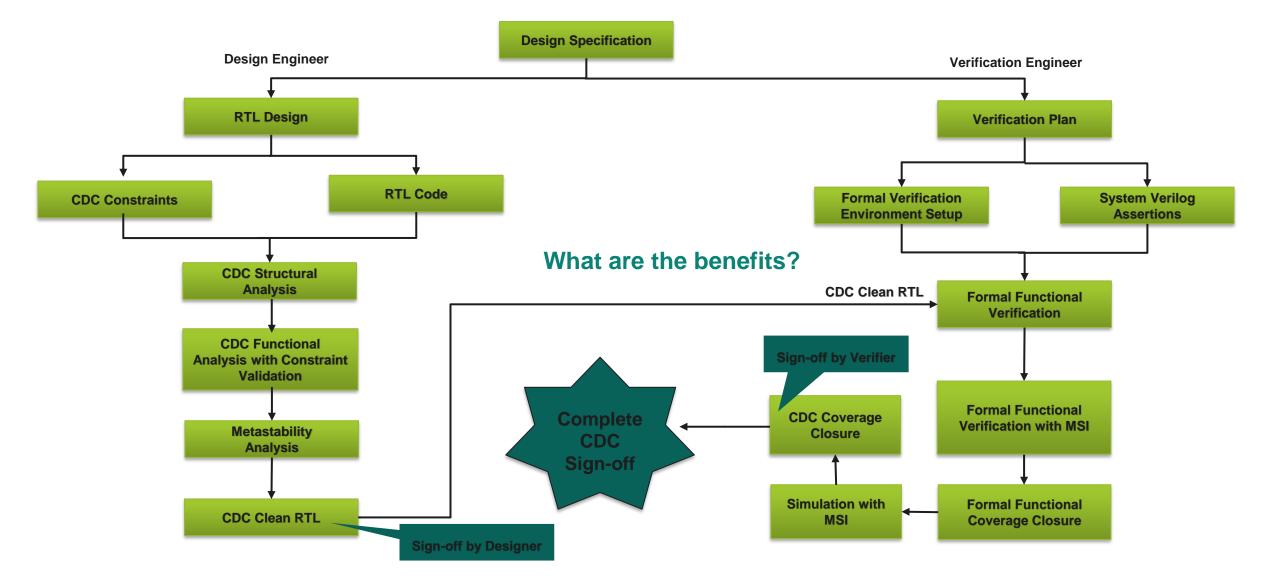
Conventional CDC verification



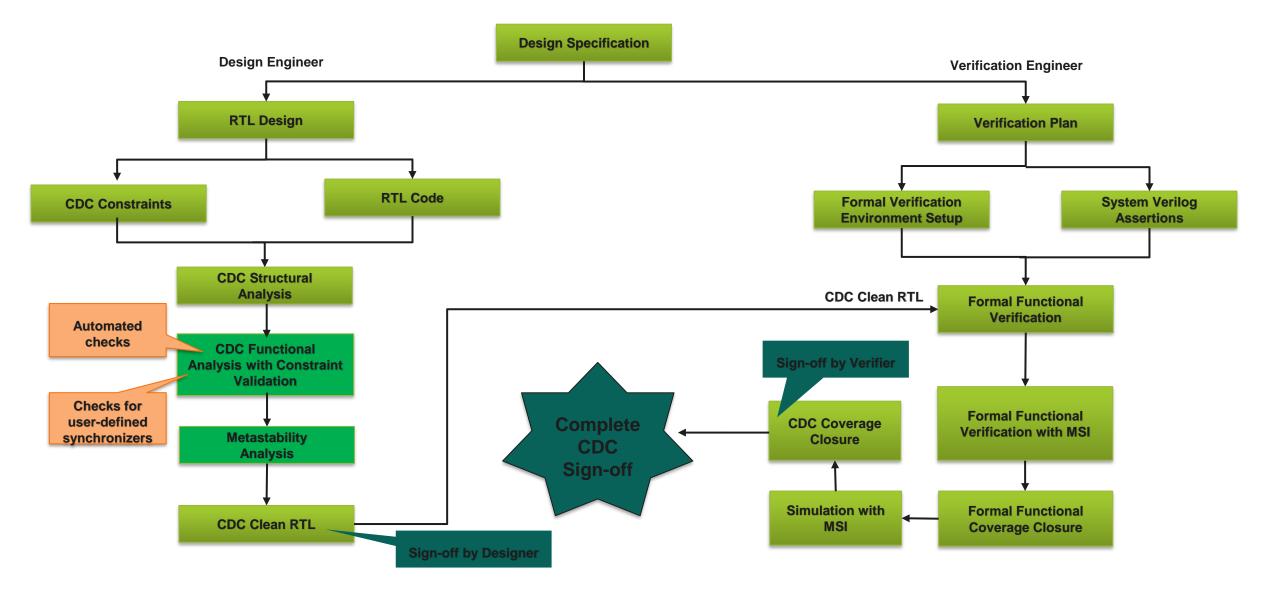


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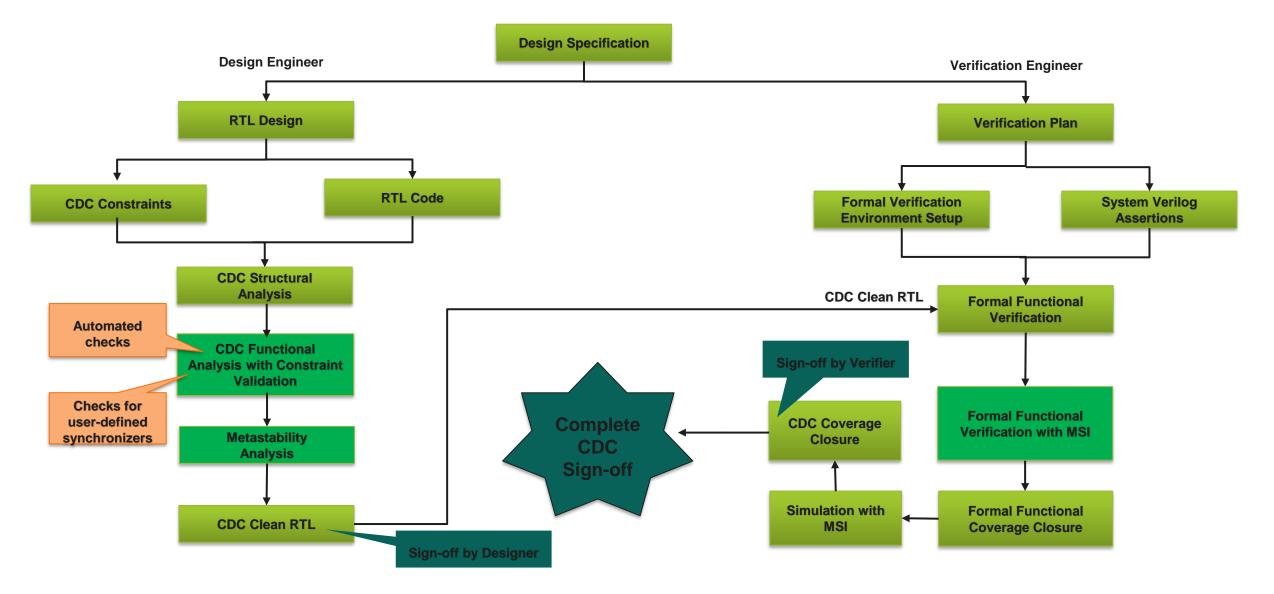




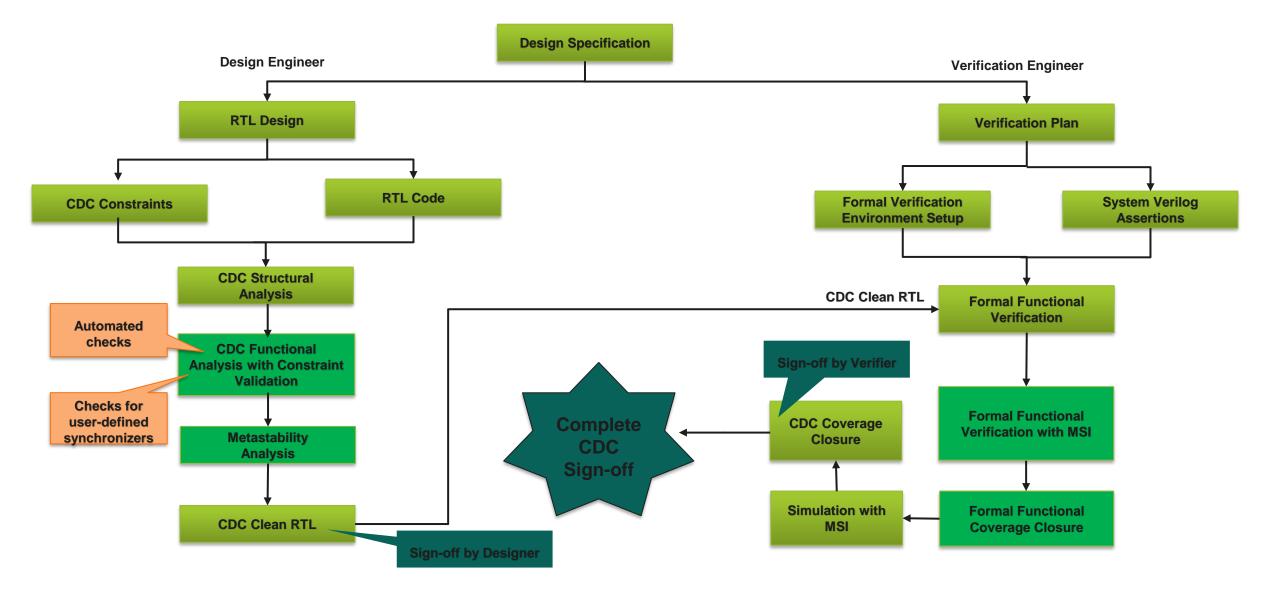




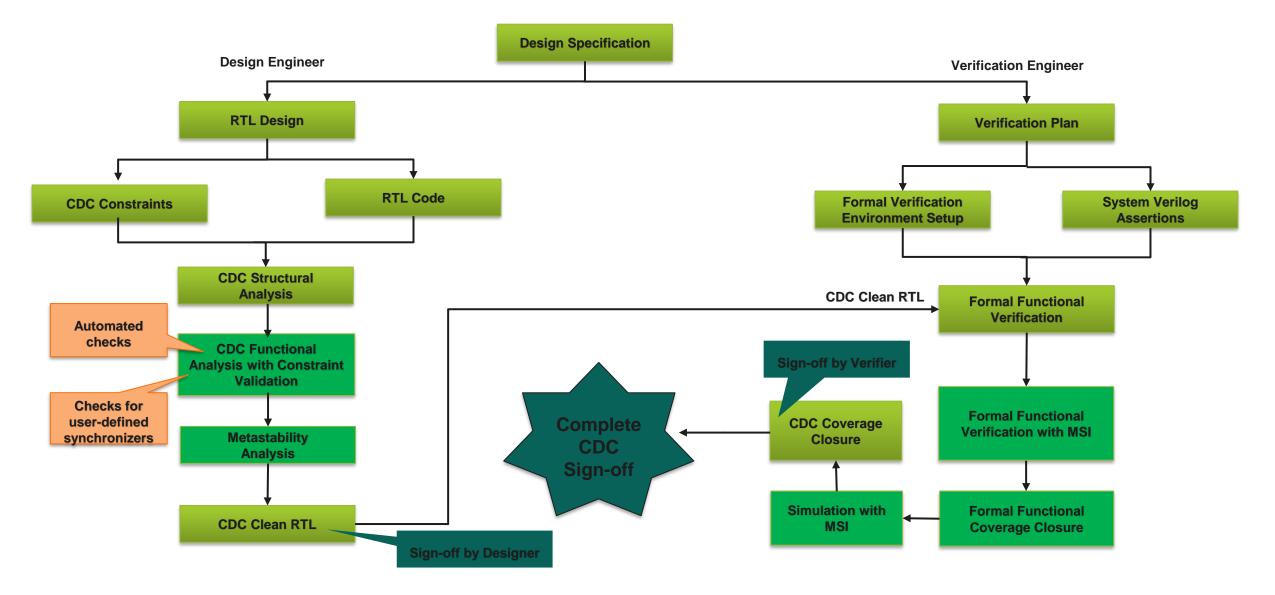




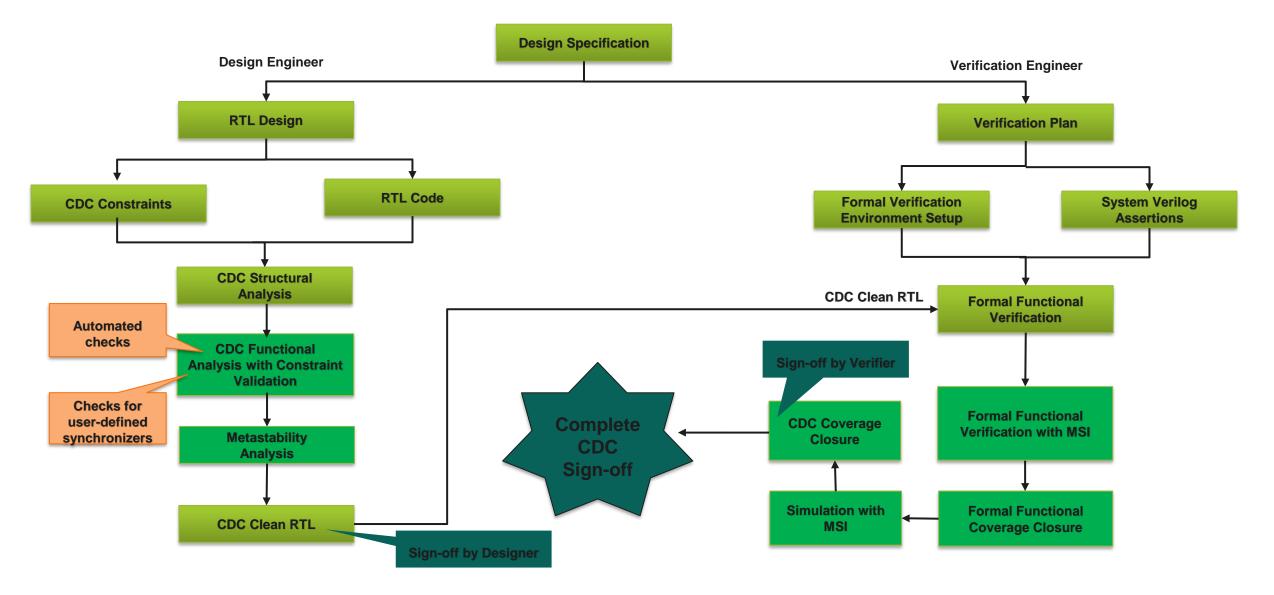














Metamodeling

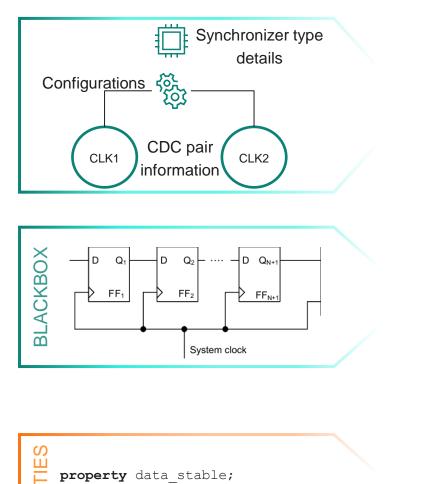
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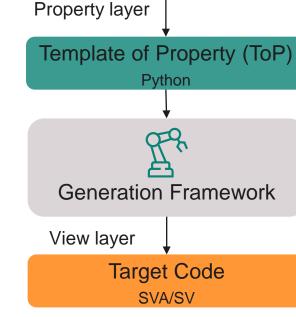
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@(posedge clk1) disable iff (!rst n)

\$stable(data i) [*2];

endproperty



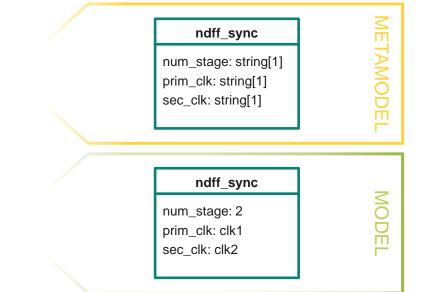
Metamodel

UML class diagram

Model of Things (MoT)

Formalized specification

Spec layer



covergroup cg @(posedge clk)
cp_src: coverpoint sig_src
cp_dest: coverpoint sig_dest
cp_cdc pair: cross cp_src, cp_dest

COVERAGE



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Bugs detected

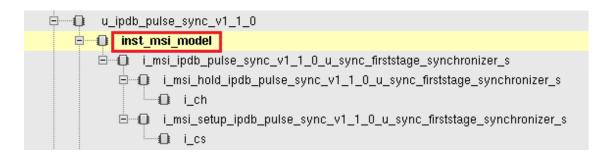
Туре	Analysis Used	Bug Description
RTL bug	Structural analysis	Missing synchronizer for CDC signal
RTL bug	Structural analysis	Missing synchronizer for RDC signal
RTL bug	Structural analysis	Combinational logic on the CDC path
RTL bug	Structural analysis	Combinational logic on the RDC path
RTL bug	Structural analysis	Reset signal converged before reaching the destination unit
RTL bug	Functional analysis	Wrong signal configuration (signal not static)
RTL bug	Functional analysis	Signal not stable enough to be captured correctly by destination unit
Testbench bug	Functional analysis	Input pulse was more than 1 cycle wide (pulse synchronizer)
Testbench bug	Functional analysis	Data loss because of incorrect clock frequencies
Testbench bug	Metastability analysis	Assertion didn't handle the extra delay due to metastability propagation
Tool bug	MSI model generation	MSI model was not getting generated for simulation

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	Tag: RST_NO_SY	(NC (62)									
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CDC verification on chip level

- MSI model integration to the simulation testbench



- Simulation waveform

Name ••	Cursor	Ø-	2320ns	2340ns	2360ns	2380ns	2400ns	2420ns	2440ns	2460ns	2480ns	2500ns	2520ns	254►
BEST WE_SLAVE_INTERFACE					10 .St.	300 (B)	10			20 - 30		10 20		-
REGISTERS			8.	_	_					_	_	_	_	
BUFFER DESCRIPTORS	-	_	_	_	_	_	_	- ¥	_	_	_	_	_	-
- WB_MASTER_INTERFACE		_		_	_	_	_			_	_	_	_	_
D BAR TX PORTS														
📰 mtxerr_pad_o	0													
⊕-• \$} mt ×d_pad_o[3:0]	'h 0		7	0		8		X o						
mtxen_pad_o	1													
mt×_cik_pad_i	1													
🖽 - 📾 🗛 PORTS														
DBG_DONE									- X					
⊕ ®_→ dout[0:0]	'h 0		0						1					
🛱 - 👫 💼 data_mid[0:0]	'h 1		0					1						
timing_violation	1													
meta_behavior	1													
Ⅲ 1000000000000000000000000000000000000	'h 1		0					1						
🕀 🛶 🗊 data (0:0)	'h 1		0					1						
⊕ <u>me</u> s	inactiv	re i	inactive							Siail*	finished			
ta_integrity contributors			simulator tb_	_ethernet_w	/ith_cop.asr	t_clata_integ	grity contribu	itors				1		
wb_clk_o	1													

CDC coverage analysis

Co	ver Gro Assertions								
b.	Cover groups								
Ex U	Name		Overall Enclosing E	ntity	Abs	tract Expand			۵ ۵
	(no filter)	Average Grade (no filter)	Covered (no filter)	(no filter)	Ex UN	Name	d_hold	inj_hold	Overall Average Grade
	🖺 cg_hold_i_msi_ethmac_WillTransmit_q		8 / 8 (1 msi_cov_e			(no filter)	(no filter)	(no filter)	(no filter)
	🖺 cg_hold_i_msi_ethmac_sync_RxAbort_data_mid		0/8(0%) msi_cov_e	hmac	1	d_0,di_0	d_0	di_0	✓ 100%
	腔 cg_hold_i_msi_ethmac_ethreg1_SetTxCIrq_sync1	0%	0/8(0%) msi_cov_e	hmac			d_0	di1	✓ 100%
	🖺 cg_hold_i_msi_ethmac_wishbone_ReadTxDataFro	0%	0/8(0%) msi_cov_e	hmac		📑 d_1,di_0	d_1	di_0	100%
	🖺 cg_hold_i_msi_ethmac_wishbone_ReadTxDataFro	0%	0/8(0%) msi_cov_e			📇 d_1,di_1	d_1	di_1	✓ 100%
1	🗅 ca hold i msi ethmac wishhone WriteRxDataTo	0%	0/8(0%) msi cov e	hmac 💌	1				
s	howing 116 items								
	Items cg_hold_i_msi_ethmac_WillTransmit_q			8 <u>-</u>					
Ex UP	^{IR} Name	Overall Avera	ge Grade	Overall Covered					
	(no filter)		(no filter)	(no filter)	1				
	🖺 d_hold	✓ 100 ^o	%	2 / 2 (100%)	1				
	🖺 inj_hold	100	%	2/2(100%)	•		IIIII		
	A×B d cross inj hold	√ 100	%	4 / 4 (100%)	S	howing 4 items			



Summary

Early detection of CDC bugs

- Detection of bugs at the pre-silicon verification phase
- Less effort/time to fix the bug
- Saves money by avoiding costly re-spin

2

Features

- Uses both formal & simulation techniques
- High-quality design ensured with coverage analysis
- Automated assertion checks



Design & verification linkage

- Bridges the gap between structural and functional analysis
- Defines a CDC sign-off flow for both design and verification



3

Future work

- Detection of more synchronizer schemes
- Automated testbench generation for MSI in simulation
- Application in poweraware

Pragmatic CDC formal verification

