

Power Aware CDC Verification at RTL for Faster SoC Verification Closure

Anindya Chakraborty, Member Consulting Staff, Mentor Graphics Corporation, Noida, India
(anindya_chakraborty@mentor.com)

Naman Jain, Sr. Engineering Manager, Mentor Graphics Corporation, Noida, India
(naman_jain@mentor.com)

Saumitra Goel, Lead Member Consulting Staff, Mentor Graphics Corporation, Noida, India
(saumitra_goel@mentor.com)

Innovations in design technologies and verification methodologies are creating complex SoCs that operate at very high speeds while incorporating optimal power management strategies to reduce power consumption. Design size inches towards multi-billion gates and designs incorporate multiple asynchronous clocks, IO-interfaces, cores and peripherals. The ever-increasing counts of asynchronous clocks—coupled with tight power constraints—pose interesting verification challenges that cannot be overlooked.

In this paper, we propose a Power Aware Clock Domain Crossing (CDC) verification methodology that accounts for the impact of power components on the CDC setup, results and verification. The methodology accounts for the ramifications of power management logic on CDC setup, clock tree analysis, reset tree analysis, domain crossing analysis and design synthesis. We highlight the impact of power elements (specifically isolation cells) on CDC results. The methodology can be extended to pure and partial gate-level designs as well as designs with power elements embedded in RTL. We also propose extending existing CDC checks with some power-aware specific checks. Note that although we express power intent in UPF format, the discussion is generic in nature. It is applicable to other forms of power specification.

Details from a customer who has used this methodology are included in this paper. They share their experience with plain CDC verification vs. Power Aware CDC verification—on both RTL and gate levels. Their experience has helped us determine our proposal and refine our methodology. In this paper, we show that Power Aware CDC analysis at RTL level is a fast and efficient way of addressing CDC verification issues in the presence of power information.

Keywords— Design Verification, CDC, Verification, Low Power, UPF, Isolation Cells

I. INTRODUCTION

Setup for CDC verification can be difficult for a design with no power information. But, accounting for power intent makes this process harder. Power components and power control intent of a design usually are specified in a power constraints file and the Unified Power Format (UPF) is the IEEE standard for these files. They provide information about power domains and about additional logic required to manage the interactions between power domains. This additional logic may be—or may not be—part of the RTL design. However, the final chip has this synthesized logic embedded within its design components.

CDC verification of an RTL design is not sufficient when it does not take into consideration the impact of the design's power constraints. These constraints add vital information about power domain transitions and power management components that interact with design logic. If ignored, such components can lead to unverified crossings, which might cause failures in the final chip.

Currently, most verification teams either ignore the impact of power information. Or, they rely on ad-hoc approaches to CDC verification of low-power designs. Such methods are not exhaustive and rely on the judgment of verification engineers. These approaches can lead to hard-to-detect bugs that are caught late in the design flow or in silicon—or maybe go completely undiscovered until it's too late.

The first step in CDC setup is: identify the clocks and the clock trees. Power artifacts inserted into a clock path (such as isolation cells and level shifters) can impact CDC analysis. Such cells in data or control paths also can affect the propagation of constraints provided to the verification tools. They could produce unforeseen clock domain changes. Most CDC verification tools report the primary clocks, clock trees and their relationships with each other. This is a good starting point for setting up power-aware CDC verification.

In addition to unforeseen changes in clock detection, grouping and propagation of user-specified and tool inferred constraints, the inserted artifacts have major impact on the structure of the design. These artifacts often introduce new paths that must be reviewed and if necessary, synchronized for a CDC-clean design. In addition, some power management artifacts can cause their associated synchronization schemes to break.

In the next section, we analyze the impact of power-element insertion on a design—specifically on clock paths, reset paths, constraints propagation and CDC analysis. We also analyze the newly-introduced domain crossings that need further CDC checking. In section III, we present our proposed methodology for finding these problems early in the CDC verification process and we describe new CDC violations related to isolation insertion that CDC tools should consider. Section IV gives an overview of using our methodology for gate-level designs. Section V shows our findings for a real customer design. Section VI provides a summary and proposes future directions.

II. IMPACT OF POWER ELEMENTS ON CDC VERIFICATION

A. Clock Paths

Consider an isolation cell inserted in a clock path, as shown in Fig. 1. In the absence of this isolation cell, *clk1* and *clk2* signals are considered part of the same clock group. However, when the isolation cell is inserted, *clk1* and *clk2* are separated by gating logic (the isolation cell). Their relationship and the clock tree might change.

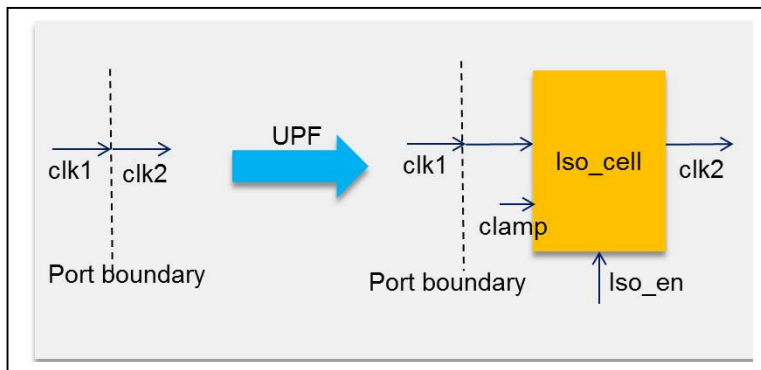


Figure 1. Isolation Cell inserted in the clock path.

(Note that a similar impact occurs when an isolation cell is inserted into a reset path.)

B. Constraint Propagation

Suppose that in the non-power-aware variant, the user provides a constraint on *en*, setting it to 1. Then, *g_clk* is assumed synchronous to *clk1*. But the insertion of an isolation cell affects constant propagation and so, *g_clk* is not considered synchronous to *clk1*. Figure 2 illustrates this issue.

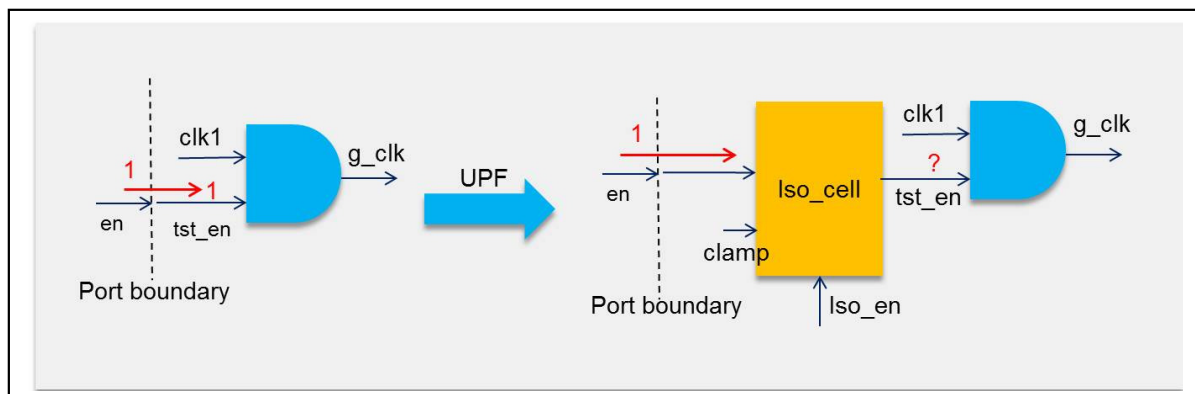


Figure 2. Isolation cell impacts constraint propagation

C. New Black Boxes

Black boxes are modules in the design for which only the interface is visible to the tool. Their internal logic is not available for analysis. These are usually caused by tool limitations such as encrypted HDL code and unsupported or non-synthesizable constructs. Synthesis and simulation tools usually do not allow black boxes and error out in their presence. In general CDC tools tolerate black boxes, however they might cause problems during CDC analysis, since spurious violations can be reported. Alternately, if the user does not carefully constrain black-box interfaces, CDC analysis might miss valid crossings.

UPF logic can insert black boxes if the user specifies custom power elements that are themselves black boxes. For example, this can be done through a *map* command such as *map_isolation_cell* or *map_retention_cell*. These new black boxes could create more violations and could reduce the visibility inside certain modules, which hinders CDC verification.

D. Introduction of New Crossings

When isolation cells are inserted into the design, new isolation enable signal paths are introduced. Some of these isolation enable signal paths are driven by power-control logic in clock domains different from the isolated signals. This scenario is demonstrated in Fig. 3.

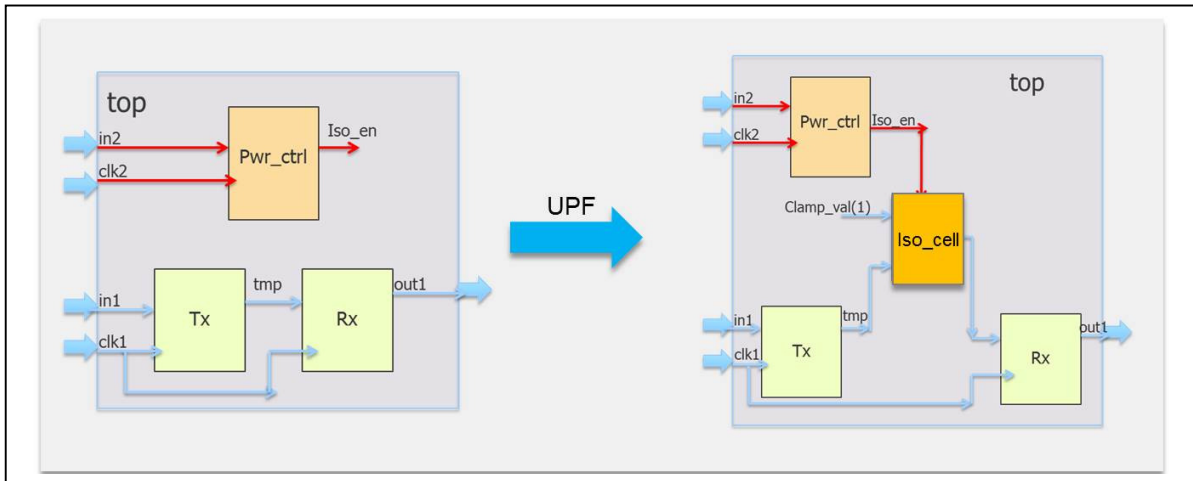


Figure 3. Isolation cell introduces new CDC path

E. Existing Synchronized Paths

UPF often introduces isolation cells in domain crossings that would be synchronized otherwise. This additional logic can cause unaccounted delays in these paths that might require additional timing verification and it can introduce glitches in certain circumstances (Fig. 4).

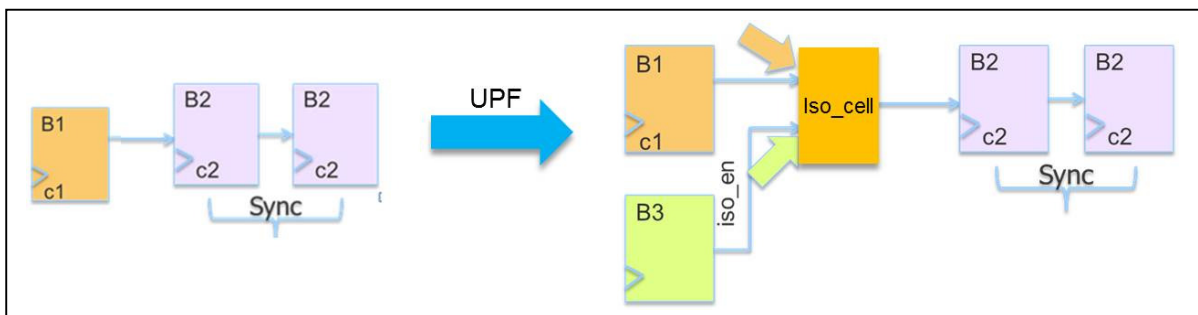


Figure 4. Isolation cell breaks existing synchronized path

Advanced domain analysis tools (such as Questa CDC from Mentor Graphics Corporation) use special checks to detect the issues created by power-aware artifacts introduced by power format files such as UPF (as described in section II-D and II-E). These tools help users quickly identify them as power-induced issues and provide debugging platforms for taking corrective action.

III. POWER AWARE CDC METHODOLOGY

Setting up the design analysis environment correctly is crucial for any verification process. For CDC analysis, the clock trees, reset trees and design topology must be verified before progressing ahead to verification. With power-aware designs this process is even more critical.

To avoid unforeseen problems caused by inserted power artifacts, primary clocks/resets, clock/reset trees and clock/reset relationships can be compared between the power-aware and the non-power-aware variants of the design. Any differences between the two must be carefully analyzed. The user should either rectify each problem or accept it as an expected deviation.

A. Ensure Sanctity of Clock Trees

Clock tree sanctity is necessary for correct CDC verification. Power intent specifications can introduce new elements in the clock paths, which can impact constant propagation and mode-specific analyses of the design. Problems in clock tree analysis in the presence of UPF are highlighted in Section II-A and II-B.

B. Ensure Sanctity of Reset Tree

Like clock trees, reset trees require analyses in presence of UPF layout over the design. The user should ensure that the power elements on the reset path do not alter the reset state of the design. (Note that the discussion in Sections II-A and II-B hold true for reset paths as well.)

C. Ensure No Extraneous Black Boxes in the Design

Black boxes, their impact, and how power intent can introduce black boxes are discussed in Section II-C. New black boxes can introduce more violations and they reduce the visibility inside their modules, making verification incomplete. The user should verify for CDC verification that the power intent specifications do not introduce extraneous black boxes. The user should properly constrain the ports of new black boxes when they are unavoidable.

D. Analysis of CDC Results

As discussed in Section II-D and II-E, power element insertion can introduce new unsynchronized crossings or break existing synchronizers. A power-aware CDC tool can capture and categorize these violations.

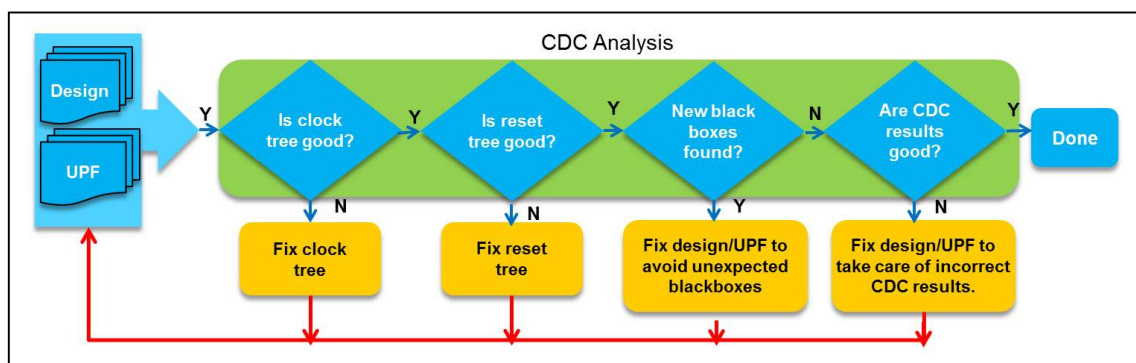


Figure 5. Iterative CDC methodology

The Power Aware CDC methodology described above is an iterative process. Each step in the proposed methodology points to potential bugs that might require corresponding changes in the design or the UPF. So, each time the RTL or UPF is changed, another iteration of the steps in the methodology are needed as shown in Fig. 5.

IV. EXTENDABLE TO MIXED RTL/GATE DESIGNS

Our proposed Power Aware CDC verification methodology is generic enough to also work for SOCs that might include external IPs and have design components as gate-level netlists. New CDC paths introduced by UPF are flagged and analyzed with this methodology on full or partial gate-level designs. The methodology applies also to designs with power artifacts embedded in RTL.

V. RESULTS

We tested our proposed methodology on a “real life” customer design at RTL level. A UPF file was applied on the design at the RTL level. Complete CDC analysis was performed for crossings and re-convergence issues. Then we analyzed a gate-level netlist that reflected both the RTL plus the UPF.

Complete power aware CDC analysis of the gate-level netlist on two blocks took 36 hours and 41 hours. Using our proposed methodology of performing CDC analysis of the RTL+UPF design, time taken was reduced by 40-50X.

A comparison of the overhead of CDC analysis on RTL with RTL plus UPF is illustrated in Table 1. Overhead introduced by UPF is not significant compared with the time taken to perform complete CDC at gate level. We found that another benefit of performing Power Aware-CDC at RTL is that turnaround time for fixes is quicker for RTL than for the netlist.

Table I. Time taken in PA-CDC on RTL Vs Netlist

Serial No.	Design Name	Time for CDC run on RTL		Time for Power Aware CDC on Netlist
		<i>Non-Power Aware CDC (Secs)</i>	<i>Power Aware CDC (Secs)</i>	<i>Synthesized Netlist (Hours)</i>
1.	Mod1	1861	2411	36 hrs
2.	Mod2	2713	3621	41 hrs

These results on the customer design highlight that power aware CDC verification at RTL is faster and more efficient for fixing bugs than delaying analysis to the gate level.

VI. SUMMARY AND FUTURE WORK

Presence of power intent along with the design in terms of a separate UPF design saves the designer from changing their RTL. But, since the power management logic required to model the power aware intent alters the design’s structure and functionality, power aware CDC verification is a must.

If CDC verification is delayed until after the gate-level design is synthesized, verification becomes very expensive. Each iteration of the CDC run, results-analysis and bug-fixing is more time consuming. The result is an exploding CDC verification time (as shown in Table 1). Hence, it is imperative to move Power Aware CDC verification earlier in the design cycle to the RTL development stage. Fortunately, the Questa CDC solution from Mentor Graphics Corporation has all of the sophisticated capabilities described in this paper.

Our Power Aware CDC methodology benefits designers the most if it is incorporated at the RTL level. But today’s designs invariably contain many IPs (both RTL and gate-level), which often have corresponding UPF information for them. Additional efforts and refinements are required to extend this methodology to handle all the various design configurations appearing in the verification of system-level designs.

In this paper, we focused our presentation and results on demonstrating the impact of isolation cells on CDC analysis of the design. But, the proposed methodology also applies to verifying the effects of other artifacts of UPF logic, such as retention cells, level shifters and so on. In the future, detailed feedback and studies will help clarify these impacts and help enhance the tools and methodologies to validate them.

VII. REFERENCES

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