



# Performance Evaluation of a Phase-Locked Loop using Variation-Aware Behavioral Models

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# Problem Statement

## AMS Verification:

Requires extensive simulation due to **p**rocess, **v**oltage, and **t**emperature (**PVT**) variations. Alternately, there is a substantial increase in number of process parameters – growth of ~20% every 4 to 5 yrs[1].

## Need:

Accurate, efficient propagation of circuit-level PVT variations in system analysis.

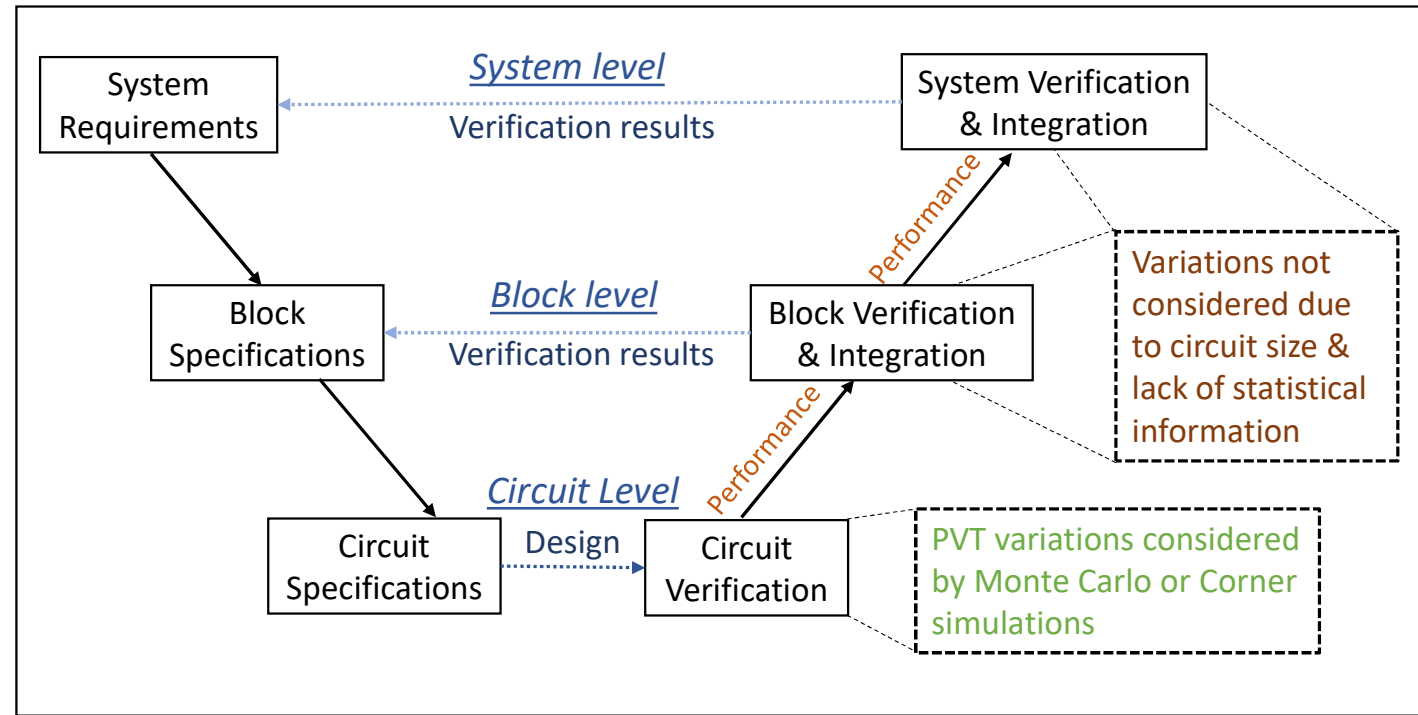


Fig: V-model for hardware development

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- Proposed Variation-Aware Behavioral Models (VABMs)
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# State-of-the-Art

## State-of-the-Art

Statistical behavioral modeling considering PVT variations:

### Polynomial-based approaches

- Response Surface Modeling (RSM) - Felt et al.[2], Filiol et al.[3]
- Random Polynomials - Lange et al.[4]
- Universal Kriging - Okobiah et al.[5]
  - + High model accuracy using quadratic models
  - + Parameter correlations using matrix( $N \times N$ )
  - Model complexity  $\sim O(N^2)$

### Learning-based approaches

- Correlated Bayesian Model Fusion (BMF) using Bayesian inference - Gao et al.[6], Alawieh et al.[7]
- Particle Swarm Optimization (PSO) - Garitselov et al.[8]
  - Increased fitting complexity and training cost
  - No capture of parameter correlations

### Linear model-based approaches

- Quasi-Sensitivity Analysis - Kuo et al.[9]
- Affine Kernel Approach - Zivkovic et al.[10]
  - + Accuracy comparable to RSM with reduced computational costs
  - + Correlation preserved by models; No need for correlation matrix

*Our behavioral models are constructed using Affine Kernel approach.*



# Variation-Aware Behavioral Models

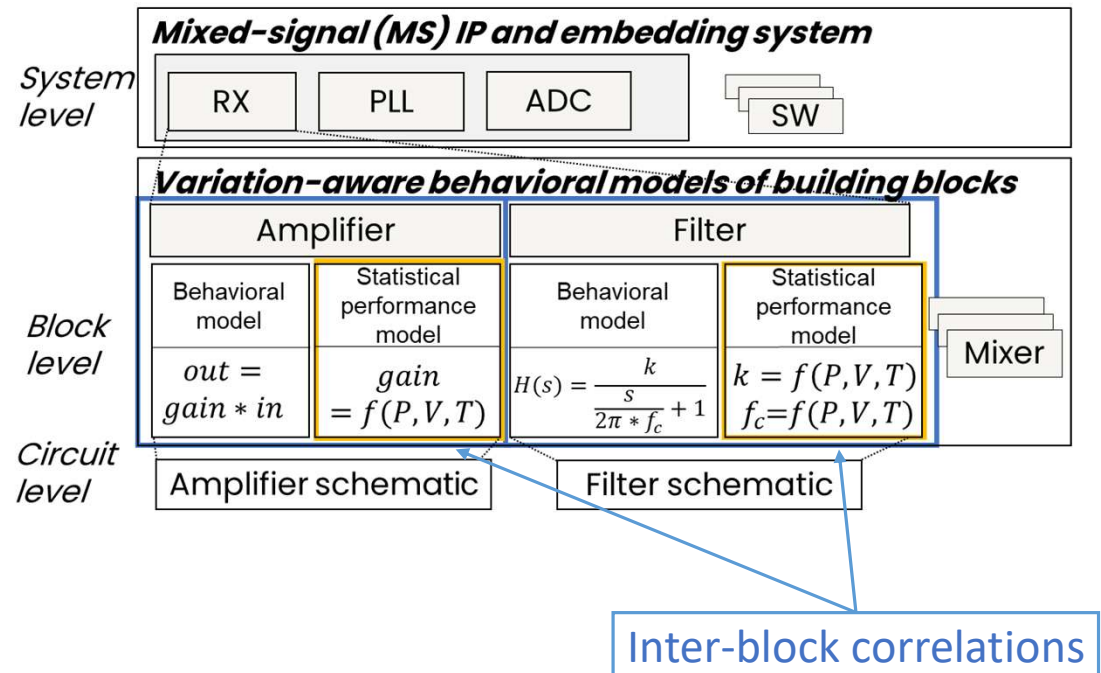
# Hierarchical Approach

## 1. Statistical Performance Models(SPM)

- ➔ Model circuit performances as a function of PVT variations

## 2. Variation-Aware Behavioral Models (VABM)

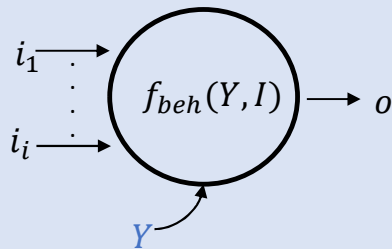
- ➔ Combine functional behavioral models with SPMs
- ➔ Account inter-block parameter correlations



# Variation-Aware Behavioral Model (VABM)

## FUNCTIONAL BEHAVIORAL MODEL

- Behavior defined as a function:  
 $f_{beh}: Inputs \rightarrow Outputs$
- Parameters ( $Y$ )  $\Leftrightarrow$  key performance metrics of the modelled circuit block



## (STATISTICAL) PERFORMANCE MODEL

- Model performance metrics as functions of P,V,T variations

$$y_j \sim f(P, V, T), \quad y_j \in Y$$

$$y_j \sim y_{nom} + \sum_{k=1}^n \delta_k s_k$$

$y_{nom}$  – nominal value of performance  $y_j$

$\delta_k$  – variation of  $k^{th}$  parameter

$s_k$  – sensitivity coefficient

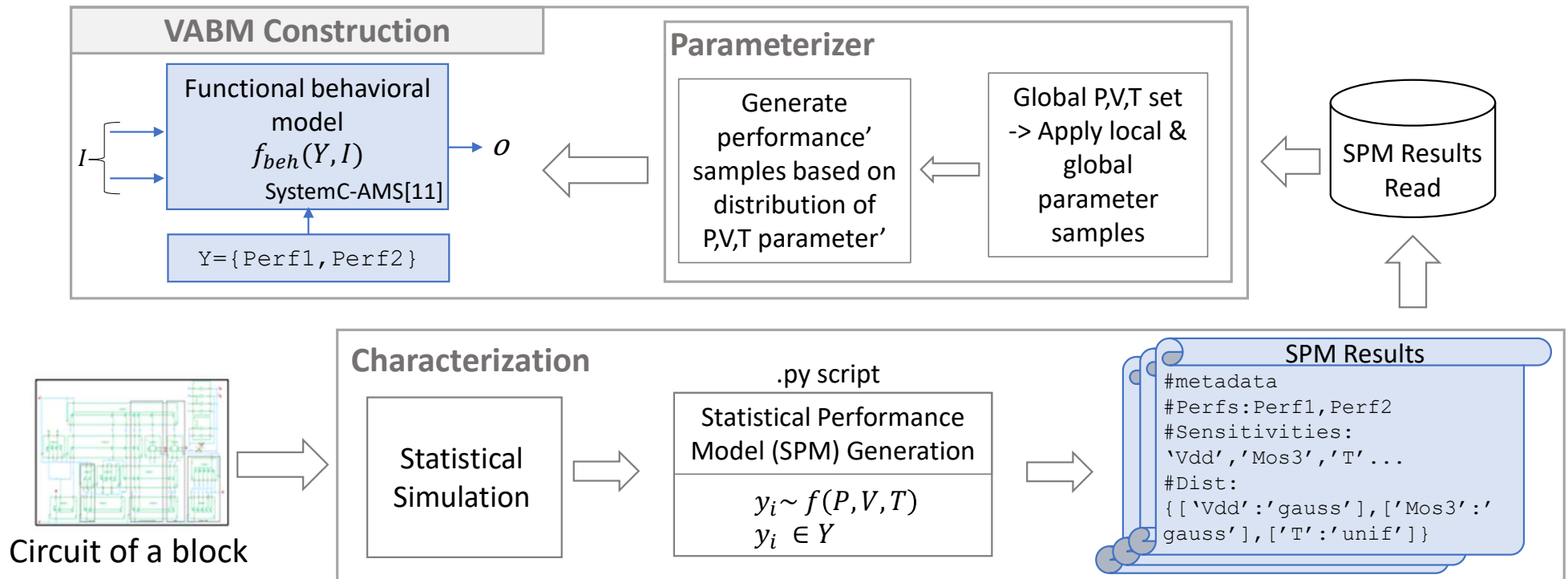
- Model generated from statistical simulation data



## VARIATION-AWARE BEHAVIORAL MODEL

- Parameters sampled based on distributions estimated by the model

# Hierarchical Framework: Bringing characterization data to behavioral block-level models

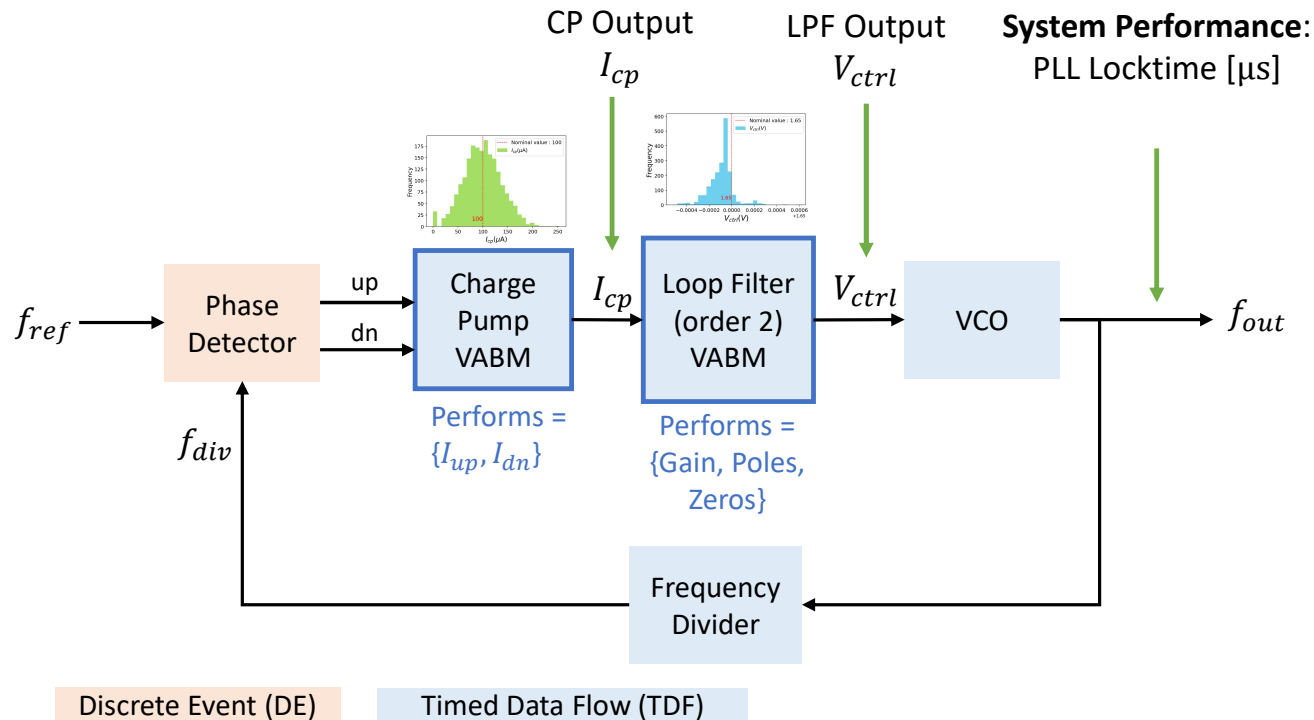


[11] "IEEE Standard for Standard SystemC(R) Analog/Mixed-Signal Extensions Language Reference Manual," Jan. 2016, doi: <https://doi.org/10.1109/ieeestd.2016.7448795>.



# Evaluation

# Phase-Locked Loop



VABMs act as plug & play models in hierarchical analysis.

VABMs takes care for inter-block correlations.

| Block Performance Metrics    | No. of PVT parameters |
|------------------------------|-----------------------|
| $I_{up}, I_{dn}$             | 35                    |
| <i>Gain, Poles, Zeros</i>    | 53                    |
| Shared variations CP and LPF | 23                    |

Fig: SystemC AMS model of a phase-locked loop[12]

[12] A. Dias, "Phase Locked Loop Simulator in SystemC-AMS," Américo Dias, Mar. 02, 2018. <https://americo.dias.pt/docs/technical/pll/>

# Model Accuracy: VABM vs Circuit Monte Carlo

| Feature                                            |                                                                                                     |
|----------------------------------------------------|-----------------------------------------------------------------------------------------------------|
| Monte Carlo Runs                                   | 2000                                                                                                |
| Probability Distribution Function (PDF) Comparison | Jenson Shannon Divergence (JSD)[13]                                                                 |
| Statistical Measures                               | Mean( $\mu$ ),<br>Standard Deviation( $\sigma$ ),<br>Skewness( $\gamma$ ),<br>Kurtosis( $\beta_2$ ) |
| Target Sigma                                       | $\pm 3\sigma$                                                                                       |

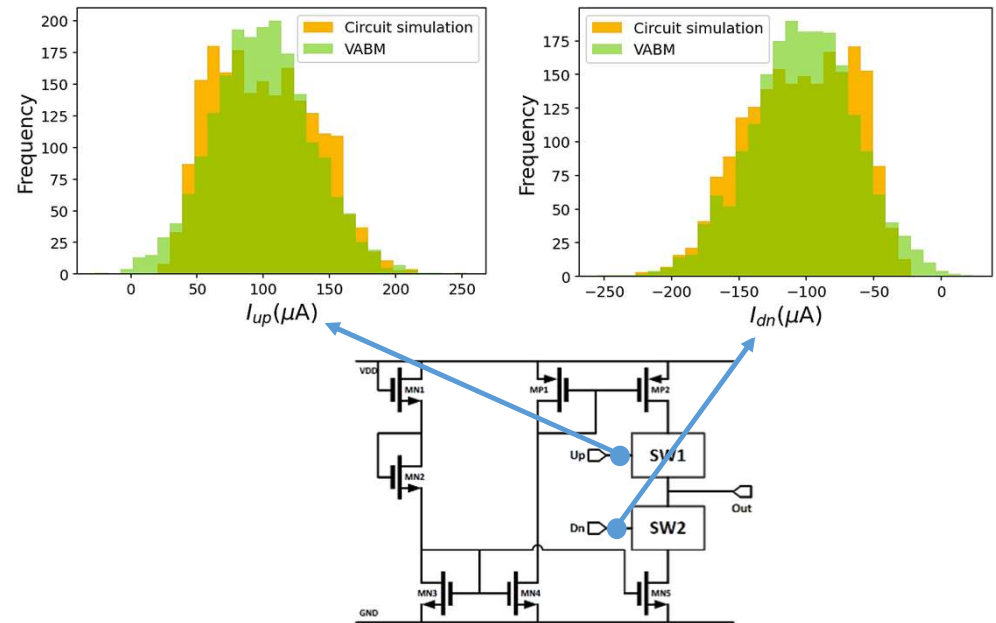


Fig: Example Charge Pump

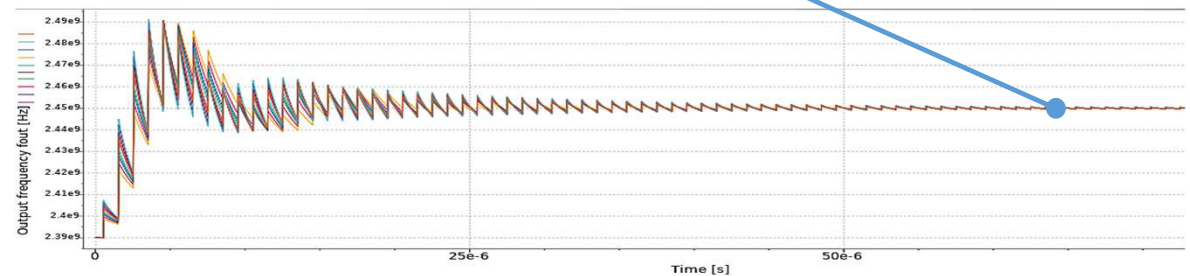
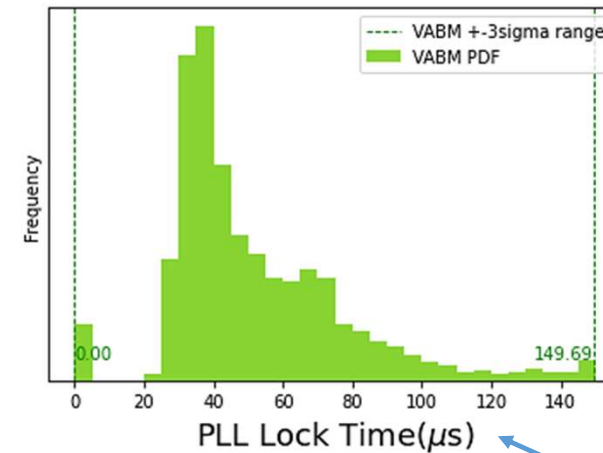


# System Analysis

# PLL System Performance using VABMs

- Performance metric: Lock time of PLL
- PDFs also highlight cases where PLL fails to lock (at 0 seconds)
- #Monte Carlo runs: 2000

| Simulation Metrics                      | Value                     |
|-----------------------------------------|---------------------------|
| Single run time                         | 0.76 [s]                  |
| Simulation overhead incl. Parameterizer | ~ 0.03 [s]                |
| Total wall clock time                   | 2000×0.76[s]<br>~ 25 mins |



Example: PLL output frequency for 10 Monte Carlo runs  
Model simulated for 200 [μs], Sampling rate 100 [ps]

## System Analysis: PLL

- Charge Pump Variation – PLL locally sensitive to CP
- Loop Filter Variation – Poor damping introduces harmonics in locking behaviour
- CP + LPF Combined Variation
  - Capture effect of inter-block correlations on PLL
  - Charge pump removes meta-stability

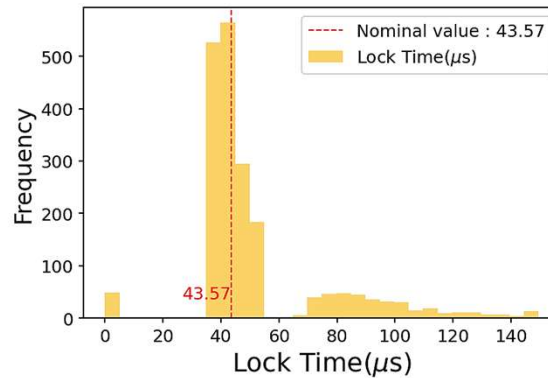


Fig: Charge pump variation effect

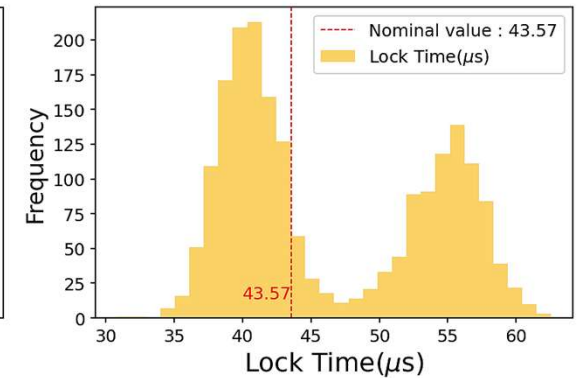


Fig: Loop filter variation effect

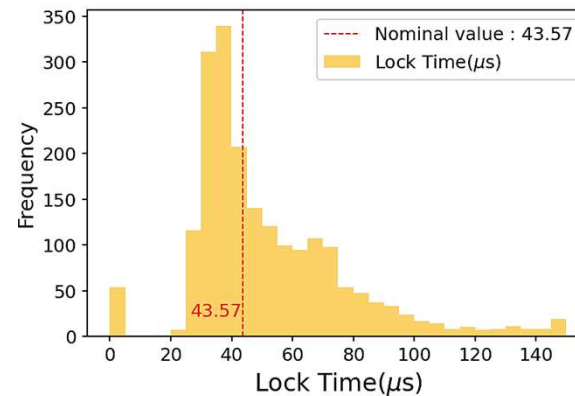


Fig: CP + LPF variation effect



# Comparison with other scenarios

# Gaussian Model

What if P,V,T variations and dependencies are not considered in system level?

Solution -> All block performance metrics are independent random variables.

## Scenario 1:

Gaussian model – Assume block performance metrics follow a normal distribution.

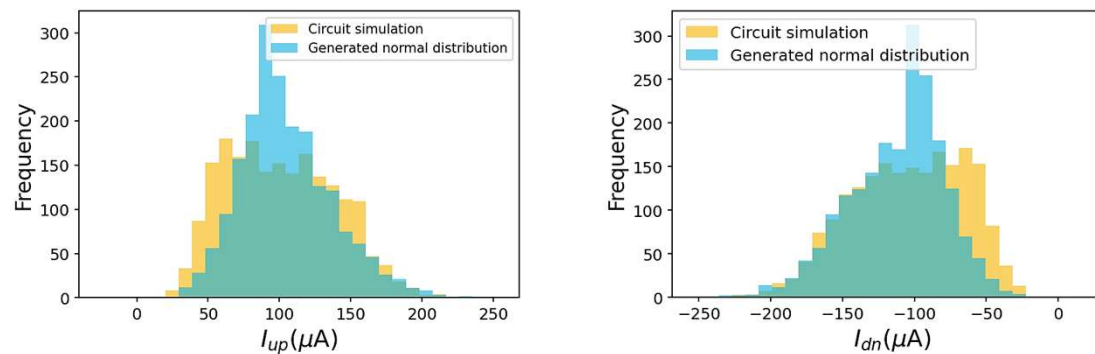


Fig: Probability distribution functions(PDFs) of charge pump currents – Gaussian model vs Circuit simulation

# Gaussian Model: Limitations

## Limitations:

- ☐ Assumes symmetric distribution
- ☐ No information on PVT data & inter-block correlations
- ☐ Estimated  $\pm 3\sigma$  ranges are narrow, potentially overlooking outlier behavior

# FMKL Generalized Lambda Distribution (FMKL GLD) model

**Scenario 2: FMKL Model:** Freimer, Mudholkar, Kollia, and Lontas [14]

- Circuit performance distributions modeled using FMKL GLD.
- Quantile function defined by inverse cumulative distribution [14,15]

$$F^{-1}(u) = \lambda_1 + \frac{\frac{u^{\lambda_3} - 1}{\lambda_3} - \frac{(1-u)^{\lambda_4} - 1}{\lambda_4}}{\lambda_2}$$

where  $0 < u < 1$

*Parameters:*

$\lambda_1$  – location

$\lambda_2$  – scale

$\lambda_3, \lambda_4$  – shape

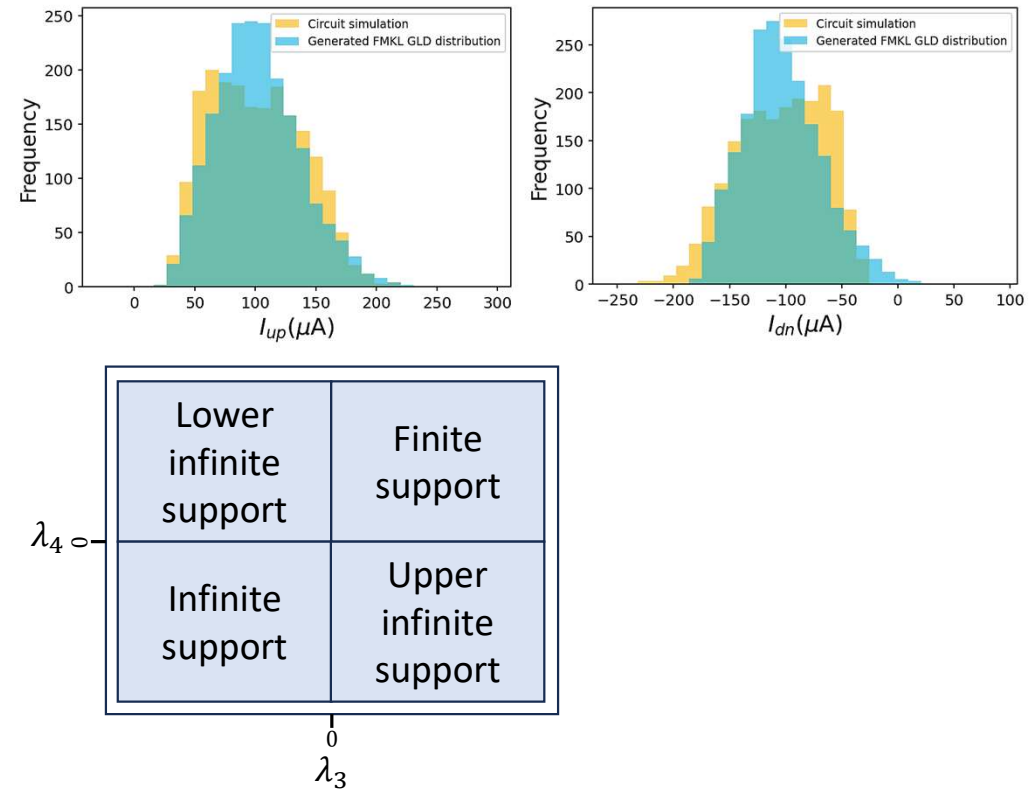
[14] A. Lange, I. Harasymiv, O. Eisenberger, F. Roger, J. Haase, and R. Minixhofer, “Towards probabilistic analog behavioral modeling,” in 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal: IEEE, May 2015, pp. 2728–2731, ISBN: 978-1-4799-8391-9. DOI: 10 . 1109 /ISCAS.2015.7169250.

[15] Z. A. Karian and E. J. Dudewicz, “Fitting the generalized lambda distribution to data: A method based on percentiles,” Communications in Statistics - Simulation and Computation, vol. 28, no. 3, pp. 793–819, 1999. DOI: 10 . 1080 /03610919908813579. eprint: <https://doi.org/10.1080/03610919908813579>.

# FMKL GLD Model: Limitations

## Limitations:

- ❑ No information on PVT data & inter-block correlations
- ❑ Limited support for  $0 \leq \lambda_3$ ,  $\lambda_4$  [16]
- ❑ No closed-form for PDF; values derived from the quantile function



[16] Y. Chalabi, D. J. Scott, and D. Wuertz, "Flexible distribution modeling with the generalized lambda distribution," 2012.

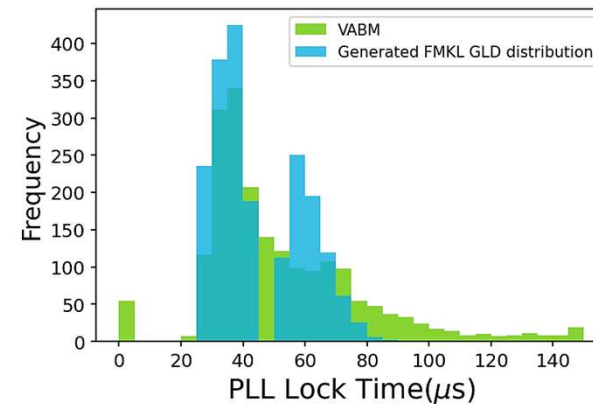
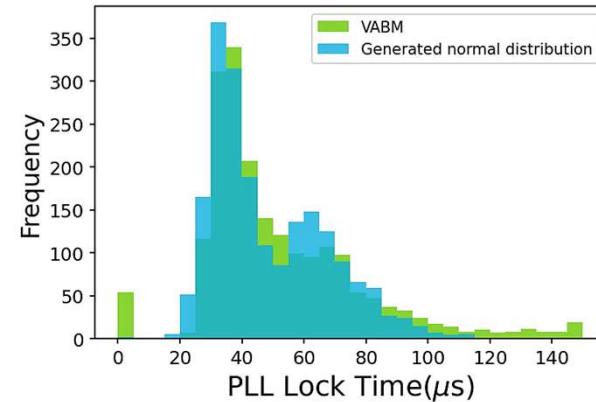
Fig: FMKL GLD Support Region [16]

## Effect of inter-block correlation

- Lower variances in PLL spread for FMKL GLD and Gaussian model.
- VABM spread similar to Gaussian model but also accounts effect of inter-block correlations.

| Performance         | Metrics             | VABM          | Gaussian Model | FMKL GLD<br>-based model |
|---------------------|---------------------|---------------|----------------|--------------------------|
| Locktime [ $\mu$ s] | Mean                | 44.35         | 41.55          | 39.50                    |
|                     | Std. Dev.           | 22.29         | 21.40          | 18.54                    |
|                     | Skewness            | 1.28          | 0.91           | 0.59                     |
|                     | Kurtosis            | 3.22          | 2.32           | 1.88                     |
|                     | JSD                 | -             | 0.0438         | 0.0433                   |
|                     | $\pm 3\sigma$ range | [0.00,149.69] | [17.60,121.62] | [25.55,86.63]            |

Fig: Comparison of system performance metrics using all approaches





# Summary

# Summary

- A scalable hierarchical methodology for propagating process variations to system-level simulations using VABMs
- Effectively account for inter-block parameter correlations
- Effectively capture circuit behavior while aligning boundaries of the distribution
- Accelerate simulation speedup with minimal computational overhead

# Outlook

- System analysis using improved SPM (employing piecewise linear models) over linear affine kernel.
- Explore significance of number of P,V,T parameters on system performance.
- Evaluate system performance using hierarchical regression analysis.
- Explore advanced statistical sampling techniques to observe tail behavior.



# Thank you! Questions?

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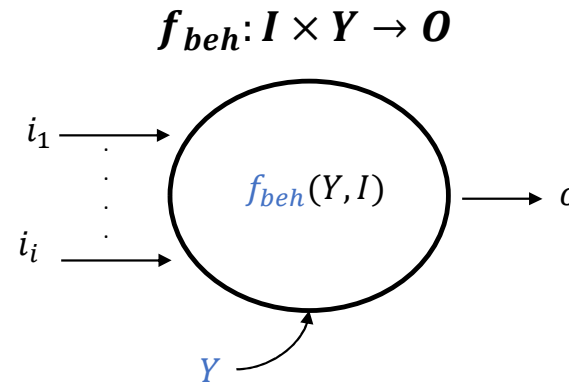


## State-of-the-art references

- [2] E. Felt, S. Zanella, C. Guardiani, and A. Sangiovanni-Vincentelli, "Hierarchical statistical characterization of mixed-signal circuits using behavioral modeling," in Proceedings of International Conference on Computer Aided Design, Nov.1996, pp. 374–380. DOI: 10.1109/ICCAD.1996.569824
- [3] H. Filiol, I. O'Connor, and D. Morche, "A new approach for variability analysis of analog ICs," in Proc. 2009 Joint IEEE North-East Workshop on Circuits and Systems and TAISA Conference (NEWCAS-TAISA), 2009. DOI: 10.1109/NEWCAS.2009.5290422.
- [4] A. Lange, I. Harasymiv, O. Eisenberger, F. Roger, J. Haase, and R. Minixhofer, 'Towards probabilistic analog behavioral modeling', in 2015 IEEE International Symposium on Circuits and Systems (ISCAS), 2015, pp. 2728–2731.
- [5] O. Okobiah, S. P. Mohanty, and E. Kougianos, "Fast statistical process variation analysis using universal kriging metamodeling: A pll example," in 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), 2013, pp. 277–280. DOI: 10.1109/MWSCAS.2013.6674639
- [6] Z. Gao, F. Wang, J. Tao, Y. Su, X. Zeng, and X. Li, "Correlated bayesian model fusion: Efficient high-dimensional performance modeling of analog/RF integrated circuits over multiple corners," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 42, no. 2, pp. 360–370, Feb. 2023, ISSN: 1937-4151. DOI: 10.1109/TCAD.2022.3174170.
- [7] M. B. Alawieh, F. Wang, and X. Li, "Efficient hierarchical performance modeling for analog and mixed-signal circuits via bayesian co-learning," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 12, pp. 2986–2998, Dec. 2018, ISSN: 1937-4151. DOI:10.1109/TCAD.2018.2789778
- [8] O. Garitselov, S. P. Mohanty, E. Kougianos, and G. Zheng, "Particle swarm optimization over non-polynomial metamodels for fast process variation resilient design of nano-cmos PLL," in Great Lakes Symposium on VLSI, Salt Lake City, UT, USA, ACM, 2012, pp. 255–258. DOI: 10.1145/2206781.2206843
- [9] C.-C. Kuo, M.-J. Lee, C.-N. Liu, and C.-J. Huang, 'Fast Statistical Analysis of Process Variation Effects Using Accurate PLL Behavioral Models', IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, no. 6, pp. 1160–1172, Jun. 2009
- [10] C. Zivkovic, J. Roedel, N. Chavan, F. Rethmeier, and C. Grimm, 'Variation-Aware Performance Verification of Analog Mixed-Signal Systems', in DVCon Europe 2023; Design and Verification Conference and Exhibition Europe, 2023, pp. 7–13.

# Proposed VABM

- Our proposed VABMs are defined based on the concept of parameter adaptive models[2].
- The functional process ( $f_{beh}$ ) represents functional behavior
- (Y) enables functional adaptivity using Affine kernel[3]



**where**

$I = \{i_1, i_2, \dots, i_i\}$ ;  $I$  is set of input signals

$o \in O$ , where  $O$  is a set of output signals

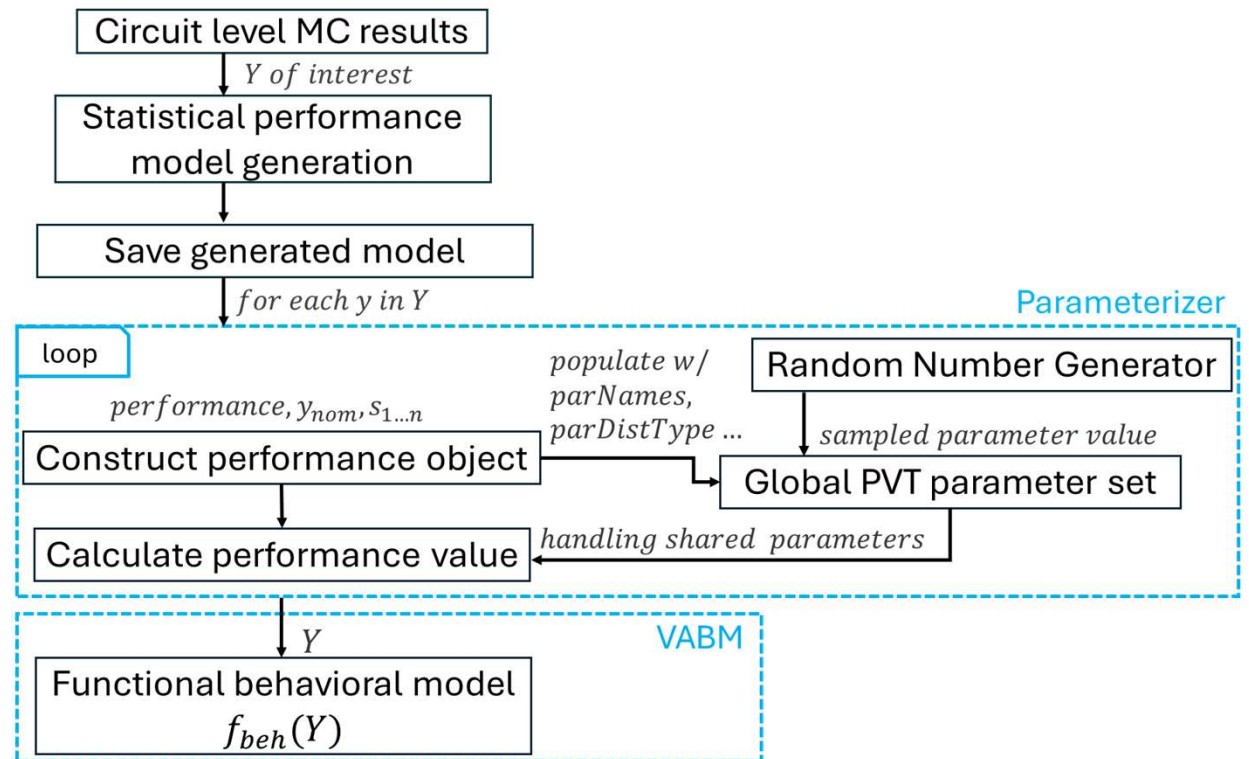
$Y = \{y_j | y_j \in \mathbb{R}, 1 \leq j \leq m\}$ ;  $m$  are performance metrics

[2] I. Sander and A. Jantsch, "Modelling adaptive systems in ForSyDe," Electronic Notes in Theoretical Computer Science, Proceedings of the First Workshop on Verification of Adaptive Systems (VerAS 2007), vol. 200, no. 2, pp. 39–54, Feb. 29, 2008, ISSN: 1571-0661. DOI: 10.1016/j.entcs.2008.02.011

[3] C. Zivkovic, J. Roedel, N. Chavan, F. Rethmeier, and C. Grimm, "Variation-aware performance verification of analog mixed-signal systems," in DVCon Europe 2023; Design and Verification Conference and Exhibition Europe, Nov. 2023, pp. 7–13.

## Hierarchical Framework

1. Read statistical performance model results onto performance objects
2. Inject all parameters in a global PVT set – ensures consistency of sampled value for all VABMs
3. Apply local sensitivity and calculate performance values
4. Feed the calculated performance to functional behavioral blocks



# Data Format (.par)

## Metadata

```
//////////////////// Metadata //////////////////////  
// folder: /home/.../simulation/ChargePump  
//2024-08-02 13:13:32.289737  
  
//k_cluster: 1  
//tau_relevant: 0.01  
//tau_lin: 1e-28  
//#MC samples: 2000
```

## Performance data

```
//////////////////// Performances //////////////////////  
moduleName = "cp"  
cp_performances = {"i_up_p", 0.000101167012965}, {"i_dn_p", -0.00010442588830000001})  
  
sens_i_up_p = {"Vsupply_unif_1", 3.4996726827876146e-05}, {"r1_io",  
1.0396822042038212e-05}, {"r19_io", 3.945994105012961e-06}, ...}  
error_mean_i_up_p = -4.724115689876391e-10  
error_stddev_i_up_p = 9.192259238706476e-06  
  
sens_i_dn_p = {"Vsupply_unif_1", -3.574452437801205e-05}, {"r1_io",  
-1.1692098714331887e-05}, {"r2_io", 5.025710131731148e-06}, {"r19_io", -4.510244056577494e-06}, ...}  
error_mean_i_dn_p = 4.630224785094836e-10  
error_stddev_i_dn_p = 9.528540473351679e-06
```

## Parameters data

```
//////////////////// Parameters //////////////////////  
parNames = {"Vsupply_unif_1", "r1_io", "r19_io", "r2_io", ...}  
parMeans = {0.0, ...}  
parDistType = {"gauss", ...}  
parStdDev = {1.0, ...}  
parZscore = {10.0, ...}
```

## Results – Charge Pump and Loop Filter VABM

| Performance metric                         | Statistical measures | Circuit-level Monte Carlo | VABM            | Gaussian Model   | FMKL GLD-based model |
|--------------------------------------------|----------------------|---------------------------|-----------------|------------------|----------------------|
| CP $I_{up}$ [ $\mu\text{A}$ ]              | Mean                 | 99.25                     | 98.90           | 99.69            | 99.61                |
|                                            | Std. Dev.            | 44.9                      | 36.79           | 29.23            | 34.08                |
|                                            | Skewness             | 0.27                      | 0.11            | 0.63             | 0.51                 |
|                                            | Kurtosis             | 2.22                      | 2.94            | 3.21             | 2.94                 |
|                                            | JSD                  | -                         | 0.0551          | 0.0433           | 0.0466               |
|                                            | $\pm 3\sigma$ range  | [28.00,210.26]            | [-2.51,216.89]  | [32.02,228.50]   | [27.77,220.99]       |
| CP $I_{dn}$ [ $\mu\text{A}$ ]              | Mean                 | -101.89                   | -102.09         | -105.29          | -105.99              |
|                                            | Std. Dev.            | 46.18                     | 38.23           | 32.53            | 34.08                |
|                                            | Skewness             | -0.28                     | -0.11           | -0.48            | 0.51                 |
|                                            | Kurtosis             | 2.24                      | 2.96            | 2.87             | 2.94                 |
|                                            | JSD                  | -                         | 0.0548          | 0.0425           | 0.0508               |
|                                            | $\pm 3\sigma$ range  | [-219.23,-27.74]          | [-227.52,5.11]  | [-222.78,-29.95] | [-177.83,15.39]      |
| LF Linear Gain [ $\times 10^9$ ]           | Mean                 | 48.74                     | 48.49           | 49.12            | 48.89                |
|                                            | Std. Dev.            | 5.83                      | 4.10            | 7.25             | 6.87                 |
|                                            | Skewness             | 0.53                      | -0.02           | 0.64             | 0.47                 |
|                                            | Kurtosis             | 2.97                      | 2.86            | 2.94             | 2.96                 |
|                                            | JSD                  | -                         | 0.0039          | 0.0066           | 0.0064               |
|                                            | $\pm 3\sigma$ range  | [35.09,71.57]             | [32.10,70.13]   | [33.66,76.41]    | [33.89,73.19]        |
| LF P1 [ $\times 10^3 \text{ rad s}^{-1}$ ] | Mean                 | 525.77                    | 521.16          | 536.86           | 528.28               |
|                                            | Std. Dev.            | 75.13                     | 74.14           | 106.07           | 68.71                |
|                                            | Skewness             | 0.50                      | 0.07            | 0.67             | 0.47                 |
|                                            | Kurtosis             | 2.95                      | 2.90            | 2.89             | 2.96                 |
|                                            | JSD                  | -                         | 0.0072          | 0.0097           | 0.007                |
|                                            | $\pm 3\sigma$ range  | [348.48,794.42]           | [315.56,782.88] | [317.09,936.14]  | [378.22,771.29]      |
| LF Z1 [ $\times 10^3 \text{ rad s}^{-1}$ ] | Mean                 | 75.32                     | 75.81           | 75.82            | 75.70                |
|                                            | Std. Dev.            | 5.20                      | 6.02            | 7.17             | 6.11                 |
|                                            | Skewness             | 0.5                       | -0.03           | 0.82             | 0.65                 |
|                                            | Kurtosis             | 2.94                      | 2.74            | 2.99             | 2.62                 |
|                                            | JSD                  | -                         | 0.0059          | 0.0097           | 0.002                |
|                                            | $\pm 3\sigma$ range  | [63.04,93.91]             | [38.70,112.85]  | [61.40,107.92]   | [67.23,95.40]        |

## Benchmarks – Response Surface Modeling vs Quasi Sensitivity Analysis

|                                  |          | HSPICE<br>MCS | Our proposed PLL<br>behavioral model                                 |          | Top-down PLL<br>behavioral model |          |
|----------------------------------|----------|---------------|----------------------------------------------------------------------|----------|----------------------------------|----------|
|                                  |          |               | Using 1 <sup>st</sup> RSM for behavioral parameters                  |          |                                  |          |
|                                  |          | Value         | Value                                                                | err. (%) | Value                            | err. (%) |
| V <sub>lock</sub> (V)            | Mean     | 0.9941        | 0.9931                                                               | -0.1     | 0.9254                           | -6.9     |
|                                  | St. Dev. | 0.0343        | 0.0365                                                               | 6.4      | 0.0384                           | 12.0     |
| T <sub>lock</sub> (us)           | Mean     | 3.3743        | 3.4489                                                               | 2.2      | 3.1641                           | -6.2     |
|                                  | St. Dev. | 0.5764        | 0.5729                                                               | -0.6     | 0.5447                           | -5.5     |
| pk-pk Jitter<br>@ 800MHz<br>(ps) | Mean     | 13.2          | 12.2                                                                 | -7.6     | 8.0                              | -39.4    |
|                                  | St. Dev. | 1.40          | 1.36                                                                 | -2.9     | 4.61                             | 229.3    |
|                                  | Worst    | 17.0          | 16.6                                                                 | -2.4     | 18.2                             | 7.1      |
| T <sub>extraction</sub> (hours)  |          | N/A           | 4(n+1) × 1.71 = 34.2 , n = 4<br>(n: # of device parameter variation) |          |                                  |          |
| T <sub>simulation</sub> (hours)  |          | 598.54        | 2.95                                                                 |          | 2.10                             |          |

|                                  |          | HSPICE<br>MCS | Our Quasi-SA<br>+BMCS                                                                |             | Trad. SA<br>+BMCS |          |
|----------------------------------|----------|---------------|--------------------------------------------------------------------------------------|-------------|-------------------|----------|
|                                  |          |               | Using our proposed accurate PLL model                                                |             |                   |          |
|                                  |          | Value         | Value                                                                                | err. (%)    | Value             | err. (%) |
| $V_{\text{lock}}$ (V)            | Mean     | 0.9941        | <b>0.9947</b>                                                                        | <b>0.1</b>  | 0.9934            | -0.1     |
|                                  | St. Dev. | 0.0343        | <b>0.0349</b>                                                                        | <b>1.7</b>  | 0.0453            | 32.1     |
| $T_{\text{lock}}$ (us)           | Mean     | 3.3743        | <b>3.4383</b>                                                                        | <b>1.9</b>  | 3.4409            | 2.0      |
|                                  | St. Dev. | 0.5764        | <b>0.5717</b>                                                                        | <b>-0.8</b> | 0.5406            | -6.2     |
| pk-pk Jitter<br>@ 800MHz<br>(ps) | Mean     | 13.2          | <b>12.4</b>                                                                          | <b>-6.1</b> | 12.4              | -6.1     |
|                                  | St. Dev. | 1.40          | <b>1.41</b>                                                                          | <b>0.7</b>  | 2.29              | 63.6     |
|                                  | Worst    | 17.0          | <b>16.7</b>                                                                          | <b>-1.8</b> | 16.4              | -3.5     |
| $T_{\text{extraction}}$ (hours)  |          | N/A           | $(n+1) \times 1.71 = 8.55, n = 4$<br>$(n: \# \text{ of device parameter variation})$ |             |                   |          |
| $T_{\text{simulation}}$ (hours)  |          | 598.54        | <b>3.50</b>                                                                          |             | 2.93              |          |

C.-C. Kuo, M.-J. Lee, C.-N. Liu, and C.-J. Huang, "Fast Statistical Analysis of Process Variation Effects Using Accurate PLL Behavioral Models," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 6, pp. 1160–1172, Jun. 2009, doi: [10.1109/TCSI.2008.2008502](https://doi.org/10.1109/TCSI.2008.2008502).

## Benchmarks – Learning-based approaches

- Correlated Bayesian Model Fusion (C-BMF) – Case study Operational Amplifier

|                          |                |
|--------------------------|----------------|
| Number of PVT parameters | 1184 P + 36 VT |
| Training cost            | 540 samples    |
| Simulation cost          | 1.05 Hours     |
| Fitting cost             | 20 Mins        |

- Particle Swarm Optimisation (PSO) – Case study PLL

|                          |                         |
|--------------------------|-------------------------|
| Number of PVT parameters | 35                      |
| Training cost            | 200 Monte Carlo Samples |
| Circuit Monte Carlo      | 1000 runs over 5 days   |

[1] Z. Gao, F. Wang, J. Tao, Y. Su, X. Zeng, and X. Li, "Correlated bayesian model fusion: Efficient high-dimensional performance modeling of analog/RF integrated circuits over multiple corners," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 42, no. 2, pp. 360–370, Feb. 2023, ISSN: 1937-4151. DOI: 10.1109/TCAD.2022.3174170.

[2] O. Garitselov, S. P. Mohanty, E. Kougianos, and G. Zheng, "Particle swarm optimization over non-polynomial metamodels for fast process variation resilient design of nano-cmos PLL," in Great Lakes Symposium on VLSI, Salt Lake City, UT, USA, ACM, 2012, pp. 255–258. DOI: 10.1145/2206781.2206843

## Jensen-Shannon Divergence (JSD)

KL is the Kullback-Leibler divergence or 'relative entropy'

$$KL(P \parallel Q) = \sum_i P(i) * \log_2 \left( \frac{P(i)}{Q(i)} \right)$$

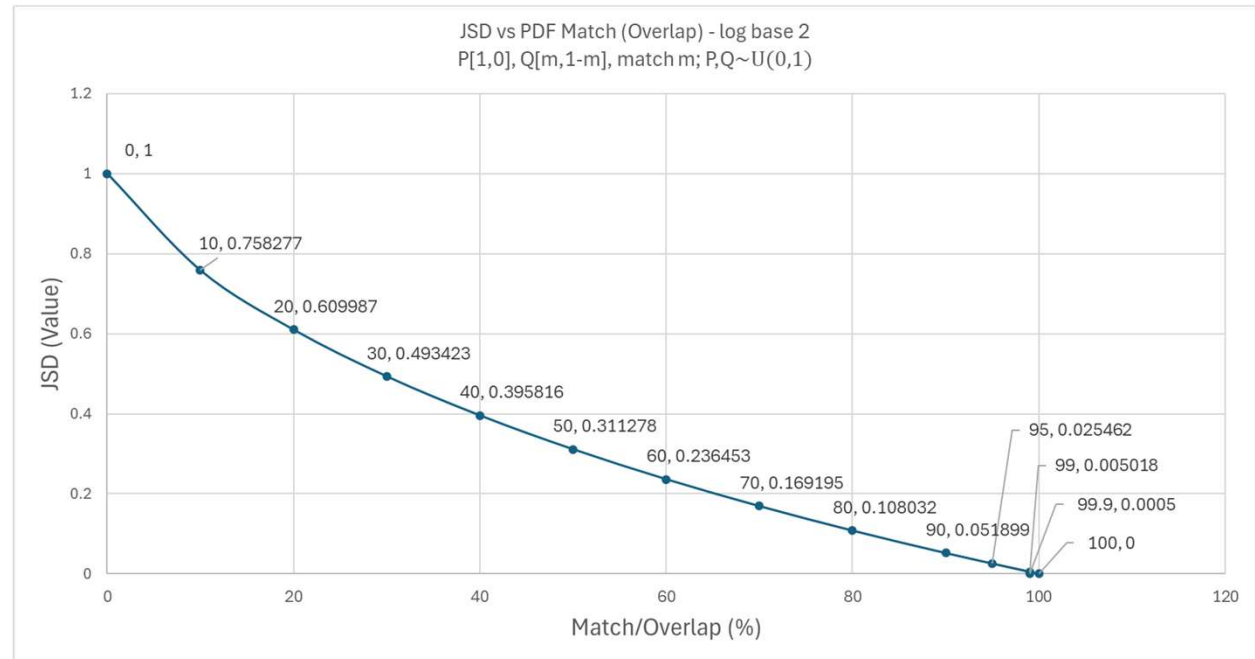
$$KL(P \parallel Q) = 0 \text{ (P identical to Q)}$$

$$KL(P \parallel Q) \neq KL(Q \parallel P)$$

JS divergence between two PDFs P and Q

$$JSD(P \parallel Q) = \frac{1}{2} KL(P \parallel M) + \frac{1}{2} KL(Q \parallel M)$$
$$M = (P+Q) / 2$$

JSD [0,1], for log base = 2



## Jensen-Shannon Divergence

### Example: For disjoint distribution

Consider probability distribution functions(PDFs) of P and Q, where

$$P(X = x) = \frac{P(\text{number of occurrences of } x)}{\text{Total number of elements}}$$

$$P = [1, 0, 0]$$

$$Q = [0, 0, 1]$$

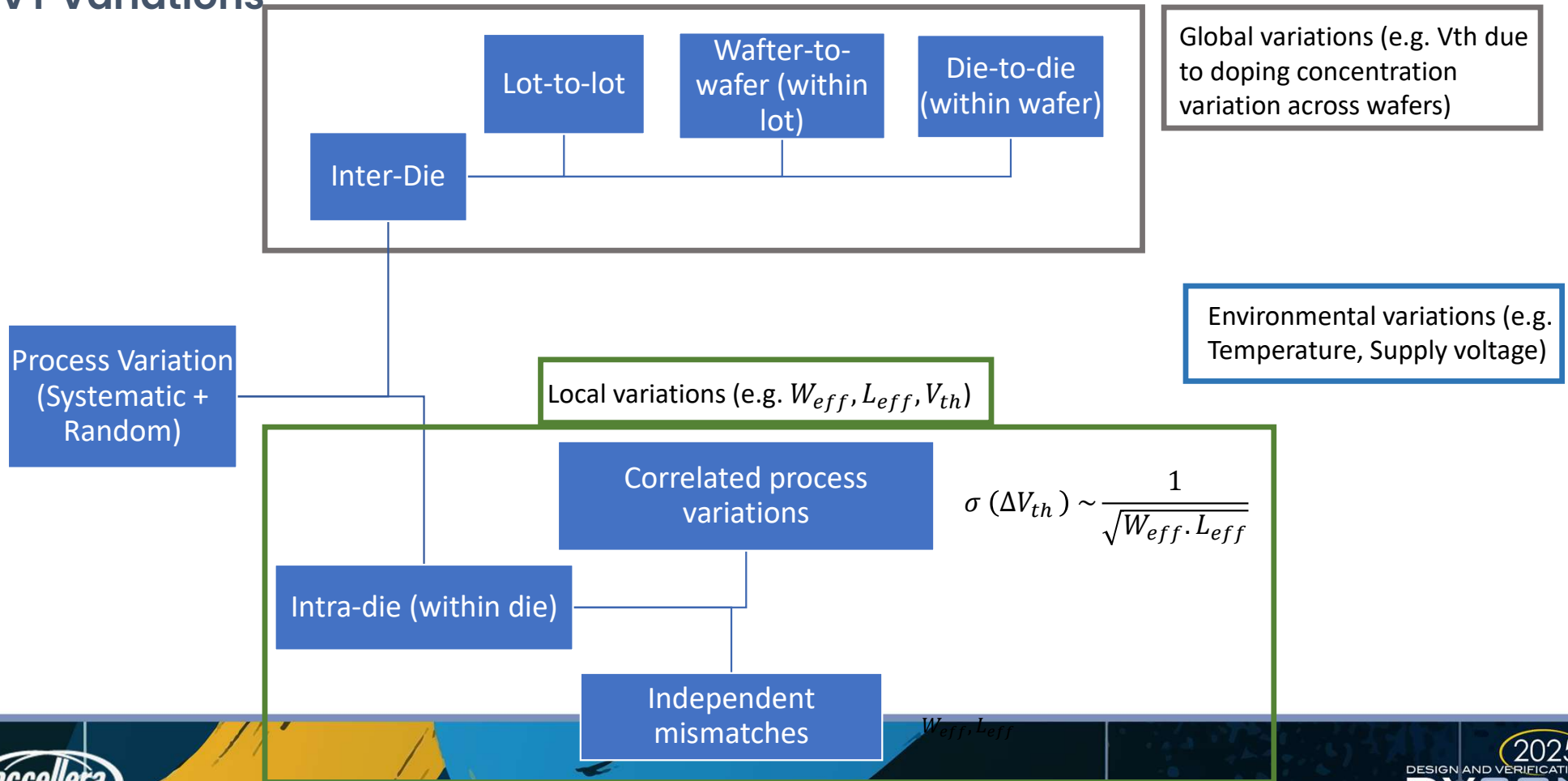
$$\text{then } M = \frac{1}{2}(P + Q) = \frac{1}{2}([1, 0, 0] + [0, 0, 1]) = [0.5, 0, 0.5]$$

$$\frac{1}{2} \text{KL}(P||M) = \frac{1}{2} \left[ 1 \log \left( \frac{1}{0.5} \right) + 0 \log \left( \frac{0}{0} \right) + 0 \log \left( \frac{0}{0.5} \right) \right] = \frac{1}{2} \log_2 2$$

$$\frac{1}{2} \text{KL}(Q||M) = 0 + 0 + \frac{1}{2} \left[ 1 \log \left( \frac{1}{0.5} \right) \right] = \frac{1}{2} \log_2 2$$

$$\text{JSD}(P||Q) = \frac{1}{2} \text{KL}(P||M) + \frac{1}{2} \text{KL}(Q||M) = 1$$

## PVT Variations



# Functional Behavioral Modeling

Analog behavioral models are typically constructed using hardware description languages (HDLs), such as SystemC-AMS and Verilog-AMS.

- Use of equation-based approaches to model circuit behavior
- significantly faster simulation compared to SPICE
- may lack accuracy because of various simplifications
- application-specific, significant efforts required for adaptation

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[4] G. Stehr, M. Pronath, F. Schenkel, H. Graeb, and K. Antreich, 'Initial sizing of analog integrated circuits by centering within topology-given implicit specifications', in ICCAD-2003. International Conference on Computer Aided Design (IEEE Cat. No.03CH37486), 2003, pp. 241–246

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