Design and Verification of the PLL using the new DCO and Its Applications to Built-In Speed Grading of Arithmetic Circuits.

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Abstract*—The Digitally Controlled Oscillator (DCO) is a key component in a cell-based Phase-Locked Loop (PLL) for on-chip high-speed clock generation. In this work, we design a cell-based DCO to achieve a more linear DCO period profile with a consistently small resolution of just 1ps. This DCO is embedded into an in-house PLL to evaluate its impact on the output clock period jitter. For verification, a mixed-level simulation method is applied to speed up the process, in which the data-path of the PLL is modeled in the transistor level while the controller in the RTL. Post-layout simulation results reveal that our DCO can achieve a resolution in the range of [0.62ps, 1.25ps] for all 5 process corners in the most extreme temperature range from -40˚C to 150˚C. At the same time, peak-to-peak jitter of our PLL over 2000 clock cycles after locking is reduced from the original 10.86ps to 6.07ps, with a reduction ratio of (10.86-6.07)/10.86 = 44%. Last, but not the least, we show the results of using our PLL to perform online speed grading for arithmetic circuits.*

***Index Terms*—**cell-based design, PLL, DCO, Varactor, step resolution, Built-In Speed Grading

I. INTRODUCTION

Built-In Speed Grading (BISG) has been applied to find out the maximum operation speed (F_{max}) of the circuit under test. All-digital cell-based Phase-Locked Loops (PLLs) have been used in the application of on-chip clock generation in BISG progress in [1]-[12]. Due to its regular architecture, process migration of this type of PLL is often much easier than its analog/mixed-signal counterparts. The basic architecture of All-digital cell-based PLL is shown in **Fig. 1**. It is constructed by a Phase Detector, Controller, Digitally Controlled Oscillator (DCO), and Frequency Divider. The Phase Detector compared the phase between reference clock and the output signal of Frequency Divider, and the Controller will adjust the control code to DCO according to the comparison result, Lead/Lag signal. The output frequency of DCO go through the Frequency Divider to compare with reference clock to complete the loop. Thus, the DCO determine the supporting clock frequency range and the peak-to-peak jitter of PLL at most.

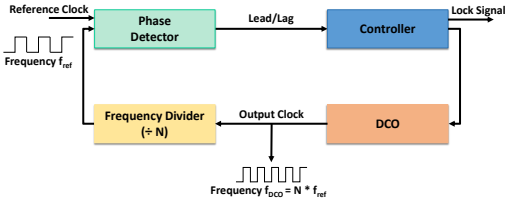


Fig. 1: Basic All-digital cell-based Phase-Locked Loop (PLL).

The rest of this paper is organized as follows. Section 2 introduces the design of the new DCO. Section 3 verification methodology and simulation result of the PLL with the new DCO and BISG. Section 4 concludes.

II. DESIGN OF THE NEW DCO

We design a new DCO which is shown in **Fig. 2**. This DCO consists of only 3 logic gates – the start-up gate and two buffer gates. All of them are varactor loaded. The coarse-tuning β-code controls the *latch-based varactor cells* at the outputs of the two buffer gates, while the fine-tuning γ-code controls the *NAND-based varactor cells* at the output of the start-up gate. In comparison, a NAND-based varactor cell provides a smaller amount of loading effect when turned on. On the other hand, a latch-based varactor cell provides a larger and more flexible loading effect.

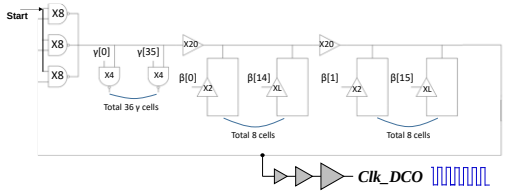


Fig. 2: New DCO architecture.

The amount of change in delay when turning on a latch-based varactor cell depends on the **driver-to-varactor size ratio**. For example, when a driver of X4 is loaded by an X1-sized latch-based varactor, the tuning effect is small. However, if we increase the driver strength to X20, then the tuning effect becomes smaller. In this work, **progressively sized latch-based varactor cells** has been designed. The comparison between same sized and progressively sized varactor cells is shown in **Fig. 3**. **Fig. 3(a)** is DCO Period Profile comparison between the the same sized XL and **progressively sized** {X2, X2, X1, X1, XL, XL, XL, XL}, and **Fig. 3(b)** is DCO Period Profile comparison between the the same sized X1 and **progressively sized**. The key characteristics are listed in **Table 1**. It shows that the **progressively sized one** can get a more linear DCO period profile while support a wider period range.

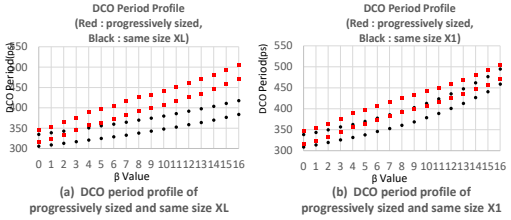


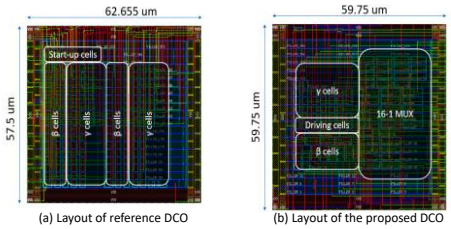
Fig. 3: DCO Period profile of of progressively sized and same size.

Table 1: Characteristics of the progressively sized and same size

DCO Characteristic Table	Same Size XL	Same Size X1	Progressive
DCO Period Range (ps)	306 ~ 408	309 ~ 495	316 ~ 506
β Segment Size Range (ps)	29 ~ 34	30 ~ 36	30 ~ 35
β-Segment Overlap Ratio (%)	79.4 ~ 89.7	50 ~ 83.3	61.3 ~ 74.2

Table 1: Characteristics of the progressively sized and same size

The layouts of the reference DCO and the proposed DCO using a 90nm CMOS process are shown in **Fig. 4**. For the new version, we have added a path-selection part controlled by the α-code so that the period can be extended.



(a) Layout of reference DCO (b) Layout of the proposed DCO

Fig. 4: The layout of two versions of DCOs using a 90nm CMOS process.

The verification flow chart is shown in **Fig. 5**. We use the EDA tool, VCS-XA, developed by Synopsys Inc. to simulation the DCOs, and perl scripts to analyze the characteristics of the DCO. The key characteristics of the two DCOs are listed in **Table 2**. Our new version excels in particularly two metrics: the β-segment size and the resolution. Originally, the β-segment size is [45ps, 252ps]. Now it becomes more uniform as [29ps, 32ps]. Originally, the resolution is [0.52ps, **3.85ps**]. Now it becomes more uniform as [0.79ps, **0.96ps**]. Based on this post-layout simulation results in the typical environment, the most significant advantage of this proposed DCO over the reference one is the *reduction of the worst-case resolution from 3.85ps down to 0.96ps.* Furthermore, the both DNL and INL is significantly smaller than reference one. It shows that the new DCO is much more linear than the reference one.

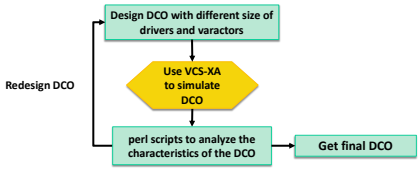


Fig. 5: The verification flow chart of DCO

Table 2: Characteristics of the proposed DCO based on post-layout simulation in a 90nm CMOS process.

Characteristics	Reference DCO [13]	Proposed DCO
1. DCO Period Range	489 ~ 1247 (ps)	467 ~ 1946 (ps)
2. β-Segment Size	45 ~ 252 (ps)	29 ~ 32 (ps)
3. Resolution	0.52 ~ 3.85 (ps)	0.79 ~ 0.96 (ps)
4. β-Segment Overlap Ratio	46.4 ~ 68.0 (%)	61.3 ~ 74.2 (%)
5. Worst DNL / INL	-72.5 / -155.7 (ps)	3.4 / -6.9 (ps)

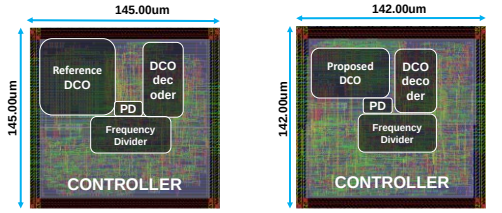
A robust DCO should be able to operate correctly under the most extreme process and operating conditions. We perform an extensive simulation to verify our DCO design under 5 process corners {TT, SS, FF, FS, SF} and 5 sampled temperatures in {-40˚C, 0˚C, 25˚C, 85˚C,150˚C}. The results are listed in **Table 3**. Among them, the resolution is [0.64ps, 1.17ps], meaning that the worst-case resolution is as small as 1.17ps even under the most extreme condition. Last but not least, the β-segment overlap ratio is still positive, meaning that there is no period gap under the worst process and the worst temperature.

Table 3: Summary of Characteristics of the proposed DCO **under extreme process and temperature conditions**.

Characteristics Summary of the Proposed DCO under Extreme Process and Temperature Conditions Process Corners: {TT, SS, FF, FS, SF} x Temperatures {-40˚C, 0˚C, 25˚C, 85˚C,150˚C}	
1. DCO Period Range	646 ~ 1493 (ps)
2. β-Segment Size	23 ~ 42 (ps)
3. Resolution	0.62 ~ 1.25 (ps)
4. β-Segment Overlap Ratio	23.4 ~ 73.1 (%) Still Positive

III. VERIFICATION METHODOLOGY AND SIMULATION RESULT OF THE PLL WITH THE NEW DCO AND BISG

A. *Layout and Simulation Waveform of Optimized PLL*



(a) Layout of PLL with reference DCO. (b) Layout of PLL with the proposed DCO.

Fig. 6: The layout of PLLs using a 90nm CMOS process.

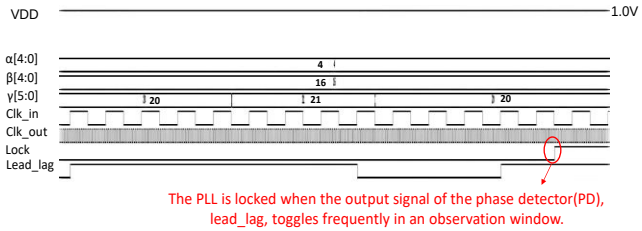


Fig. 7 Post-layout simulation waveforms of the cell-based PLL with the proposed DCO using a 90nm CMOS process (TT corner, 25℃).

The layouts of cell-based PLLs with the reference DCO and the proposed DCO using a 90nm CMOS process are shown in **Fig. 6.** The simulation waveforms of the cell-based PLL with the proposed DCO using a 90nm CMOS process are shown in **Fig. 7**. We use the EDA tool, VCS-XA, developed by Synopsys Inc. to perform post-layout mixed-level simulation of our cell-based PLLs, and perl scripts to measure the peak-to-peak jitters. A 10,000ns simulation takes about 16 hours to complete. The simulation shows that our PLL is locked under the three-level control code <α, β, γ>=<4, 16, 20-21>. Due to the havering of the γ-code between 20 and 21, the phase detector's output signal, i.e., *lead_lag*, toggles several times within an observation window to indicate a locked condition.

Table 4: Characteristics of cell-based PLL with the proposed DCO based on post-layout simulation in a 90nm CMOS process.

Characteristics	The cell-based PLL with the Reference DCO [13]	The cell-based PLL with the Proposed DCO
1. Area	21025(um^2)	20164(um^2)
2. Power	3.879mW	3.008mW
3. Peak-to-Peak Jitter	10.86(ps)	6.07(ps)

The key characteristics of two versions of PLLs producing 1GHz clock signals by taking a 50MHz reference clock are listed in **Table 4**. Area achieves a reduction ratio of (21025-20164)/21025 = 4.09% and power achieves a reduction ratio of

(3.879-3.008)/3.879 = 22.45%, respectively. The post-layout simulation reveals that the peak-to-peak jitters within an observation window of over 2000 clock cycles after locking are indeed reduced from the original 10.86ps to 6.07ps, achieving a reduction ratio of (10.86-6.07)/10.86 = 44%.

B. Verifacation and Simulation Result of BISG

One key application of the PLL is used to as on-chip clock generation to produce different test clock frequencies. As the benefit, it helps us to perform BISG. The flow chart of BISG methodology is shown in **Fig. 8**. It is by performing multiple runs of BIST to approach the maximum operation speed (Fmax). However, it takes a lot of time to wait for the PLL locking and test pattern shifted in to perform all-transistor level BISG simulation. In order to speed up the simulation process and get the fast verification, there are two methodology. One is using mixed-level simulation and the other is verify BISG by performing Built-In Self Test (BIST) of different test clock frequencies at the same time.

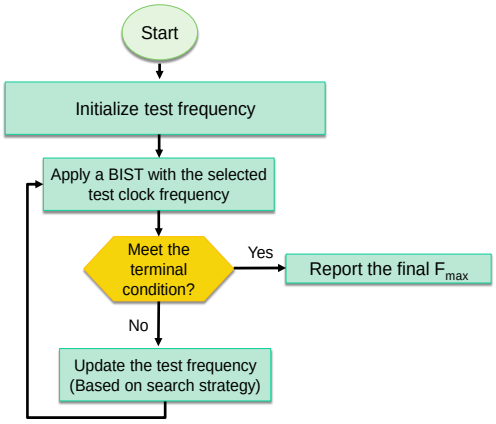


Fig. 8: The flow chart of BISG methodology.

We use the EDA tool, VCS-XA, developed by Synopsys Inc. to perform post-layout mixed-level simulation. The mixed-level simulation module is shown in **Fig. 9**, in which the most important part of the circuit, the data-path of the PLL and the circuit under test (e.g. 16 bits adder) with BIST component, is modeled in the transistor level to keep up the timing information precisely, while the controller of the PLL is in the RTL. The advantage of using RTL module for PLL controller is to set the initial control code of DCO close to the target frequency, that can make the PLL lock faster to reduce the simulation time. Furthermore, BISG is by performing multiple runs of BIST to approach the maximum operation speed (Fmax). Therefore, to get the fast verification result, we can simulate the BIST under different test clock frequencies at the same time. This may takes fewer time since the PLL can lock faster due to mixed-level simulation but also no need on waiting the BIST pass/fail signal to change the test clock frequency.

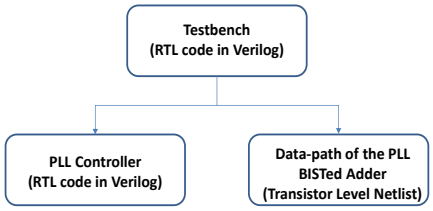


Fig. 9: The mixed-level simulation module for BIST.

To get fast verification, the simulation waveforms of BIST for 16 bits adder under 1ns and 1.1ns test clock using a 90nm CMOS process are shown in **Fig. 10 and Fig. 11** respectively. Both test clock 1ns and 1.1ns take about 7500ns on waiting the cell-based PLL to lock. After the test clock being prepared, we start the BIST progress. The BIST progress is done, once shifting in all the test pattern generated by LFSR. Then we compare between the signature compressed by MISR and golden signature. The pass/fail signal goes high if they are the same, which means the CUT can operate under that test clock. For example, a 16 bits adder can operate under 1.1ns and may fail under 1ns.

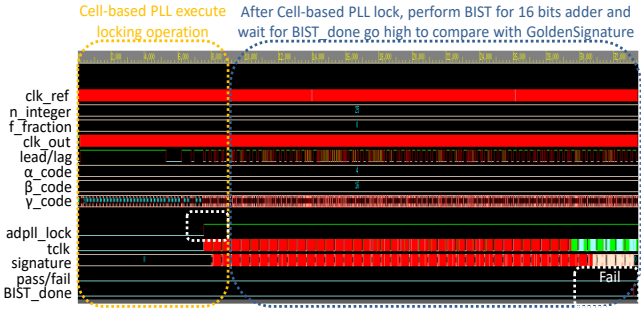


Fig. 10: The simulation waveforms of BIST for 16 bits adder under 1ns.

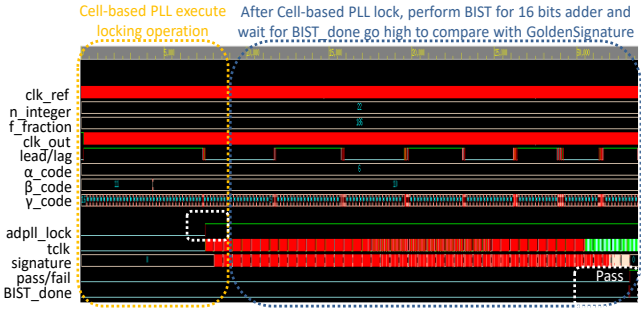


Fig. 10: The simulation waveforms of BIST for 16 bits adder under 1.1ns.

The simulation results of critical path delay (the reciprocal of F_{max}) for different bits binary adder using a 90nm CMOS process are shown in **Fig. 12**. The result includes design compiler report result, gate-level simulation result, mixed-level simulation result. The result shows that we can do speed grading for different CUT to find out F_{max} by these verification while reduce simulation time.

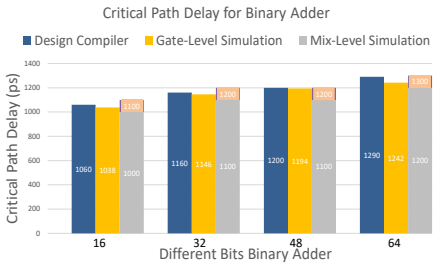


Fig. 12: The simulation results of critical path delay (the reciprocal of Fmax) for different bits binary adder.

IV. Conclusion

To get a more accurate on-chip high-speed test clock signal, we design a new DCO architecture. We use the EDA tool, VCS-XA, to simulate and perl scripts to analyze the characteristics of the DCO. This can make us find out the DCO good or not quickly instead of observing the simulation waveform in detail.

As the result, we can achieve better features beyond existing solutions. First, our architecture does not have any "DCO period gap" even under 5 process corners and an extreme temperature ranging from -40 to 150. This feature makes our DCO very robust. Last, but not the least, our DCO has a linear DCO period profile, thus contributing to a uniform 1ps step resolution across the supported output clock period range. Compared to a prior reference design, the worst-case resolution has been effectively reduced from 3.85ps to 0.96ps in a typical condition or to 1.25ps in extreme process and temperature conditions, leading to a peak-to-peak jitter reduction of 44% from the original 10.86ps to 6.07ps in the PLL that uses this new DCO, while the area and the power consumption is less than the previous version.

And to get fast verification of BISG, we use mixed-level simulation and perform BIST of different test clock frequencies. This takes less time on simulation and can successfully find out the circuit under test operation speed.

Acknowledgments

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