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SAR ADC Layout Generation Using Digital Place-and-Route Tools

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***Abstract*—Digital place-and-route (DPR) tools are used to interconnect the analog macro-cells and digital circuits in two asynchronous successive approximation register (SAR) analog-to-digital converters (ADCs) with 12-bit 20-MS/s and 10-bit 100-MS/s. To realize the macro-cells of analog sub-circuits, three techniques are used to mitigate the parasitic effects caused by the DPR tools. The software settings for the macro-cell generation are presented. Compared to the full-custom method, to facilitate the interconnection wires of the 12-bit SAR ADC, it is speed up by a factor of 288 by using the DPR flow.**

***Keywords*—Successive approximation register, analog-to-digital converter, digital place-and-route, capacitive digital-to-analog converter, bootstrapped switch, and dynamic logic.**

I. Introduction

The successive-approximation-register (SAR) ADCs are widely adopted because of the advantages of low power and small area. For the advanced CMOS processes, since the design rules of the layout become more and more complex, it is difficult to generate the layout of the mixed-signal circuit in a short time. Furthermore, if the ADC is migrated to other processes, its layout should be re-designed.

To realize the layout of the synthesizable SAR ADCs using the DPR tools [1]–[3], it saves the place-and-route time. However, the nonlinearities are induced to impact the sensitive analog circuits [4], [5]. For instance, the linearity of the capacitive digital-to-analog converter (CDAC) and the bootstrapped switch, the leakage current in the dynamic digital circuits, the current density of the metal interconnections, and the IR drop issues have been considered [4]. In [5], the charge sharing of the bootstrapped switch, the offset voltage of the comparator. and the ripple of the reference voltage are considered. Different from [4], [5], the software settings for analog cell library and layout generation flow are focused on in this article. It is organized as follows. Section II gives the circuit description of the proposed SAR ADC by using the digital place-and-route (DPR) tools. Section III gives the experimental results. The conclusion is given in Section IV.

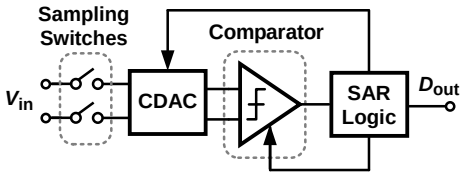


Fig. 1. A simplified SAR ADC.

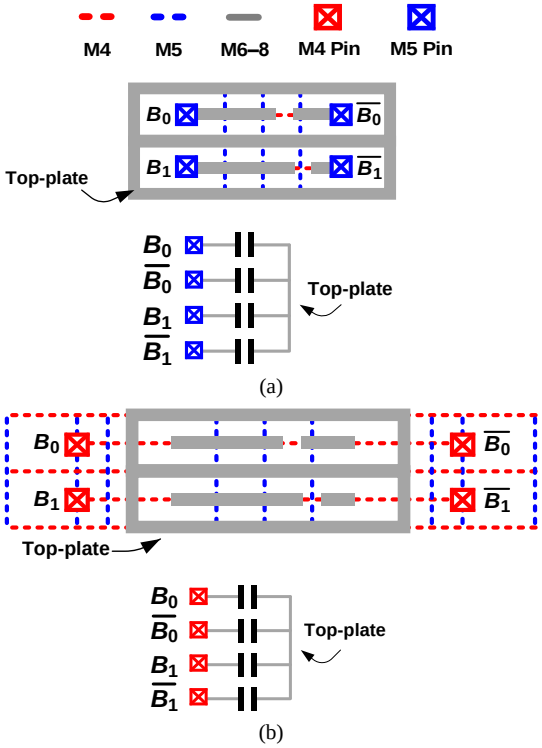


Fig. 2. The macro-cell of a two-bit CDAC with (a) a shield and (b) an extended shield [4].

II. Analog Cell Generation Considerations

Fig. 1 shows that a simplified SAR ADC which is composed of sampling switches, a CDAC, a comparator, and a SAR logic. To use the DPR tools, several considerations for the layout of analog sub-circuits will be discussed as follows.

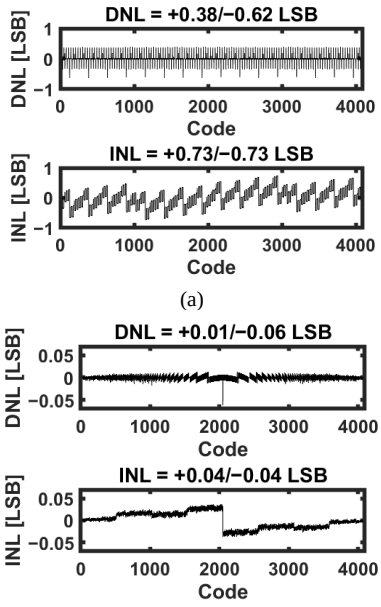


Fig. 3. Simulated DNL/INL of the 12-bit CDAC (a) without and (b) with extended shield and "cover" metal blockage level of 6th-8th metal layers. .

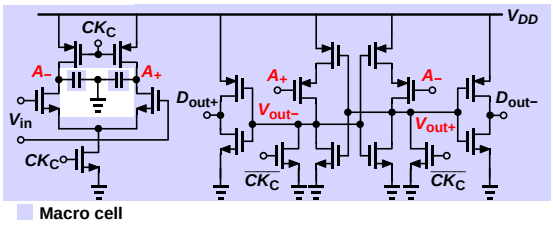


Fig. 4. A dynamic double-tail comparator.

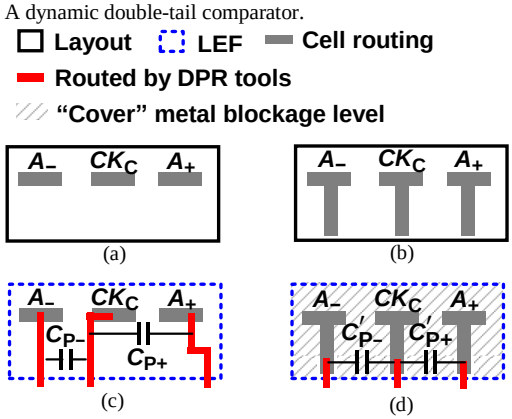


Fig. 5. The layout settings of the comparator's macro-cell (a) without and (b) with the "cover" metal blockage level, respectively. The LEF routed by DPR tools (c) without and (d) with the "cover" metal blockage level, respectively.

TABLE I
SIMULATION RESULTS OF COMPARATOR CELL

	Fig. 5 (c)	Fig. 5 (d)
$C_{P+} - C_{P-}$ ($C'_{P+} - C'_{P-}$)	1.7 fF	0.6 fF
Comparator offset	1.125 mV	0.425 mV

A. CDAC

The CDAC is realized by using differential difference capacitors [6]. Fig. 2(a) shows the macro-cell of a 2-bit CDAC which is realized by using 6th-8th metal layers. The active circuits are connected by the 1st–3rd metal layers. The 4th and 5th metal layers are used as a shield to isolate the coupling noises from the active circuits. If the 5th–8th metal layers are automatically routed as the interconnections by DPR tools, the parasitic capacitors between the bottom and top plates are induced to degrade the CDAC linearity.

Fig. 2(b) shows the macro-cell of a 2-bit CDAC with an extended shield which is realized by the 4th and 5th metal layers. By using the DPR tools, the coupling capacitances induced by the 5th metal layer are mitigated by the extended shield. The tool "Abstract generator" [7] is used and the metal blockage level is set as "cover" for the 6th–8th metal layers. The router doesn't route the 6th–8th metal layers beside the macro-cell. Thus, the top-plate of the CDAC is not affected by the coupling capacitances induced by the 6th–8th metal layer. The metal blockage level is set as "detailed" for the 4th and 5th metal layers. The router connects the CDAC drivers and the macro-cell by the 1st–3rd metal layers.

The macro-cell of a 12-bit CDAC [4] is realized by the above considerations. Its simulated DNL/INL results are shown in Fig. 3. Without both the extended shield and the "cover" metal blockage levels of 6th–8th metal layers, the peak DNL and INL are +0.38/−0.62 LSB and +0.73/−0.73 LSB, respectively. With both the extended shield and the "cover" metal blockage levels of 6th-8th metal layers, the peak DNL and INL are +0.01/−0.06 LSB and +0.04/−0.04 LSB, respectively.

B. Comparator

Fig. 4 shows a dynamic double-tail comparator with the clock CK_C. It is well-known that the mismatch between the parasitic capacitances at the nodes of A_+/A_- and V_{out+}/V_{out-} degrades the input-referred offset voltage [8]. is shown in Fig. 5(a) and (b) shows the layouts for abstract generator settings of the comparator's macro-cell without and with the "cover" metal blockage level, respectively. The LEF routed by DPR tools without and with the "cover" metal blockage level is shown in Fig. 5(c) and (d), respectively. In Fig. 5(c), the coupling capacitances C_{P+} and C_{P-} between the metal layers by the DPR tools degrade the comparator's offset. With the "cover" metal blockage level, the router can only access the nodes A_-, CK_C, and A_+ of the macro-cell on the boundary. Thus, Fig. 5(d) shows the final layout with the coupling capacitances C'_{P+} and C'_{P-}. Table I shows that the simulated capacitance differences, $C_{P+} - C_{P-}$ and $C'_{P+} - C'_{P-}$, are equal to 1.7 fF and 0.6 fF, respectively. The corresponding input-referred offset is reduced from 1.125 mV to 0.425 mV.

C. Multi-Macro-Cell Floorplan

Fig. 6(a) and (b) show the floorplan of macro-cells and standard cells without and with the placement constraint, respectively. It's well-known that the standard cells need a N-well process layer. In Fig. 6(a), if the standard cells

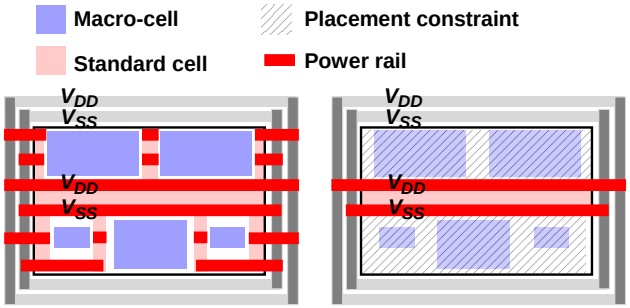


Fig. 6. Floorplan (a) without and (b) with the placement constraint.

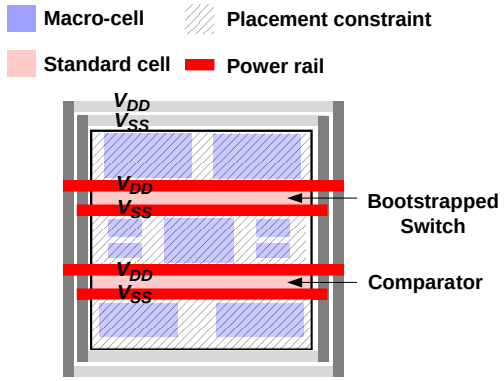


Fig. 7. Floorplan of a bootstrapped switch and a comparator.

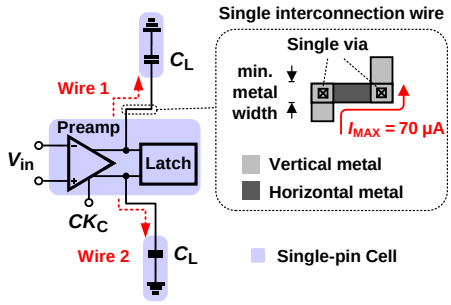
zones are separated by the macro-cells without the placement constraint, the body cells have to be added in each zone. These small zones may violate the DRC rules, such as N-well narrow spacing and small area. To fix them, Fig. 6(b) shows the floorplan with the placement constraint by the tool Encounter [9]. Since the standard cells can't be placed inside the constraint, the DRC errors are avoided. The placement constraint for DRC error can be extended to more than one zone. Fig. 7 shows the floorplan of the bootstrapped switch and the comparator [4][5].

D. Current Density

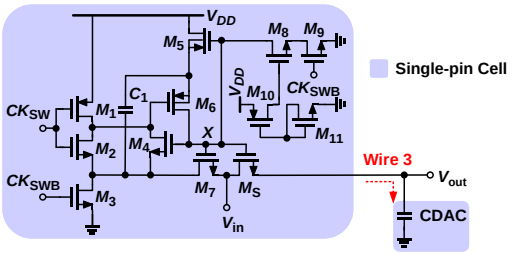
Fig. 8(a) shows that there are two interconnection wires between the pre-amplifier with the latch and the loading capacitors C_L in the dynamic double-tail comparator. Note that the capacitor C_L is realized as a macro-cell. By using the DPR tools, the vertical and horizontal routings usually utilize the different metal layers. Besides, the metal with a minimum width and a single VIA are used for the voltage-driven routing. For a 40-nm process, the maximum current I_{MAX} for the minimum width metal and a single VIA is limited to 70μA. Fig. 8(b) shows an interconnection wire between the proposed bootstrapped switch and the CDAC. To know the current density of the metal layer, the averaging current of the capacitor within the time Δt is approximated as

$$\bar{I} = \frac{C \times \Delta V}{\Delta t} \qquad (1)$$

where C is the capacitance and ΔV is the voltage difference of the capacitor. The averaging currents passing the three interconnection wires are calculated and summarized in



(a)



(b)

Fig. 8. Single interconnection wire of (a) the comparator and (b) the bootstrapped switch and the CDAC.

TABLE II
THREE CURRENT-DRIVEN WIRES

Wire	C	ΔV	$\bar{I}$	Δt
1, 2	200 fF	0.9 V	93.6 μA ($> I_{MAX}$)	$\frac{1}{20\,M} \cdot \frac{1}{2} \cdot \frac{1}{13}$
			187.2 μA ($> I_{MAX}$)	$\frac{1}{40\,M} \cdot \frac{1}{2} \cdot \frac{1}{13}$
3	1360 fF	0.9 V	48.96 μA	$\frac{1}{20\,M} \cdot \frac{1}{2}$
			97.92 μA ($> I_{MAX}$)	$\frac{1}{40\,M} \cdot \frac{1}{2}$

Table II. The capacitances C_L and the CDAC are equal to 200 fF and 1.36 pF, respectively. Δt is estimated by the reciprocal of the sampling frequency multiplied by the charging or discharging operation times. ΔV is equal to the supply voltage of 0.9 V. For every conversion cycle of the ADC, the comparator operates 13 times including the twelve bits and one redundant bit. When the sampling rate is equal to 40 MS/s, the average current of the interconnection wires of Fig. 8(a) and (b) are equal to 187.2 μA and 97.92 μA, respectively. By using the DPR tools, both averaging currents exceed the maximum one of 70 μA. For Fig. 8(a), when the sampling rate is equal to 20 MS/s, the average current of the interconnection wire is equal to 93.6 μA which also exceeds 70 μA.

A standard cell uses a single-pin as shown in Fig. 9(a), which has a limited the current density. To deal with this issue, Fig. 9(b) shows the multi-pin cell used in this work. For example, four pins, A[0], A[1], A[2], and A[3], are used to have a large current driving capability. Three settings should be utilized; the first one is in layout; the second setting is in "Abstract generator", and the last one is in Verilog netlist. To translate the layout to the LEF by "Abstract generator" [7], the connectivity of each pin is

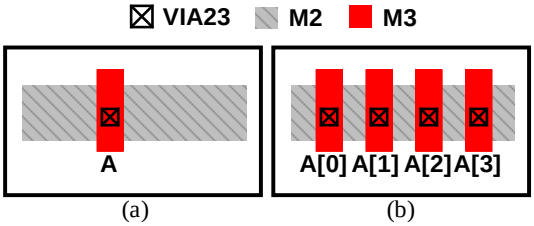


Fig. 9. (a) Single-pin cell and (b) multi-pin cell.

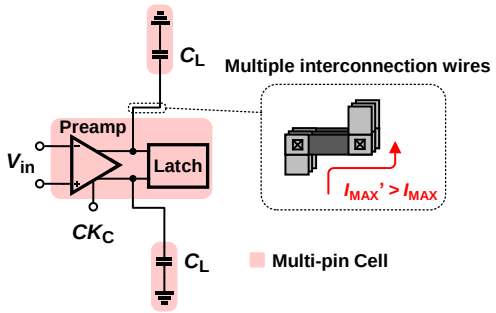


Fig. 10. Multiple interconnection wires for the comparator in the DPR flow.

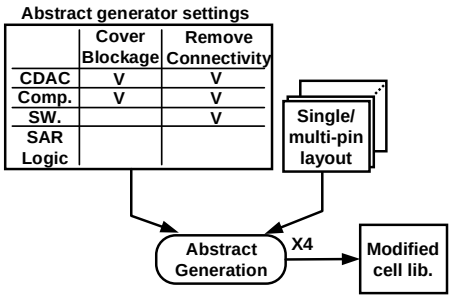
checked. The "pin short" errors among A[0], A[1], A[2], A[3] may occur. It is not allowed to connect four different pins to the same metal layer by VIAs. To eliminate these errors, two settings should be used. First, the pins A[0]–A[3] should be labelled on the 3rd metal layer. Second, the connectivity realized by the 2nd, 3rd metal layers and the VIAs (M2, M3, and VIA23) should be removed in "Abstract generator". With these two settings, the "pin short" error is avoided and the pins A[0]–A[3] are labelled on the 3rd metal layer. Finally, in Verilog netlists, the net A should be declared as an array type (i.e., wire A[3:0]) for multi-pin interconnection wires. With these three settings, the minimum current density of four wires can is increased up to 280 μA.

The pre-amplifier with the latch and the loading capacitor C_L are realized by the multi-pin cells as shown in Fig. 10. The number of the multiple interconnection wires should be higher than the ratio of the averaging current to I_{MAX}. In this work, four interconnection wires are used in the dynamic comparator.

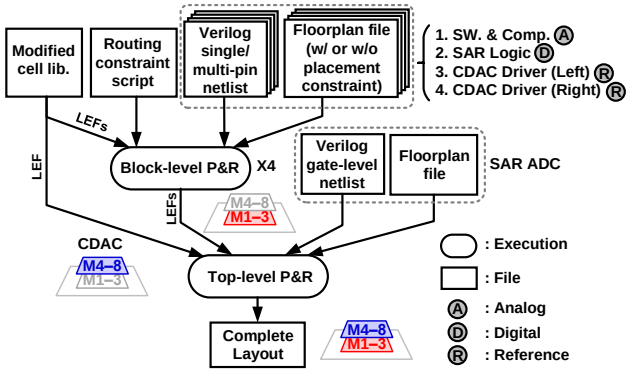
E. DPR Flow

Fig. 11(a) shows the modified cell library generation flow. To consider the coupling capacitor issues (Section II-A, II-B), the metal blockage level "cover" should be set for the CDAC and the comparator in "Abstract generator" [7]. For the CDAC, the comparator, and the switch, the connectivity should be removed to consider the current density issue (Section II-D). To mitigate the current density issue (Section II-D), the multi-pin cells are used for the CDAC, the comparator, and the switch. The "Abstract generator" will generate the modified cell library.

Fig. 11(b) shows the DPR flow. First, the modified cell library is generated from Fig. 11(a). Second, the routing constraint script is generated by Encounter [9] with the 1st-3rd metal layers. Third, the Verilog single/multi-pin netlists should be declared as an array type. Fourth, the floorplan



(a)



(b)

	Setup time per file	# of file
Modified cell lib.	17 hours	1
Routing constraint script	1 mins	1
Verilog single/multi-pin netlist	10 mins	5
Floorplan file	20 mins	5

(c)

Fig. 11. (a) Modified cell library generation, (b) DPR flow, and (c) the setup time of the DPR flow [4][5].

files for the bootstrapped switch and the comparator should be setup with the placement constraints to consider the N-well related DRC errors (Section II-C) in Encounter [9]. Then, four LEF files are generated by the block-level place and route (P&R). For the top-level P&R execution, a modified cell library, four LEF files from the block-level P&R execution, a Verilog netlist, and a floorplan file are required to generate the final layout of SAR ADC. Fig. 11(c) shows the setup time of the DPR flow. First, the abstract settings and single/multi-pin cell layouts are required as shown in Fig. 11(a). The setup time for abstract settings takes less than 5 minutes for each abstract generation. For the time to draw the layouts, it depends on the complexity of each cell. The layout time of the CDAC array and the comparator takes 3 and 10 hours, respectively. For the remaining three macro-cells and five custom cells for the switch and the SAR logic, they take 4 hours. It totally takes 17 hours for the modified cell library. Second, the routing constraint script is generated by Encounter tool [9] with the setup time of 1 min. Third, each Verilog gate-level netlist requires the setup time of 10 mins by using the Virtuoso NC-Verilog tool [10]. Finally, the generation of each floorplan files takes 20 mins by Encounter tool [9]. The setup time for the SAR ADC in the proposed DPR flow is about 19.5 hours.

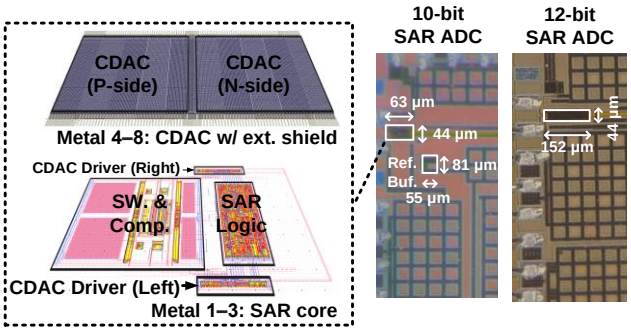


Fig. 12. The layout of a 10-bit SAR ADC and the die photos for two ADCs.

TABLE III
TOTAL REQUIRED WIRES

	Routed Wires	
	12-bit 20-MS/s SAR ADC [4]	10-bit 100-MS/s SAR ADC [5]
CDAC	62	22
Bootstrapped switch	40	40
Comparator	14	14
SAR Logic	195	165
Total	311	241

TABLE IV
PERFORMANCE SUMMARY TABLE

	12-bit 20-MS/s SAR ADC [4]	10-bit 100-MS/s SAR ADC [5]
Process [nm]	40	40
Area [mm^2]	0.0067	0.0072
Supply [V]	0.9	0.9
Resolution	12	10
DNL [LSB]	+2.08/−0.96	+0.54/−0.43
INL [LSB]	+1.24/−1.41	+0.46/−0.64
$SNDR_{LowF.}$ [dB]	63	57
$SNDR_{Nyq.}$ [dB]	59.5	53.4
$SFDR_{Nyq.}$ [dB]	72.4	71
Power [µW]	363	418
F_S [MS/s]	20	100
$FoM_{W,LowF}$ [fJ/c.step]	15.7	7.2
$FoM_{W,Nyq.}$ [fJ/c.step]	23.5	10.9
Calibration-free	No	Yes
Synthesizable	Yes	Yes

III. EXPERIMENTAL RESULTS

Fig. 12 shows the layout of a 10-bit 100MS/s SAR ADC which are generated by the DPR flow. The die photos of the 12-bit 20MS/s and 10-bit 100MS/s SAR ADCs [5] are also shown in Fig. 12. These two SAR ADCs [4,5] are fabricated by 40nm CMOS process. Table III shows the total wires required for these two SAR ADCs. The total interconnection wires are 311 and 241 for the 12-bit and 10-bit ADCs, respectively. Suppose 5 minutes are required to complete one interconnection wire between two circuits. By using the full-custom method, 1555 minutes and 1205 minutes are required to complete the interconnection wires of the 12-bit and 10-bit ADCs, respectively, including the time for DRC/LVS. By using the DPR tools, the total runtime is within 5 min to complete the layout of the SAR ADC. To compare with the full-custom method, the proposed DPR flow can save a lot of time to complete the interconnection wires. Table IV shows the measured performance summary of two SAR ADCs. The Walden FoMs for the 12-bit 20MS/s and the 10-bit 100MS/S SAR ADCs are 23.5 and 10.9 fJ/c. step, respectively.

IV. CONCLUSION

To consider the coupling capacitances and the current density issue, several techniques are presented to realize the macro-cells for the SAR ADC. The DPR tools are used to complete the interconnection wires of the SAR ADC efficiently. Finally, the layouts of two SAR ADCs are generated by using the DPR tools. Experimental results are also given to demonstrate the proposed techniques.

ACKNOWLEDGMENT

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