2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION JAPAN

Enhancing PHY Design Verification: A Tailored VIP Solution for PIPE Interface-Based Designs

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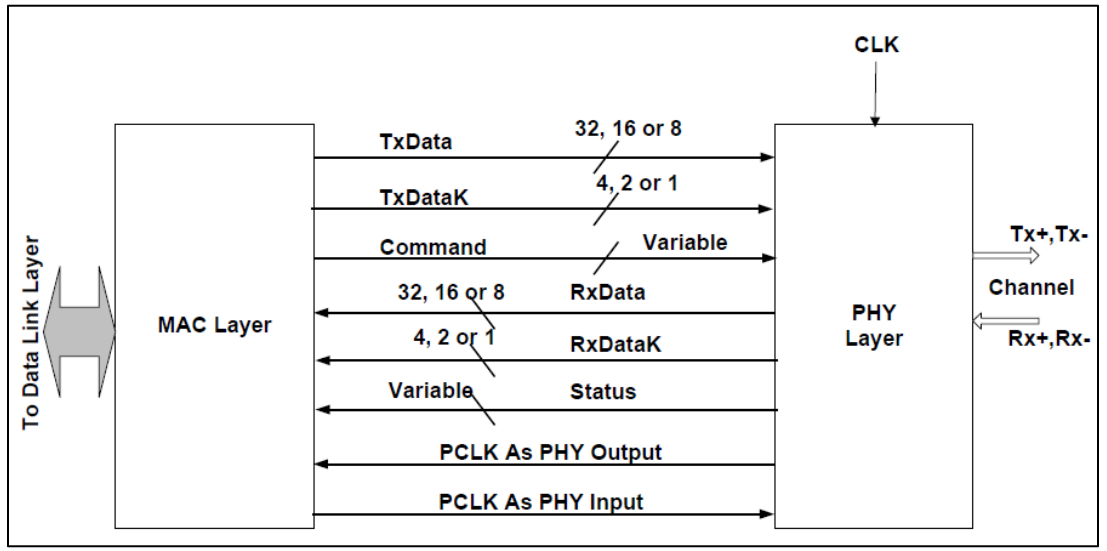
Introduction to PHY VIP

- The **P**HY **I**nterface for the **P**CI **E**xpress (PCIe), SATA, USB3.2, DisplayPort, and USB4 Architectures (**PIPE**) is intended to enable the development of functionalities equivalent to the PHYs of PCIe, SATA, USB, DisplayPort, and USB4.

- These PHYs can be delivered as discrete Integrated Circuits (ICs) or as macrocells for inclusion in Application-Specific Integrated Circuit (ASIC) designs



Introduction to PHY VIP

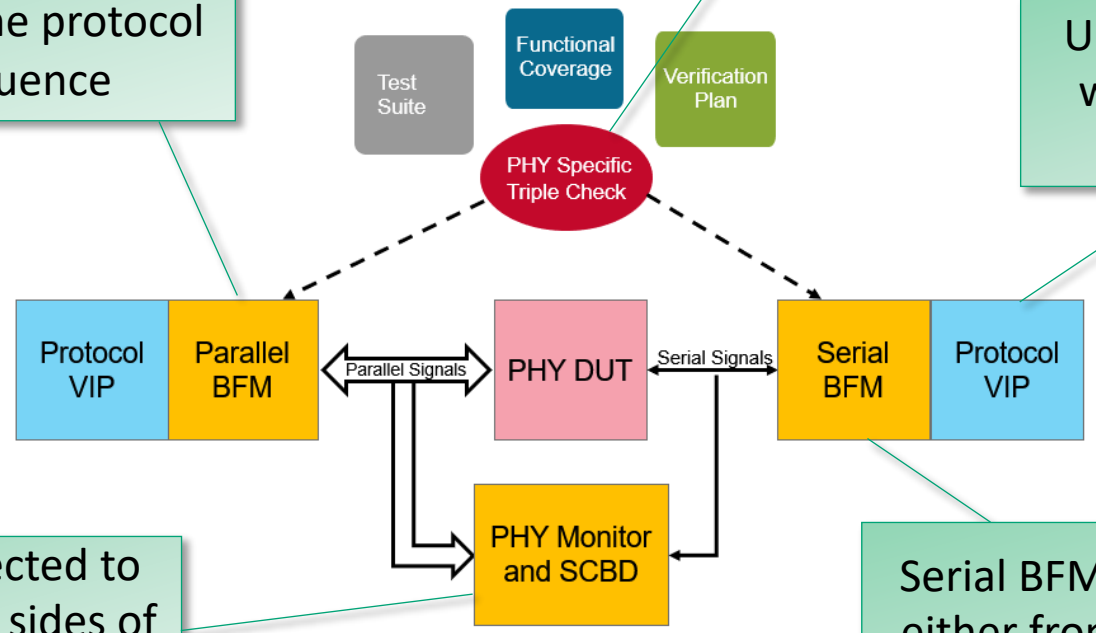
- Cadence's customers have been verifying different PHY designs using Cadence protocol VIPs for many years.
- The protocol VIPs were mainly designed for full stack verification and introduced an overhead to the verification in the form of the protocol specific rules that were outside the scope of the PHY.
- The trend in PIPE specification is simplifying the PHY design to allow reuse and move more logic to the MAC (e.g. SerDes architecture introduced in PIPE 5.0)
- Cadence PHY VIP solution offers a PHY specific test suite.
- This resulted in a development of a PHY specific VIP, to address the unique challenges of a PHY design.

PHY VIP Architecture

PHY specific TripleCheck solution with a verification plan on the PIPE spec mapped to relevant PIPE coverage items

Parallel BFM, driving traffic into the PHY either from the protocol VIP or from a sequence

Under-the-hood connection with protocol VIPs to drive protocol specific traffic

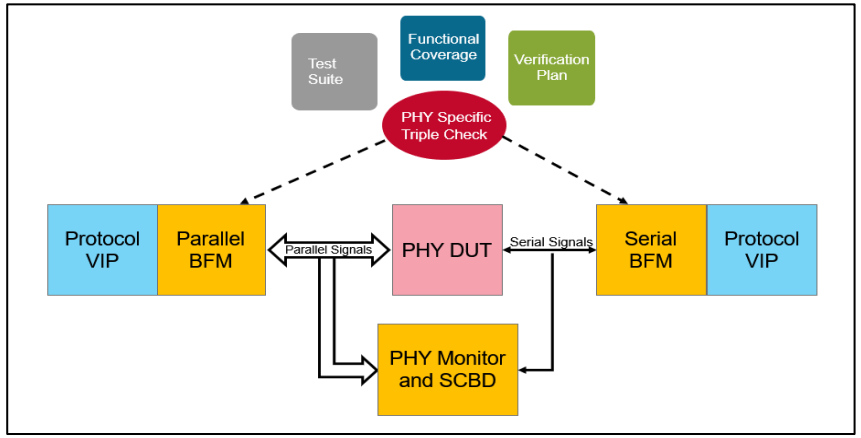


PHY monitor connected to both serial and PIPE sides of the PHY

Serial BFM, driving traffic into the PHY either from the protocol VIP or from a sequence as well as handling SSC+jitter

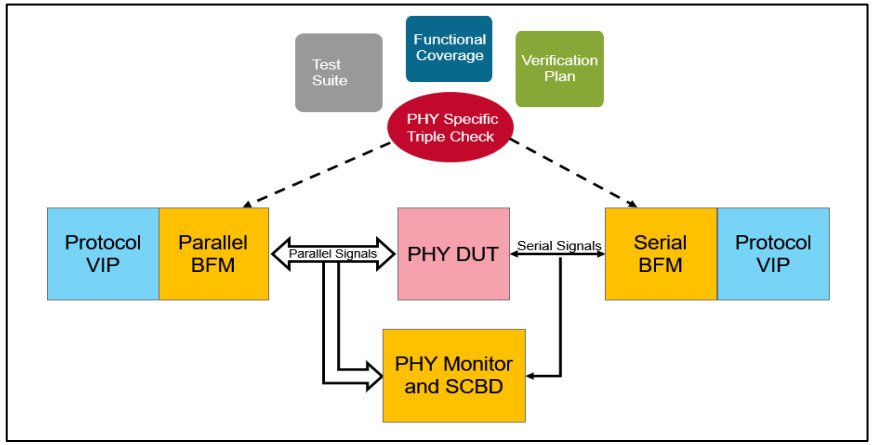
BFM Features

- Drive data into the PHY
  - API to drive data transactions.
  - API to sample PHY outputs
  - API to drive PHY inputs.



- Ability to control Jitter/SSC to stress CDR logic (serial BFM only).
- Callbacks on before/after the encoder and the serializer to allow fine grain control
- Transmit/receive bit clock can be either TB generated or internally generated/recovered.
- Can be connected seamlessly to a protocol VIP and drive protocol traffic.
  - Currently supported for USB/USB4, planned for PCIe.

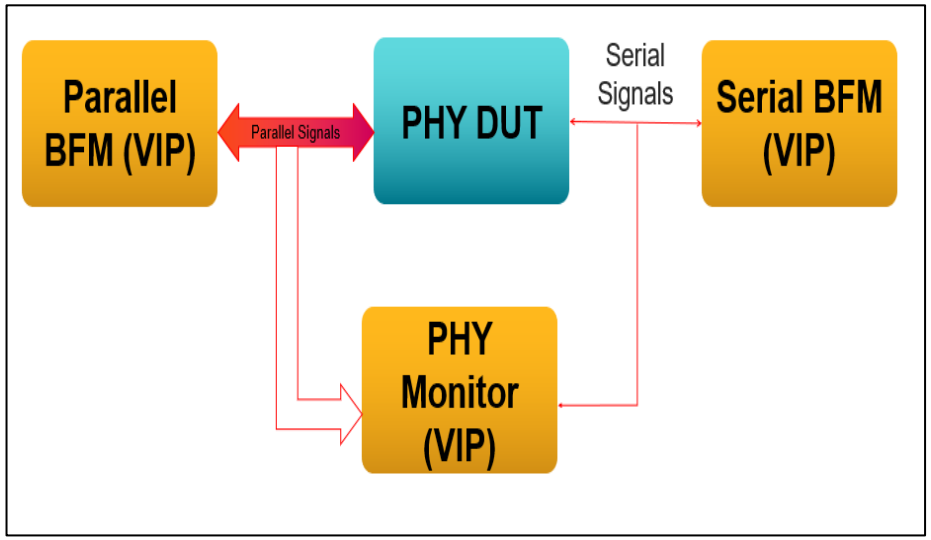
PHY Monitor Features



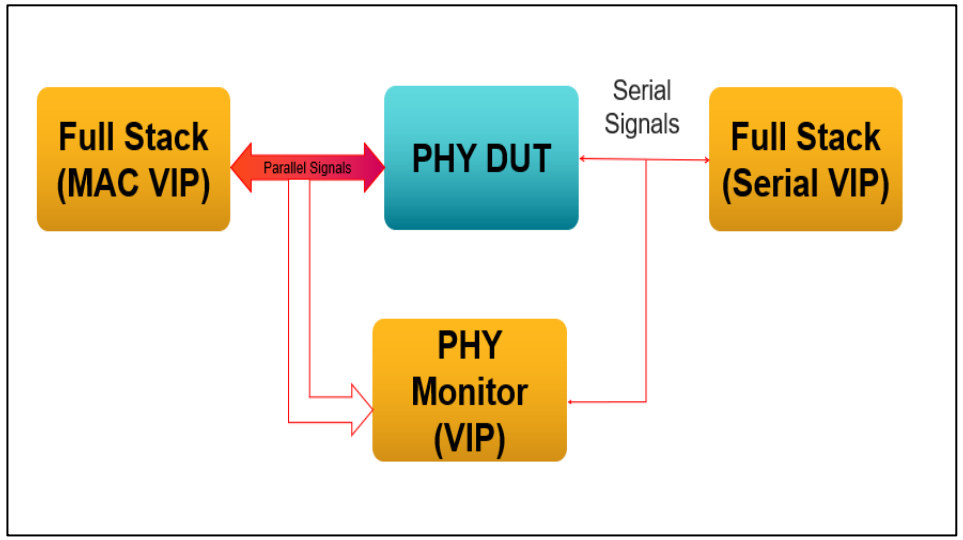
- Built in score boarding on Rx, Tx and loopback
  - Ability to deal with data consumed by phy
  - Checking effected by changes made by elastic buffer (in original PIPE mode).
- Unique ability to check data across the PHY (unlike a monitor who is only aware of a single interface).
- Callbacks to capture the data for custom checking.
- Comprehensive timing configuration to ensure PHY responds within the desired time period.

USE Models (1/2)

- PHY DUT environment where traffic is driven by the PHY BFM on both serial and PIPE side.

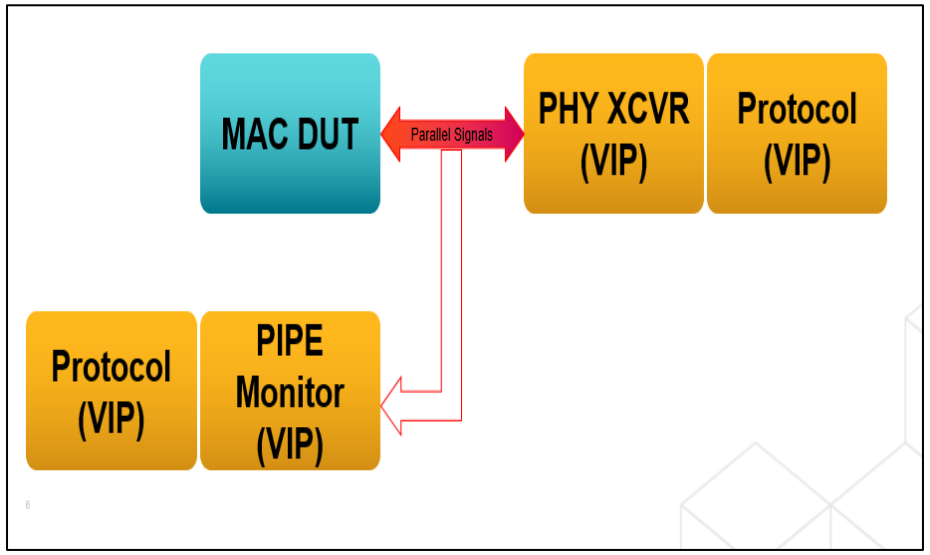


- Monitor only environment where the PHY monitor is added on top of protocol VIPs.

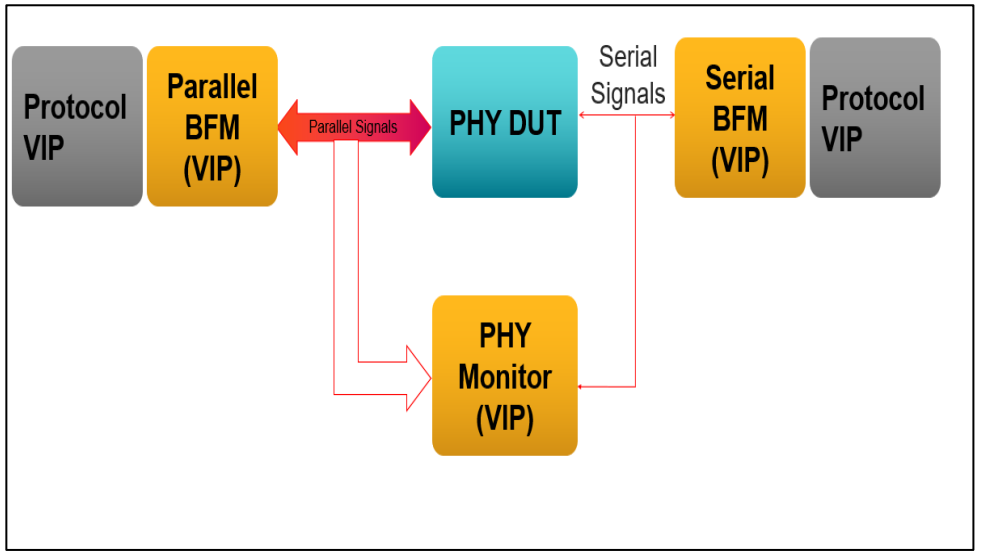


USE Models (2/2)

- MAC DUT environment without having serial interface env.



- Protocol + PHY VIP integrated environment for PHY DUT verification.



PHY VIP unique capabilities (1/2)

- The PHY monitor was designed for PHY VIPs and therefore allows built in support of features that previously were not supported or required complex testbench code:
  - Out of the box built in data score boarding which is flexible enough to support common phy scenarios (consuming data due to bit/symbol/block lock, phy delays, etc.)

```
/************************** Tx Path Score Board Summary ************************/
   Number of symbols matched: 1899
   Number of mismatch errors: 0
   Number of symbols uncompared: PIPE side: 0, Serial side: 0
   Number of skip symbols received: PIPE side: 0, Serial side: 0
   Number of skip ordered sets received: PIPE side: 0, Serial side: 0
   Pipe Line Delay: 12 Symbols
   /*******************************************************************************/
```

  - The SCBD is reset every time the DUT enters electrical idle and starts again once data transmission continues (independently on Rx and Tx path)

PHY VIP unique capabilities (2/2)

- End to end checkers, that ensure that actions on the PIPE side are handled in a timely manner on the serial interface.

```
  DENALI_PIPEPHY_NON_IDLE_LINES_AFTER_TXELECIDLE_SET = 117, // PIPE spec Table 6.2 : Tx D
p/Dn lines are not idle even %s after TxElecIdle signal is asserted at %s.Program the exp
ected PHY Delay value using SOMA Parameter :tTxElecIdleResp or Register: DENALI_PIPEPHY_R
EG_TXELECIDLE_RESP_TIME.
```

- Glitch checkers on both serial and PIPE signals.

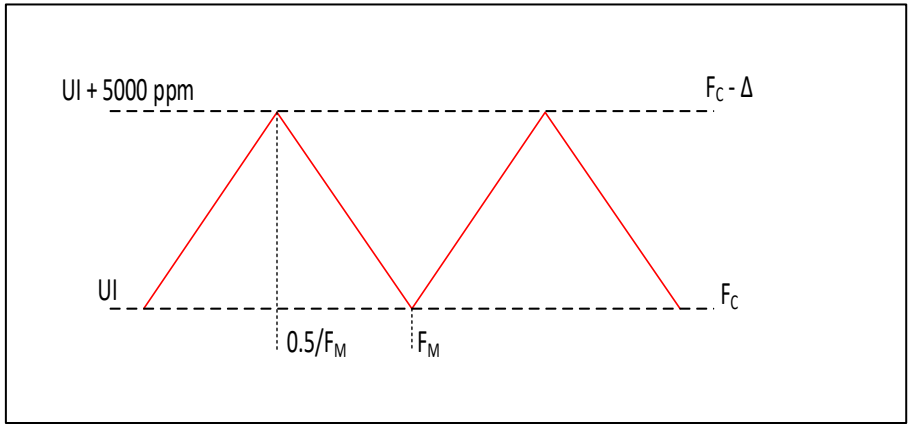
```
DENALI_PIPEPHY_SERIAL_TX_UI_GLITCH = 129, // PIPE spec Section 6 : Detected Glitch on T
Serial line. Expected bit time = %s. Received bit time = %s.
```

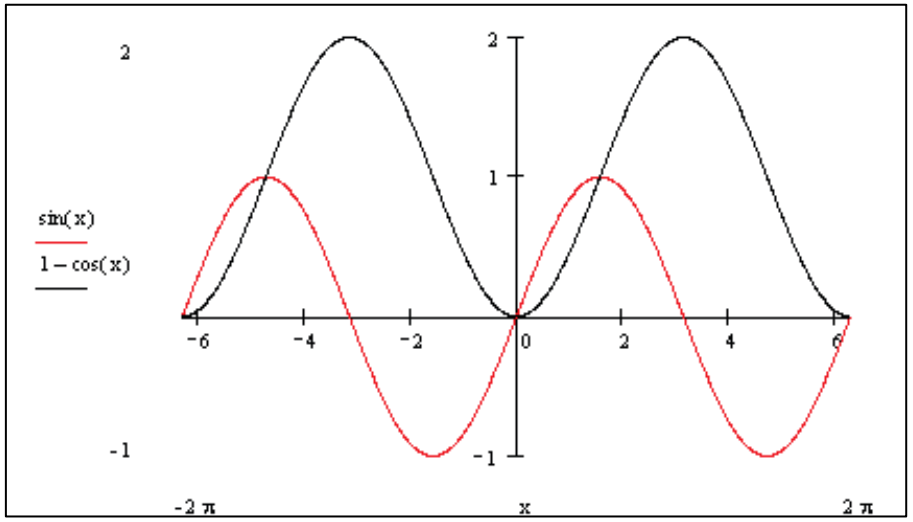
- Simplified configuration with PHY related items only.

- Over 200+ PHY specific checkers.

PHY VIP unique capabilities

- SSC - Triangular wave with down spread
  - PPM offset on the output clock
  - Control parameters:
    - Modulation frequency
    - SSC PPM
    - Offset PPM
- Jitter
  - Absolute jitter – programmable parameters
    - Amplitude
    - Frequency
  - Random jitter – programmable parameter
    - - Variance
  - Total Jitter = Absolute Jitter + Random Jitter



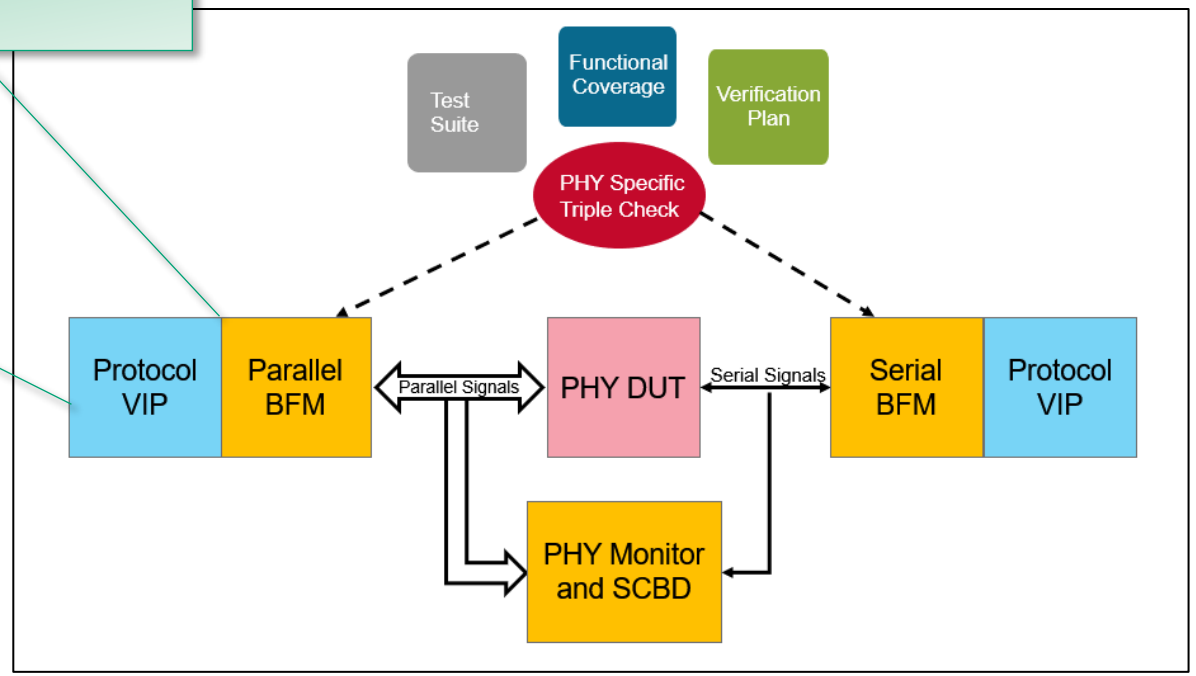


Integration with Protocol VIP

- Long term plan is to have all relevant VIPs use the PHY VIP

Seamless connection in the c-layer

Ability to use protocol transactions and link training but data will be sent using the PHY VIP



Q & A