Enhancing PHY Design Verification: A Tailored VIP Solution for PIPE Interface-Based Designs

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***Abstract*—Customers have been verifying their PCIe, DP, USB, USB4 PIPE PHY designs using protocol VIPs or custom traffic generators, which introduced an overhead to the verification in the form of protocol specific rules that were outside the scope of the PHY. Also, there was no PHY monitor solution which can observe both serial and parallel interface of the PHY DUT. Identifying this gap, Cadence developed a solution to address standalone PHY DUT Design verification.**

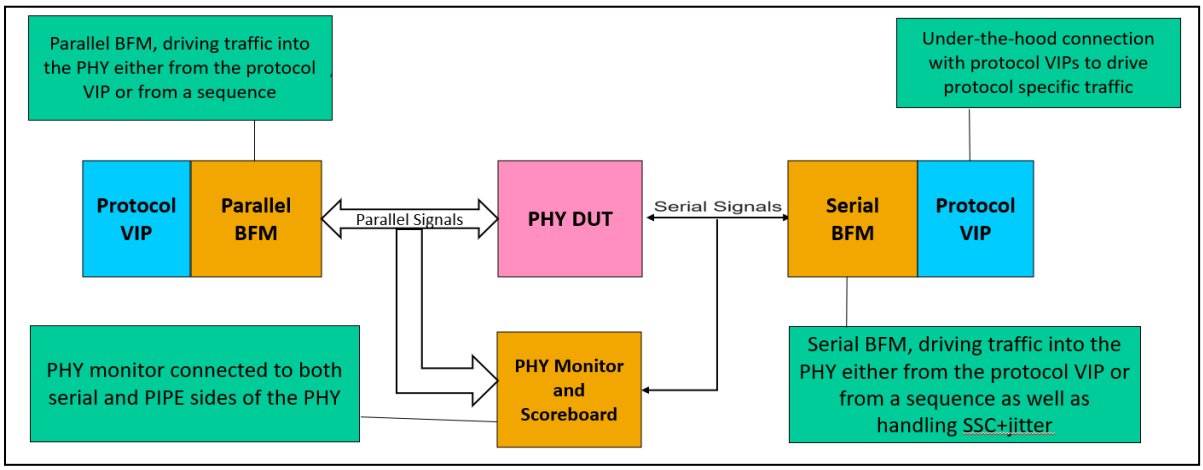
Keywords—PIPE based PHY Design Verification; SERDES PHY verification; Verification of PCIE/DP/USB3/USB4 with PIPE Interface;

I. Related Work

PHY DUT verification used to be done through testchip or FPGA or through protocol VIPs. Therefore, Cadence came up with the solution to completely verify PHY DUT without any dependency on the MAC DUT or protocol specific traffic.

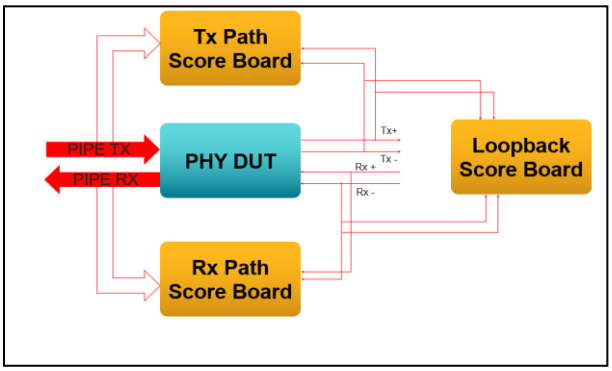
II. PHY VIP Architecture

PHY VIP solution consists of three components PIPEXceiver (Parallel BFM), SerialXceiver (Serial BFM) and PHYmonitor. PIPEXceiver and SerialXceiver components were developed to be able to drive and receive traffic to/from PHY DUT, which provide very granular control of all PHY DUT signals. PHYmonitor was developed to monitor serial and parallel interface of the PHY DUT and for scoreboarding purpose.



PHY VIP BFM components PIPEXceiver and SerialXceiver can be connected seamlessly to a protocol VIP to drive protocol traffic. BFM contains APIs to drive data transactions, and to sample PHY inputs and outputs. Serial BFM has an ability to control Jitter/SSC to stress CDR logic. BFM provides an option to generate transmit or receive bit clocks through testbench or can be generated internally.

PHY monitor has built-in scoreboard which monitors Tx and Rx path of parallel as well as serial interface of PHY DUT. Scoreboard is capable enough to validate transactions during normal transactions as well as when loopback is enabled. It also has ability to deal with the data consumed by the PHY DUT for the clock data recovery (CDR). Unlike a regular monitor which is only aware of a single interface, PHY monitor has a unique ability to check data across the PHY. PHY monitor has comprehensive timing configuration to check that the PHY DUT responds within the desired time period or not. Also, PHY monitor has an option to check PIPE compliance on signals driven by the MAC/controller when connected to a controller DUT. Scoreboard is agnostic to protocol, ordered sets, data blocks, and symbol types.



PHY monitor scoreboard

Cadence PHY VIP solution is compatible with all verification languages like SV/UVM/OVM. Cadence PHY VIP solution supports all different verification tools like Xcelium, VCS, MTI.

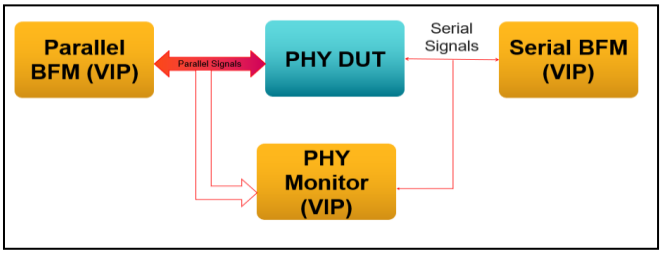
III. APPLICATIONS

There are several applications of using Cadence's PHY VIP solution which helped many of our customers in verifying their setup quickly and more robustly. Below are some of the major applications,

- Customers were using protocol VIPs or custom traffic generators to verify their PCIe, DP, USB, USB4 PIPE PHY designs. Our PHY VIP solution reduce this overhead of verification.
- By using standalone PHY VIP solution customers can verify major features such as asymmetric link and message bus separately without using protocol VIP, which can reduce their verification effort significantly.

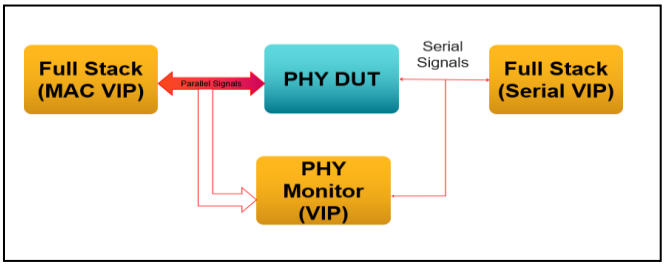
PHY VIP use models: Below are some of the examples of PHY VIP use models,

- **PHY DUT environment** where traffic is driven by the PHY BFM on both serial and PIPE side.



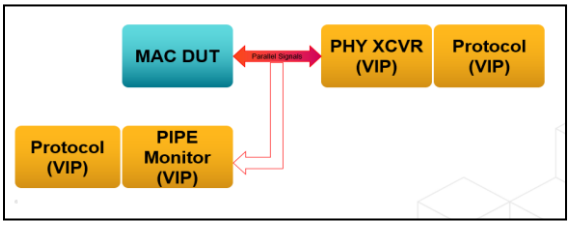
Use Model-I

- **Monitor only environment** where the PHY monitor is added on top of protocol VIPs, where MAC VIP and Serial VIP are having their own pipe and serial interface respectively.



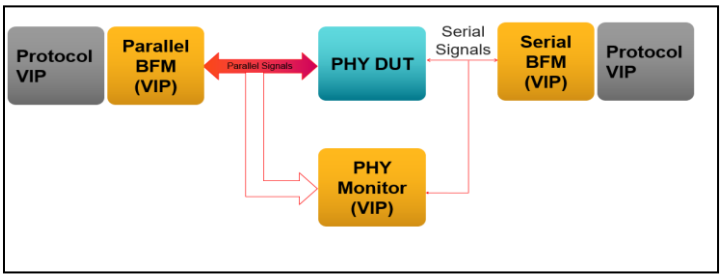
Use Model-II

- MAC DUT environment **without having serial interface env**.



Use Model-III

- **Protocol + PHY VIP integrated environment** for PHY DUT verification, where Parallel BFM and Serial BFM are generic PHY VIP components.



Use Model-IV

IV. PHY VIP UNIQUE CAPABILITIES

PIPE specification is fully mapped and annotated with all possible cover groups. User can enable/Disable PHY VIP features statically as well as dynamically.

Cadence has created coverage plans for all different PHY specification versions like 4.3, 4.4.1, 5.x, 6.x for protocols like USB3, USB4 and PCIe. Created cover groups based on different features like PowerDown, MessageBus, PclkRate, Rate, LFPS and many more to incorporate all possible scenarios through our coverage plan to provide granular coverage report to our users.

Also, Cadence have handled coverage of features which are interrelated with each other. For example, rate,width and PclkRate have some valid and invalid combinations. So, Cadence has also exercised such interrelated signals through cross-coverage to improve overall coverage efficiency.

PHY monitor was designed for PHY DUTs and therefore allows built in support of features that previously were not supported or required complex testbench code. PHY monitor provides built in data scoreboarding which is flexible enough to support various scenarios such as consuming data due to bit/symbol/block lock, phy delays, etc.

```
/************************ Tx Path Score Board Summary ********************/
   Number of symbols matched: 1899
   Number of mismatch errors: 0
   Number of symbols uncompared: PIPE side: 0, Serial side: 0
   Number of skip symbols received: PIPE side: 0, Serial side: 0
   Number of skip ordered sets received: PIPE side: 0, Serial side: 0
   Pipe Line Delay: 12 Symbols
   /************************************************************************/
```

Example of scoreboard log

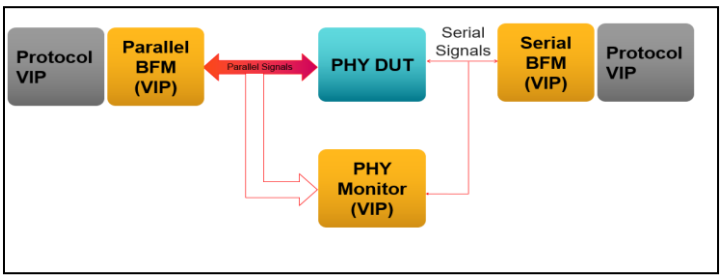
PHY VIP solution has PHY specific checkers to verify PHY DUT extensively. PHY VIP solution does not have any protocol (USB3, USB4 or PCIe) specific checkers, it has all PHY specific checkers which covers all the different PHY features like PowerDown, MessageBus, Width, PclkRate, Rate, LFPS, Tx/RxElecIdle, RxValid, TxDetectRx, Rxequalization, RxMargining and many more. Cadence have taken a particular feature and created checkers for all possible combinations require to validate that feature, like wise Cadence has created groups of checkers for all other different PHY features.

Through 200+ end-to-end checkers PHY monitor ensures that the actions on the pipe interface are handled in a timely manner on the serial interface and vice versa. Below is an example of one of the PHY monitor checker,

```
  DENALI_PIPEPHY_NON_IDLE_LINES_AFTER_TXELECIDLE_SET = 117, // PIPE spec Table 6.2 : Tx D
p/Dn lines are not idle even %s after TxElecIdle signal is asserted at %s.Program the exp
ected PHY Delay value using SOMA Parameter :tTxElecIdleResp or Register: DENALI_PIPEPHY_R
EG_TXELECIDLE_RESP_TIME.
DENALI_PIPEPHY_SERIAL_TX_UI_GLITCH = 129, // PIPE spec Section 6 : Detected Glitch on T
 Serial line. Expected bit time = %s. Received bit time = %s.
```

Example of VIP checker log

V. INTEGRATION OF PROTOCOL VIP WITH PHY VIP



As shown in the above diagram user can verify their standalone PHY DUT using generic PHY VIP components – Parallel BFM, Serial BFM and PHY Monitor (shown in the yellow box above). User can generate transactions as per their verification needs and PHY VIP components will ensure the verification of that test is done efficiently.

To verify PHY DUT with Protocol traffic, user can use Protocol VIP along with generic PHY VIP components. User can use USB3, USB4, DP or PCIe protocol VIPs (developed by Cadence) along with PHY VIP components to verify their PHY DUT. Here Protocol VIP and PHY VIP components are connected through an adapter logic which is built as a part of Protocol VIP and it is transparent to the end user. This kind of integration makes the simulation faster compared to integrating using signals. So, the end user needs to only put efforts to write protocol test and the rest is taken care of by the VIP depending on whether they are driving PIPE interface or Serial interface. All the control and data information of the Protocol is passed to PHY VIP through internal interface. This integrated VIP takes care of driving the appropriate power signals to the PHY VIP based on the Protocol state machine.

VI. CHALLENGES

The biggest challenge Cadence development team faced was to verify the data integrity of PHY DUT. It means to ensure PHY DUT is transmitting valid data on serial (Tx Path)/parallel (Rx Path) interface. To address this, Cadence has introduced a scoreboard in PHY monitor component. Users are verifying PHY DUT using protocol test suite. In this, users were not having granular control of all the PHY DUT signals. To resolve this challenge, Cadence has created Parallel BFM with comprehensive set of APIs using which user can create any complex scenario to verify PHY DUT.

VII. RESULTS

To verify PHY DUT, customers were using PCIe or USB3 or USB4 protocol VIPs. Cadence has come up with a better way to verify PHY DUT more quickly and efficiently. With standalone Cadence's PHY VIP solution customer can plug their PHY DUT without using any protocol VIPs and they can drive interface signals as per their verification needs and verify their PHY DUT separately. Once their PHY DUT is verified separately with our PHY VIP solution, they can plug the protocol VIPs on top of the PHY VIP to verify PHY DUT more exhaustively.

Initially with the protocol VIPs, the PHY DUT verification was more tedious and time consuming as customers must make sure of protocol specific rules. With PHY VIP approach, Cadence observed that customers were able to close their PHY DUT verification cycle quickly.

Cadence has created a separate component PHY XCVR which provides a direct parallel connection between MAC and protocol VIP. With this solution users have seen around significant improvement in test case simulation time. Refer fig. Use Model-III above for this solution topology.

VIII. CONCLUSION

Cadence's PHY VIP solution provides features like built in scoreboard, SSC, Jitter, clock data recovery, PHY specific coverage, reduced verification effort, better performance and speeding up regression closure. With Cadence's PHY VIP solution user can verify their PHY DUT for any protocol without really using a protocol VIP. Cadence solution also allows the user to extend their verification env to include full protocol stack once their standalone PHY design is fully verified. Cadence PHY VIP solution is compatible with different PHY modes like PCIe, DP, USB3, USB4.

IX. ABBRIVIATIONS USED

VIP: Verification Intellectual Property

DUT: Design Under Test

PHY: Physical Layer

BFM: Bus Functional Model

CDR: Clock and Data Recovery

API: Application Programming Interface

PIPE: PHY interface for PCIe Express, SATA, USB, DP and USB4

FPGA: Field Programmable Gate Array

MAC: Media Access Layer

SSC: Spread Spectrum Clocking

LFPS: Low Frequency Periodic Signaling

SERDES: Serializer/deserializer

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REFERENCES

[1] PHY Interface for the PCI Express*, SATA, USB 3.2, DisplayPort*, and USB4* Architectures