2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION JAPAN

New Serial NAND Flash Octal Double Data Rate Feature

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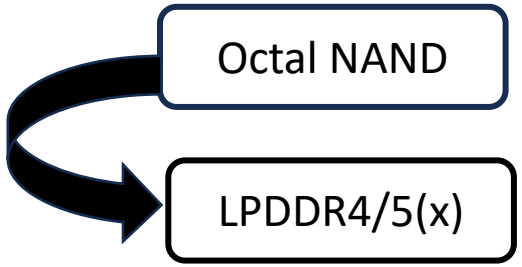
Introduction

- SPI NAND memory is an ideal candidate for automotive applications
- To meet the increasing bandwidth needs of the automotive industry, SPI NAND Flash memory vendors added the Octal SPI interface with double data rates (DDR)
- The Octal double data rate protocol uses an 8-bit wide synchronous bus interface active on both rising and falling edge of the system clock for command, address and data
- Winbond SPI NAND Flash already supported high speed continuous read across Page and Block boundaries
- Combined → increase in complexity of the verification matrix

Winbond perspective on Motivation for SPI Octal NAND

- Fast startup time in emerging automotive applications needs Flash of high read thruput
  - FCM (Front Camera Module), DMS (Driver Monitor System), and ADAS Domain control are some of such applications

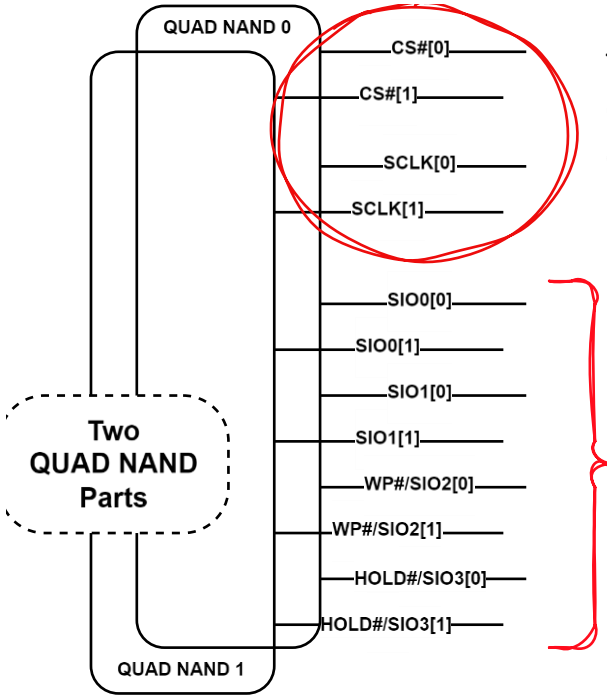


- Many such automotive applications download from Flash to LPDDR4/5(x) at startup
  - Time to download 2Gb is 3 sec with QSPI NOR or QspiNAND at 80MB/s, whereas only 1 sec with Octal NAND at 240MB/s
  - Fast startup time is important for either user experience (e.g. FCM and DMS) or regulatory requirement (e.g. rear camera)
- Winbond Octal NAND of 1Gb~4Gb densities provide novel code storage Flash solution
  - SoC partners have enabled or are in process of enabling support for Octal NAND
  - EDA partners such as Cadence provide timing models (covered in paper) to help with SoC support of Octal NAND
- Winbond Octal NAND has multiple projects under design-in/production and growing !

Problem Statement

- New changes in architecture and design implementation limit rapid and effective verification
- Though pin compatible with Octal SPI NOR Flash devices
  - Cannot apply existing NOR Flash verification memory models
  - Cannot apply existing Serial, Dual or Quad NAND Flash models
- Challenges when compared with actual SPI Octal NAND Flash devices :
  - Cannot model the Command-Address-Data instruction sequences at the transactional level
  - The pin level signaling is incompatible
  - AC/Timing characteristics are inconsistent

NXP ODDR Controller IP Verification

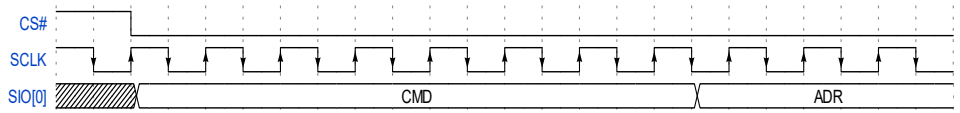


The **CS#** and **SCLK** outputs from the ODDR Controller design can be split to drive the corresponding pins of the Quad NAND models together

The two Quad NAND parts would offer 8 **SIO*n*** pins for the 8-bit ODDR Controller – any method of combining or interleaving the pins would superficially meet the architectural requirements for Octal DDR NAND.

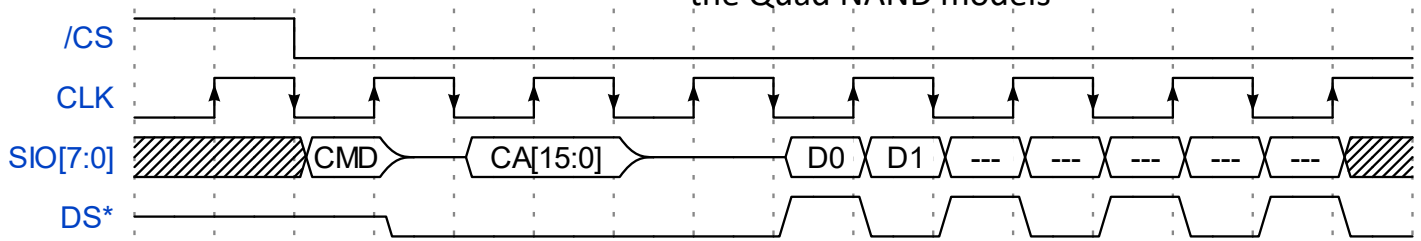
BUT… at a transactional level, the command-address-data encoding scheme would be in violation.

For the Fast Read instruction, the Quad NAND model expects to receive 8 bits of the command on **SIO0** pin over 8 clock cycles



BUT… the ODDR Controller will drive a 1-byte Octal DDR Fast Read command on all **SIO[7:0]** pins and over ONE clock cycle

The ODDR Controller would also drive the new **Data Strobe DS** signal but that will be ignored by the Quad NAND models

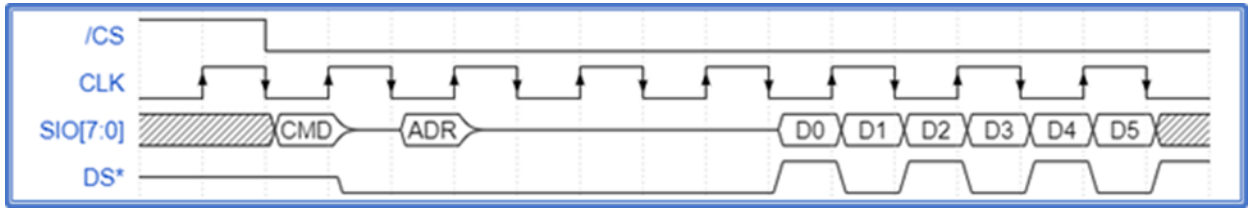


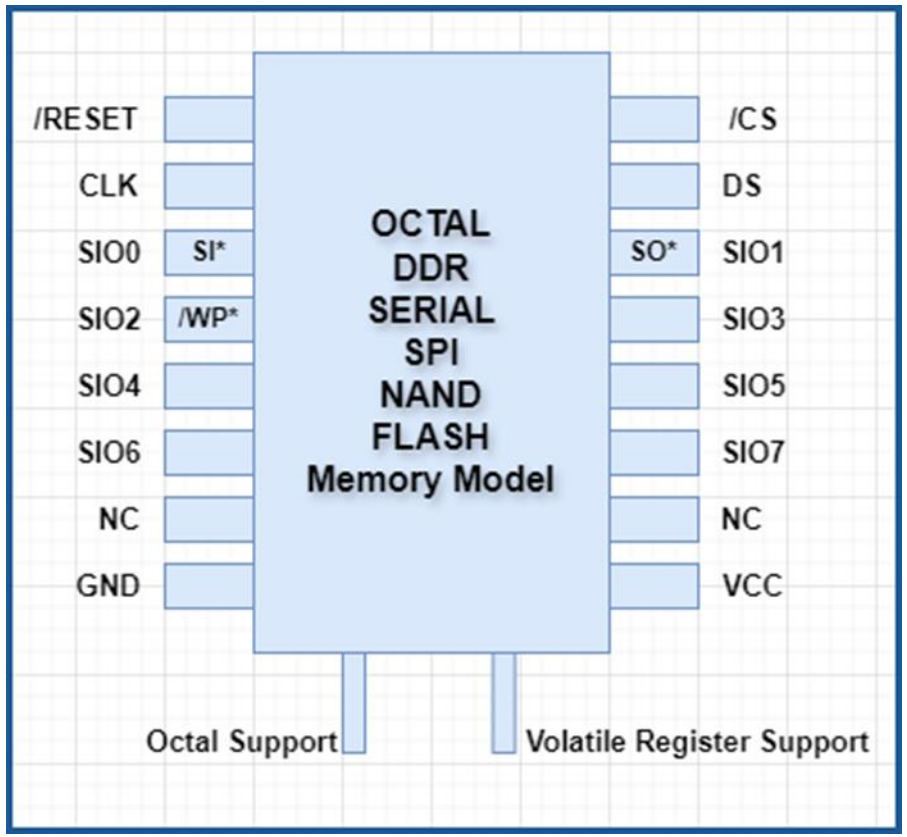
Solution

- Cadence/Winbond Collaboration:
  - Added SPI Octal DDR Verification support to existing SPI NAND Memory Model
- New Operational Mode: SPI Octal DDR NAND Flash Memory Model
  - Supports functional simulation at theoretical maximum 240MB/s continuous read data transfer rates at 120MHz clock speeds
- New command specifications:
  - Command format follows the C-A-D (Command-Address-Data) sequence as specified in the Winbond datasheets
- Full backward compatibility:
  - Programmable to operate in 1-bit and 8-bit SPI Single Data Rate mode, 1-bit and 8-bit SPI Double Data Rate mode

Implementation

- SPI Octal DDR capabilities enabled with a new configuration parameter
- Additional configuration parameter to enable support for a Volatile Configuration Register for programming of the correct Octal transfer mode
- Legacy SI and SO pins are reused as SIO0 and SIO1, respectively, the /WP pin is reused as SIO2, and new SIO3-SIO7 pins are added to the package.
- New Data Strobe output pin, DS, acts as strobe for data output added to the package
- Volatile Config Register programming supported for DS-selection per Winbond datasheets





With the SPI Octal DDR interface, the data transfers over the Serial NAND wires are adapted to utilize the 8-bit wide data bus now available, along with the data strobe transferring data on every clock edge

Implementation Details

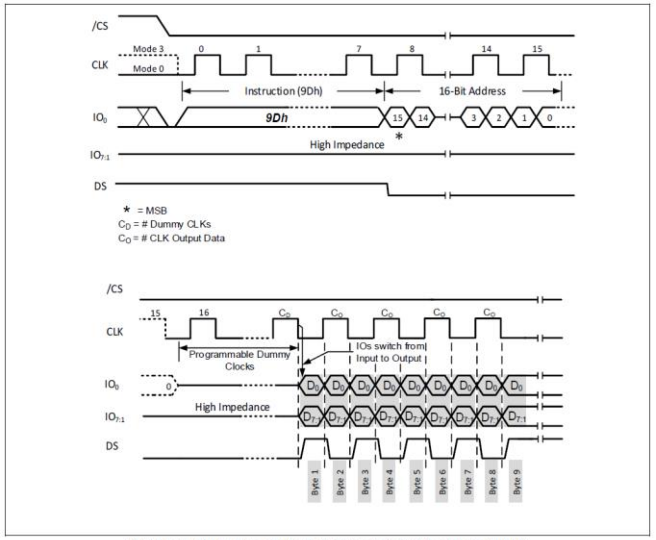


Figure 8-49 DDR Fast Read Instruction SDR mode (Buffer Read Mode, BUF=1)

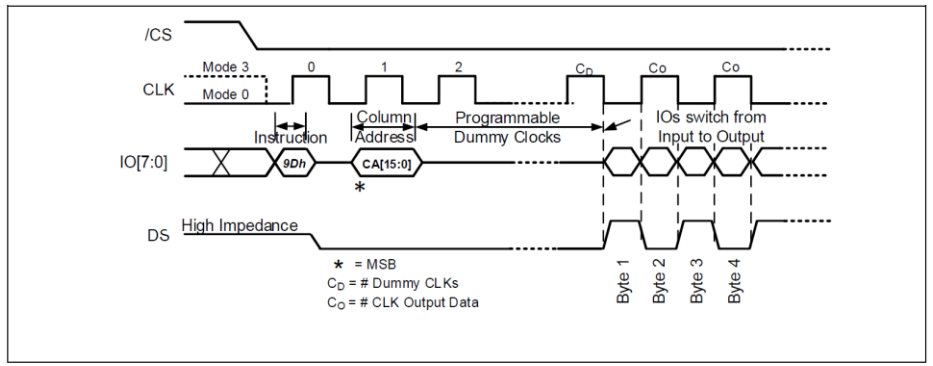
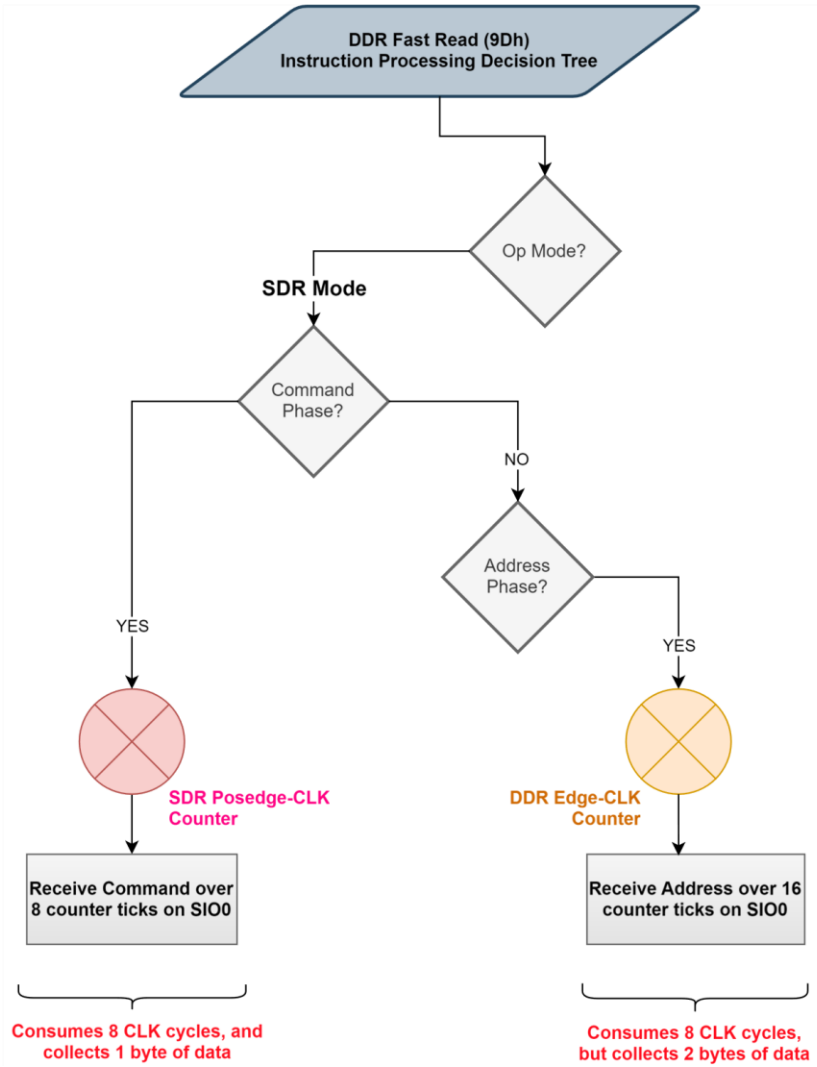


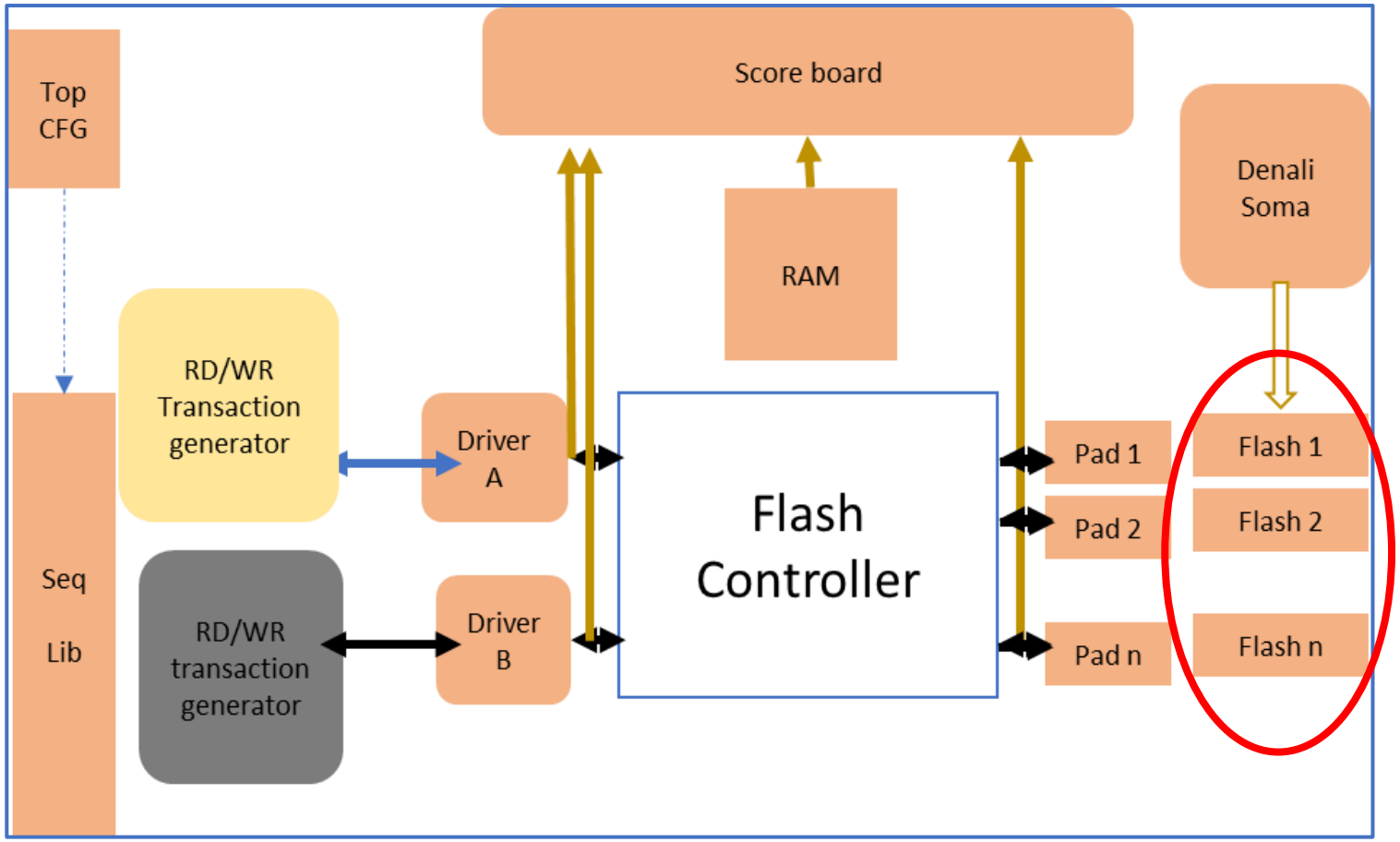
Figure 8-51 DDR Fast Read Instruction ODDR mode (Buffer Read Mode, BUF=1)

Source: Images from Winbond W35N01JW Datasheet



Verification Results at NXP - 1

- New SPI NAND models with updated Octal interface were seamlessly dropped into testbench with new Octal Flash Controller design IP
- Configurability allowed testing of all density grades
- New model architecture allowed command stream to adapt seamlessly based on programmed density



Verification Results at NXP - 2

- Enhanced model's extensive checks helped identify bugs in Controller for driving incorrect register configurations for specified frequency ranges

```
*Denali* Error: Detected[testbench.flashA.flash] ADDR_NOT_COMPLETED @2503648596 ps :: For Fast Read Octal DDR Output Command command the CSn pin is de-asserted @ 2503648596 ps But the Address cycle is not completed.
*Denali* Error: Detected[testbench.flashA.flash] DUMMY_CYCLE_NOT_COMPLETED @2647085497 ps :: Dummy cycle not completed. CSn high without DataIn or DataOut for Fast Read Octal DDR Output Command command @ 2647085497 ps
```

- Model's Data Valid Window timer enabled testing of invalid data regions
- Model drove valid data during valid window timer and X's outside the window

```
*Denali* Error: Detected[testbench.flashA.flash] WRITE_ENABLE_OR_DISABLE_DURING_BUSY @521191345 ps :: Command Write Enable given during Read, Program or Erase busy period @ 521184681 ps.
*Denali* Error: Detected[testbench.flashA.flash] PROGRAM_LOAD_DURING_BUSY @521551201 ps :: Command Random Data Program given during Read, Program or Erase busy period @ 521544537 ps.
*Denali* Error: Detected[testbench.flashA.flash] PROGRAM_LOAD_DURING_BUSY @521557865 ps :: Command Random Data Program given during Read, Program or Erase busy period @ 521544537 ps.
*Denali* Error: Detected[testbench.flashA.flash] PROGRAM_LOAD_DURING_BUSY @521564529 ps :: Command Random Data Program given during Read, Program or Erase busy period @ 521544537 ps.
```

- Model flagged violations in AC timings for Controller Design

```
*Denali* Error: Memory Instance: testbench.flashA.flash Time: 453246701 ps; Hold Violation (tCLDX=1700 ps) of 200 ps on signal SIO5
*Denali* Error: Detected[testbench.flashA.flash] DATA_IN_HOLD_VIOLATION @453246701 ps :: Data In Hold Time violation of 200 ps @ 453246701 ps on SIO5 signal.

*Denali* Error: Memory Instance: testbench.flashA.flash Time: 453246701 ps; Hold Violation (tCLDX=1700 ps) of 200 ps on signal SIO6
*Denali* Error: Detected[testbench.flashA.flash] DATA_IN_HOLD_VIOLATION @453246701 ps :: Data In Hold Time violation of 200 ps @ 453246701 ps on SIO6 signal.

*Denali* Error: Memory Instance: testbench.flashA.flash Time: 453246701 ps; Hold Violation (tCLDX=1700 ps) of 200 ps on signal SIO7
```

Questions