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New Serial NAND Flash Octal Double Data Rate Feature

Its Verification Challenges and Solution for the Automotive Application Space

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***Abstract*— To meet the increasing bandwidth needs of the automotive industry, Serial NAND Flash memories have evolved from a 1-bit slow clock SPI interface to fast clock speeds over 2-bit and 4-bit derived SPI interfaces. Recently memory vendors added the Octal SPI interface to the Serial NAND Flash devices that enables 8-bit wide high bandwidth synchronous data transfers at manageable clock speeds. In several cases, the Octal SPI interface is combined with double data rate capabilities. The changes in device architecture and design have presented SoC validators with few options for rapid and effective verification of the feature within the high-demand and high-volume automotive application space. Automotive SoC and Flash Controller Silicon IP require a proven and reliable solution for the recent Octal DDR update to their controller. Cadence in partnership with suppliers of Octal Serial NAND including Winbond crafted a solution to add Octal DDR Verification support. The new Octal Serial NAND devices with Double Data Rate capability from Winbond offer up to 240MB/s continuous read data transfer rates at 120MHz clock speeds. This paper delves into the challenges faced by design validators and the implementation and usage details of the verification solution and demonstrates methods to verify Octal Serial NAND capabilities using a highly configurable user interface and Memory Model Advanced Verification (MMAV).**

Keywords*— *Octal; DDR; SPI; Serial; NAND; FLASH; Memory Model; VIP; Verification; Simulation

I. INTRODUCTION

NAND Flash has been in a constant battle to prove its competitive edge over the more prevalent NOR Flash and find a path to break into the code storage market. Delegated for use as off-chip data storage, and passed over because of the high bandwidth requirements for code fetch, the NAND Flash has spent decades improving its sluggard image.

Targeting data throughput, Winbond Electronics, a leading NAND Flash memory vendor, introduced a high-speed continuous/sequential read capability in the Serial NAND devices with no gaps at page and block boundaries. Coupled with an innovative bad block management scheme and bringing ECC on-chip, susceptibility to errors being another drawback of the NAND Flash devices, the continuous read capability improved the Serial NAND Flash performance significantly.

To meet the increasing bandwidth needs of the automotive industry today, Serial NAND Flash memories have evolved from a 1-bit slow clock SPI interface to fast clock speeds over 2-bit and 4-bit derived SPI interfaces. Most recently memory vendors, and Winbond specifically, added the Octal SPI interface to the Serial NAND Flash devices that enables 8-bit wide high bandwidth synchronous data transfers at manageable clock speeds. In several cases, the Octal SPI interface is combined with double data rate capabilities (Winbond W35* devices). The changes in device architecture and design have presented IP and SoC validators with limited options for rapid and effective verification of the feature within the high-demand and high-volume automotive application space. Automotive SoC and Flash Controller Silicon IP require a proven and reliable solution for the recent Octal DDR update to their controller designs.

II. APPLICATION

The Octal SPI interface notably introduces additional pinout. In this mode, the legacy SI and SO pins are reused as SIO0 and SIO1 respectively, the /WP pin is reused as SIO2, and new SIO3-SIO7 pins are added to the package. The Winbond Octal SPI Serial NAND Flash Memory with Double Data Rate capability can offer up to 240MB/s continuous read data transfer rates at 120MHz clock speeds. The Octal double data rate protocol uses a byte-wide synchronous bus interface on both the rising and the falling edge of the clock for command, address, and data. To support this capability, there is also a new Data Strobe output pin, DS, that acts in conjunction with the read data to signal to the host controller to latch data when

running at the maximum DDR frequencies. Figure 1 is an illustration of a typical pinout for the Octal SPI interface added to the Serial NAND Flash devices.

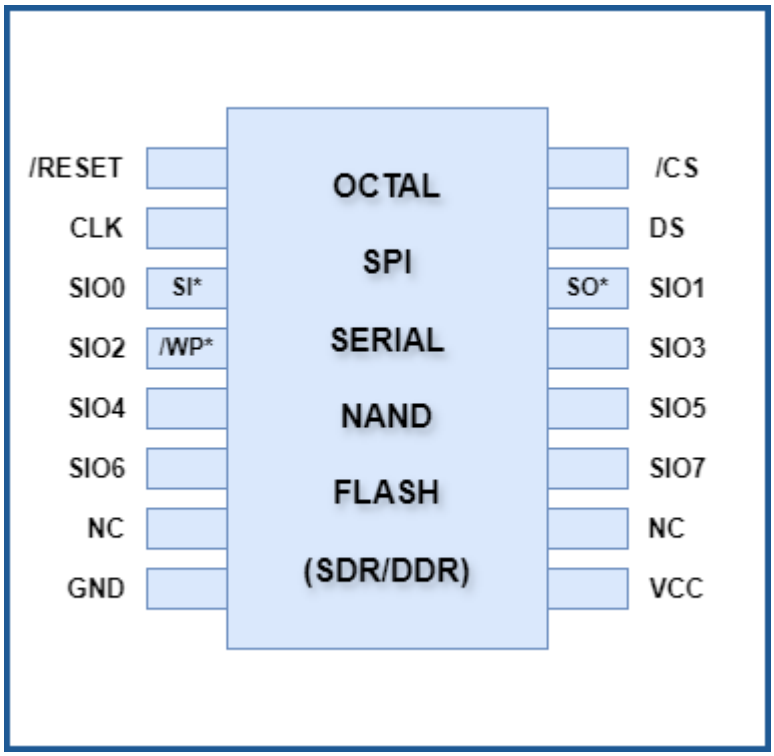

Figure 1 Typical Octal Serial NAND Device

With the Octal SPI DDR interface, the data transfers over the Serial NAND wires are adapted to utilize the 8-bit wide data bus now available, along with the data strobe transferring data on every clock edge.

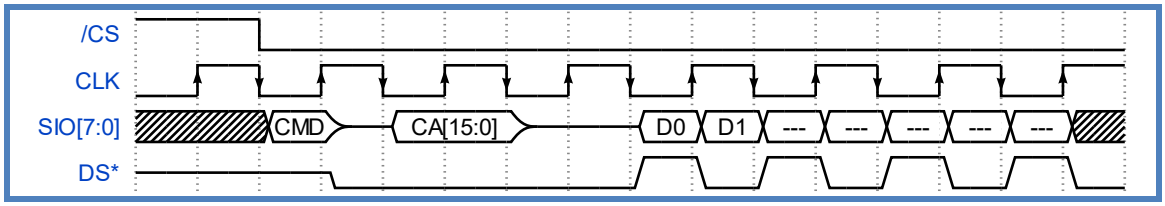

Figure 2 Octal SPI DDR NAND Data Transfer, the Data Strobe (DS*) is applicable for Read Command and driven by the Flash device to qualify the read data

The Octal SPI interface is intentionally pin compatible with the popular NOR Octal SPI specification but the existing OSPI verification memory models are NOR Flash devices and cannot model the SPI Serial NAND Flash architectures. The Serial NAND Flash verification memory models currently available in the market are x1, x2 or at best x4 Quad SPI Serial NAND devices. While these Verification IPs could model the SPI Serial NAND devices architecturally, they cannot address the x8 Octal interface.

Moreover, the true advantage of the Octal SPI Serial NAND device is not attainable without enabling the Double Data Rate capability and this feature does not exist for the SPI and Quad SPI Serial NAND devices. Even ignoring the DDR capability, a user cannot connect multiple copies of the SPI or Quad SPI Serial NAND devices to try and mimic an Octal device – the signaling is incompatible and such testing would be vastly inaccurate when the functional as well as AC/Timing parameters of actual Octal SPI Serial NAND Flash memory devices from vendors are considered.

Winbond's new Octal DDR capability, further combined with their high-speed Continuous Read capability enabling accesses across page and block boundaries, offers a fully integrated on-chip solution for high speed read. But it increases the complexity of the verification matrix.

III. MOTIVATION FOR SPI OCTAL NAND: WINBOND PERSPECTIVE

Emerging Automotive applications require high-density/high-performance Code Storage Flash. Most of these applications emerged in the past 5~10 years. Some examples include:

- Advanced FCM "Front Camera Module": The FCM comes with a capacity requirement of 1Gb~4Gb Flash code load with a maximum startup time limited to <10 seconds.
- DMS "Driver Monitor System": The recently approved requirements for the DMS (passed in Europe, others to follow) include a 1Gb~2Gb code load capacity with a startup time window of 5~10 seconds.
- ADAS Domain control for Surround View System and auto-parking applications have the most stringent requirements; with the rear camera application requiring a 1Gb~2Gb image load with a time window of < 2 seconds (NHTSA/USA).

Many of the automotive applications download code image from Flash to LPDDR4/LPDDR5x at startup.

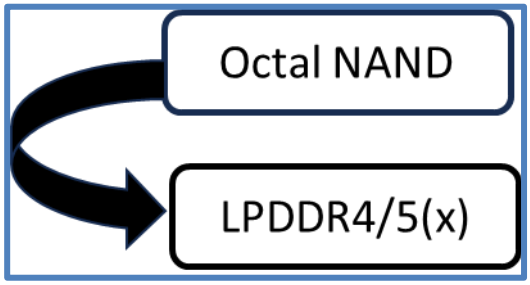

Figure 3 Typical code fetch flow in automotive applications today

Winbond introduced W35N01/02/04JW Octal NAND at 240MB/s to meet these requirements. Octal NAND at 240MB/s (120MHZ Octal DDR with DS "Data Strobe") can download a 2Gb image in a mere 1 second window. Comparatively, the currently available narrower device solutions, such as the Quad SPI NAND, can sustain data transfer rates of 80MB/s (80MHz Quad DDR), and can download 2Gb of Flash code image in 3 seconds. While this speed is decent, it is still too long for some applications. Fast startup time is important for either user experience (e.g. FCM and DMS) or regulatory requirement (e.g. rear camera).

The new solution of Octal NAND from Winbond Electronics addresses the whole eco-system: SoC hyperscalers, EDA tool providers, and applications SW developers. SoC partners have enabled or are in the process of enabling support for Octal NAND devices. EDA providers such as Cadence Design Systems have developed accurate timing models (covered in this paper) to help with SoC integration of Octal NAND controllers and components. SW support such as for low-level drivers, Linux and AUTOSAR, are becoming available for end customers in time. With many projects in production and under design, SPI Octal DDR NAND is rapidly proliferating.

IV. VERIFICATION CHALLENGES

At the outset, there are few alternative validation vehicles to verify the Octal DDR SPI Serial NAND Flash interface.

There are Octal SPI NOR Flash verification memory models available that can drive and sample the 8-bit Octal SPI interface, and in fact embody the very protocol interface that the Octal SPI Serial NAND Flash devices strived to emulate. However, the fundamental difference in the cell topology and memory addressing, coupled with the vast difference in the use-case for NOR Flash devices, makes the system level protocol incompatible with NAND Flash. Because the NOR Flash memory is primarily used as read/write direct program execution memory, given its low latency, row-parallel addressing and fast random-access for read, write and erase down to the byte-level granularity, the command structure is significantly different and more complicated for the NOR Flash than that for the NAND Flash device. Taking the Octal DDR mode fast read operation for both families of Flash, the signal protocol for the typical NOR Flash devices available in the market use 24 or 32 address bits, frequently split up as 3 bytes or 4 bytes of address phase. The Octal DDR NAND Flash uses a fixed 2-byte address phase and typically consuming less than the 16 bits supplied for addressing. Beyond the obvious dissimilarities in addressing, the command phase for NOR Flash devices can be 1 or 2 bytes long, whereas the NAND Flash with its limited command options is a fixed 1-byte command phase.

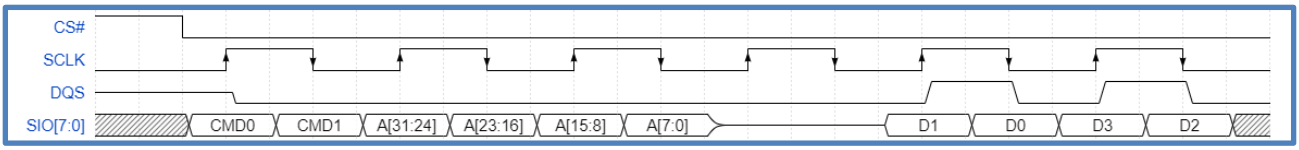

Figure 4 Timing waveform for typical Octal DDR SPI NOR Fast Read Operation

As an alternative to using NOR Flash models, validation efforts could opt to use a combination of the various 1-bit SPI Serial NAND Flash or 2-bit Dual SPI Serial NAND Flash memory models that are available with the goal of stitching together 8 of the 1-bit devices or 4 of the 2-bit devices in some fashion to mimic the 8-bit Octal interface. Another option was to use 2 instances of the 4-bit Quad SPI Serial NAND Flash memory models and connect them together to model the Octal interface. Functionally, the Quad SPI Serial NAND Flash datasheets included the Continuous Read Mode capability and, on the surface, could allow verifying the new Octal feature. While these could stand in for the Octal DDR SPI NAND devices at an architectural pinout level, the sets of models combined in these manners cannot approximate the Command-Address-Data instruction sequences for Octal DDR at the transactional level.

To take the case in hand of combining two Quad NAND parts together to achieve the 8 SIO data pins, we find that there are some options to combine the chip select and the system clock driven to the memory models. However, the 8 SIO pins when driven by a Memory Controller design that is operating in an Octal DDR mode would not arrive at the two Quad parts following the signaling protocol required to program Quad NAND Flash.

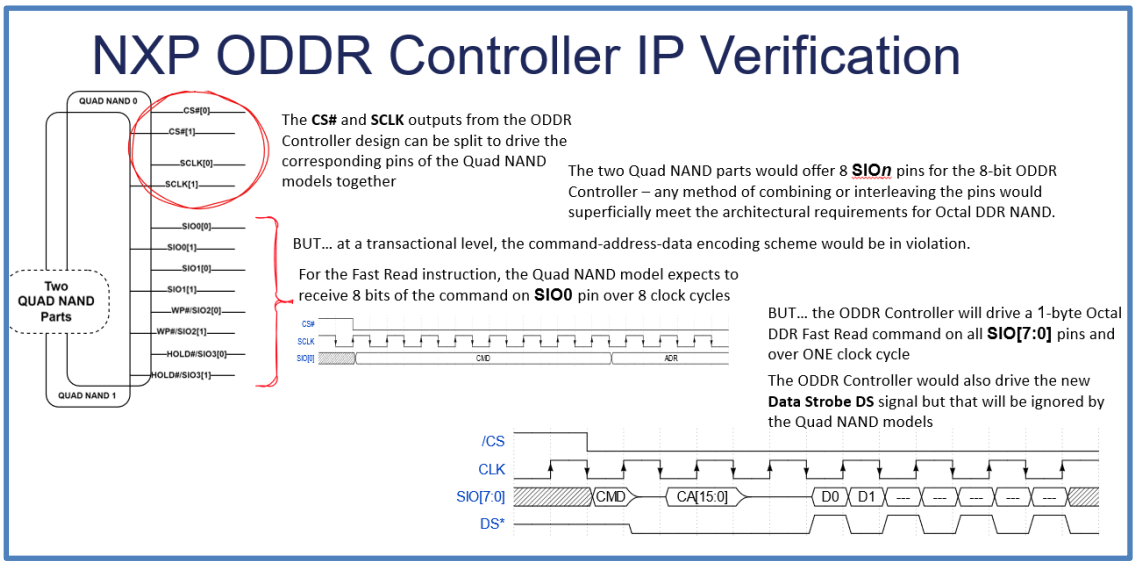

Figure 5 Mismatched design when combining two Quad NAND devices to tackle an Octal DDR NAND mode Controller

The disparity in the various timing parameters between the NOR Flash devices and NAND Flash devices, or alternatively between the Quad NAND Flash devices and the Octal NAND Flash devices, presents a final challenge to effectively verifying whether the Memory Controller design meets all device compliance requirements. The timing parameters are a critical aspect of memory interface verification. All memory devices have strict AC characteristics that set boundaries for the interface signal transitions within which the device can store and retrieve data reliably. If a Memory Controller drives the memory interface signals outside of the prescribed AC timing, then the device does not guarantee proper operation. Thus, it is essential for a Memory VIP to be able to accurately model these AC timings and clearly flag violations whenever the Memory Controller steps outside of the timing bounds – design bug. The timing parameters that define the AC characteristics of the devices include a large set – and they are not the same across the various model options mentioned above.

Below are a select few instances of discrepancies that, when taken in aggregate with all of the various AC timing parameters, can lead to severe oversights in validation:

- tSLCH: The parameter such as tSLCH defines the active setup time for the device chip select pin relative to its clock edge. This parameter is defined for all of the devices – NOR Flash, Quad NAND Flash, and the Octal DDR NAND Flash. But it is different between the NOR Flash devices and the NAND Flash devices. The chip select setup time is one of the most basic AC timing characteristics of any memory device. A memory model that does not check for

this timing requirement could allow a flagrantly offending Memory Controller design to go into manufacturing only to then fail on post-silicon test cards.

- t_{RD2}: The t_{RD2} parameter does not exist for the NOR Flash devices. It is unique to the NAND Flash devices. This difference is fundamental – this parameter defines the time to load a page-size worth of data during a continuous/sequential read operation. The NOR Flash, given its row parallel architecture and ability to support direct addressability, does not include page sized operations and instead specifies array commands. Though this parameter is common to both the Quad and the Octal DDR NAND Flash, it is assigned unique values between the two types of Serial NAND devices, and can lead to significant deviation in validation if the memory model fails to reflect this AC timing in its responses to a Memory Controller design.
- t_{DVW}: This is a parameter that exists only for the Octal DDR SPI NAND device. It specifically defines the window of time when the output data from the memory device is valid. It does not exist for either the NOR Flash devices or the Quad NAND Flash devices. Any Memory Controller design that expects to operate compatibly with the Octal DDR SPI NAND Flash, must ensure precise compliance with this parameter if it is to correctly record the serial output from the device. A model that does not adhere to this timing, and further does not enforce this requirement on the Memory Controller design during simulation, can lead to false positive results for the validation efforts.

Similar analysis of the exhaustive list of AC timing parameters among the various NOR and NAND Flash devices is left to the reader's discretion. The authors of this paper assert that selecting alternative verification approaches prior to implementing the final solution derived herein have proven to be deficient validation vehicles.

V. Verification Solution

This paper describes the precise enhancement to the implementation of a SPI Serial NAND Flash memory verification reuse model that supports this new Octal SPI DDR capability which can be enabled in the memory model with a new configuration parameter. There is an additional configuration parameter that enables the memory model support for a volatile configuration register that allows programming the correct Octal transfer modes. The Octal DDR SPI mode can be configured with or without a data strobe accompanying the read data. The feature includes support for vendor specific command flows, that allows for the selection of the data strobe enable as described in vendor datasheets. All new command specifications as described in vendor datasheets are supported in the Octal DDR SPI mode. The command format follows the C-A-D (Command-Address-Data) transactional sequence as specified in vendor datasheets. The memory model described performs accurate checking of all AC/Timing parameters and is fully backward compatible, as specified in vendor datasheets. Depending on the configuration programmed by user, the model can operate in 1-bit SPI Single Data Rate (SDR) mode, 1-bit SPI Double Data Rate (DDR) mode, 8-bit Octal SPI SDR mode and 8-bit Octal SPI DDR mode.

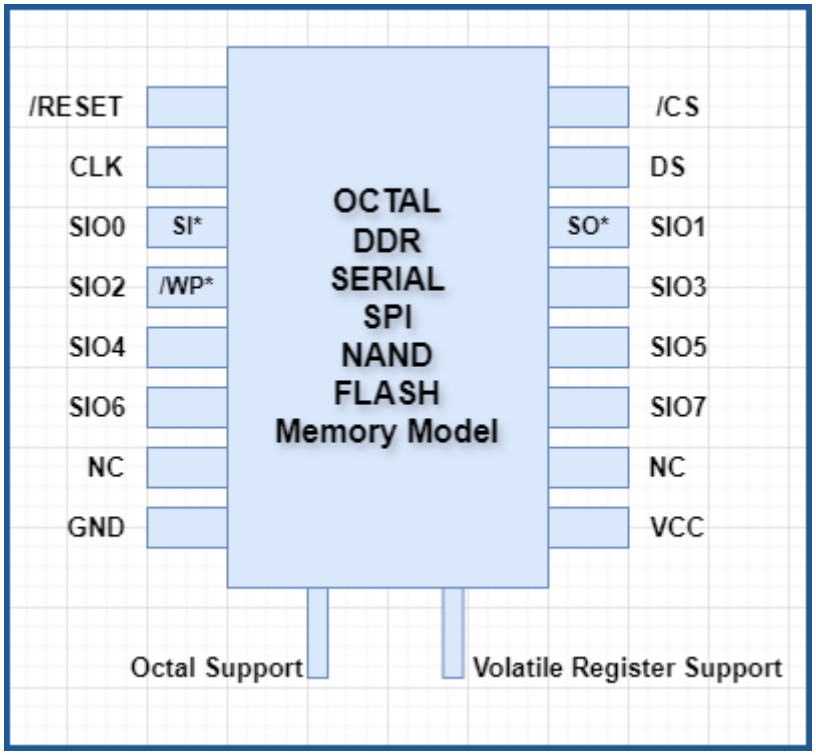

Figure 6 Memory Model for the Octal DDR SPI Serial NAND Flash

The key implementation decision that allowed rapid development of the model while maintaining a path to full backward compatibility was to use a modularized clock edge counter design. Modeling the Octal NAND device required multiple counters that could independently count rising edges of the clock input, falling edges of the clock input and both rising and falling edges of the clock input. These counters are then used to orthogonally detect data on the SIO[0] pin, on the 7-bit wide SIO[7:1] pins, or on the byte-wide SIO[7:0] bus, depending on which instruction is being processed and what phase of the transaction is being processed.

This requirement is most pronounced when processing the Fast Read instruction in either the SDR or Octal DDR mode. In SDR mode, the Fast Read instruction's byte-sized command encoding is received on the SIO[0] pin over 8 cycles of the rising edge of the clock, then the 16-bit address is received again on the SIO[0] pin but this time at a dual-data-rate over the rising and falling edges of the clock, and finally each byte of data is transmitted on the combined { SIO[0] , SIO[7:1] } pins again at a dual-data-rate over the rising and falling edges of the clock.

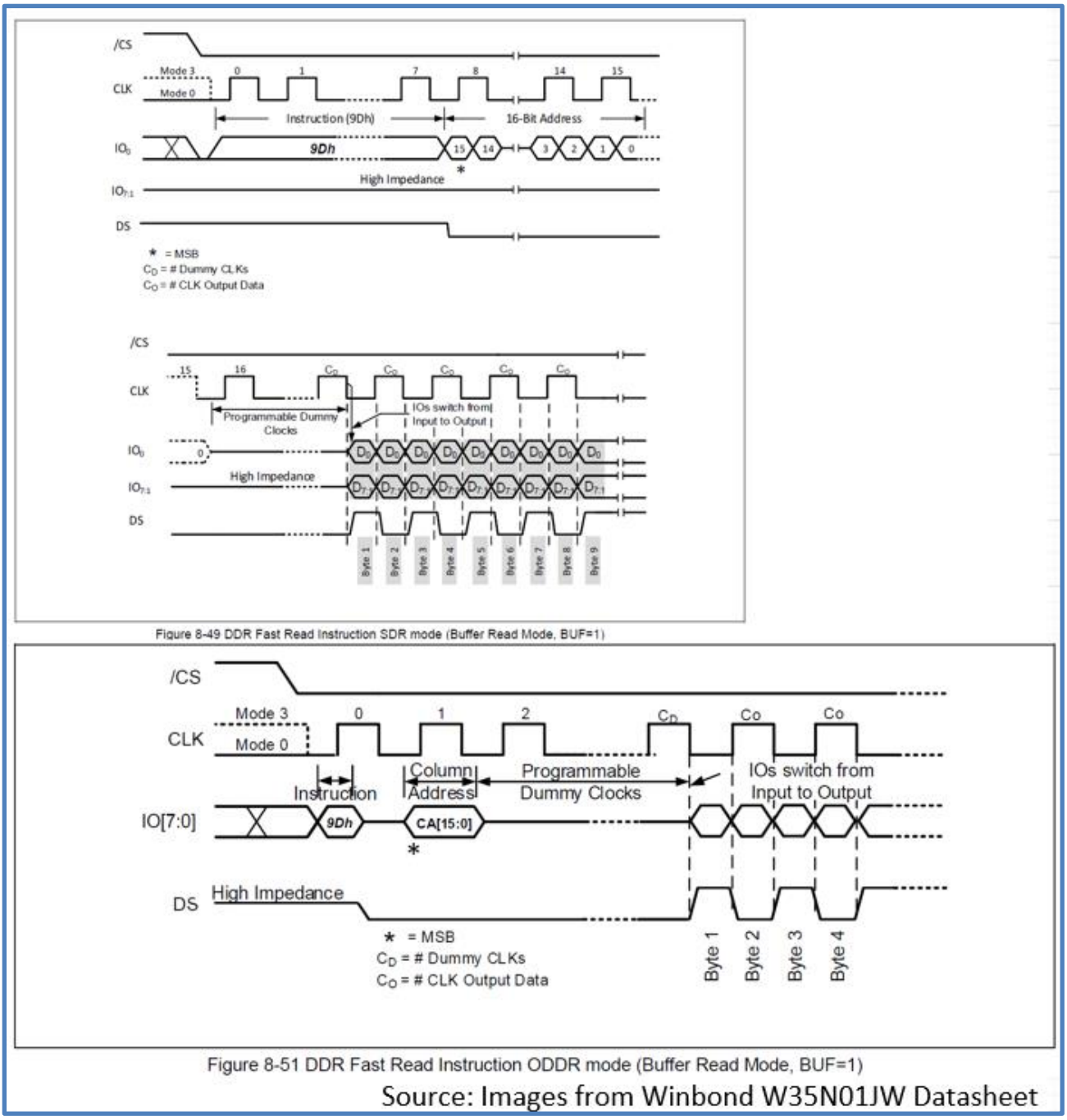

Figure 7 Waveform diagrams of the Fast Read instruction processing in SDR and Octal DDR modes

In Octal DDR mode, by contrast, the complete byte-size command encoding for the Fast Read instruction is received on the SIO0[7:0] bus at a dual-data-rate over the rising edge of the clock, the 16-bit address is received again at a dual-data-rate also on the SIO[7:0] bus over both the rising edge and falling edge of the clock, and each byte of data is transmitted at a dual-data-rate on the SIO[7:0] bus over both rising edge and falling edge of the clock.

The fully modularized implementation of the counters and functional independence from the data detection logic allows the memory model to not only exhibit efficient instruction processing for the Fast Read command, but at the same time enable a mix-and-match capability for the developer to go on and implement every other instruction processing flow that is defined for the memory device. The final implementation of the memory model includes a set of statically initialized instances of the counters, with independent data flow logic that is able to dynamically attach to the relevant counter depending on the transaction phase of its state machine as it processes each instruction in the pipeline. With code duplication

eliminated and streamlined, the overall effort to test the model before production release was simplified and was possible to complete in a short time to meet NXP's project commitments in a timely fashion.

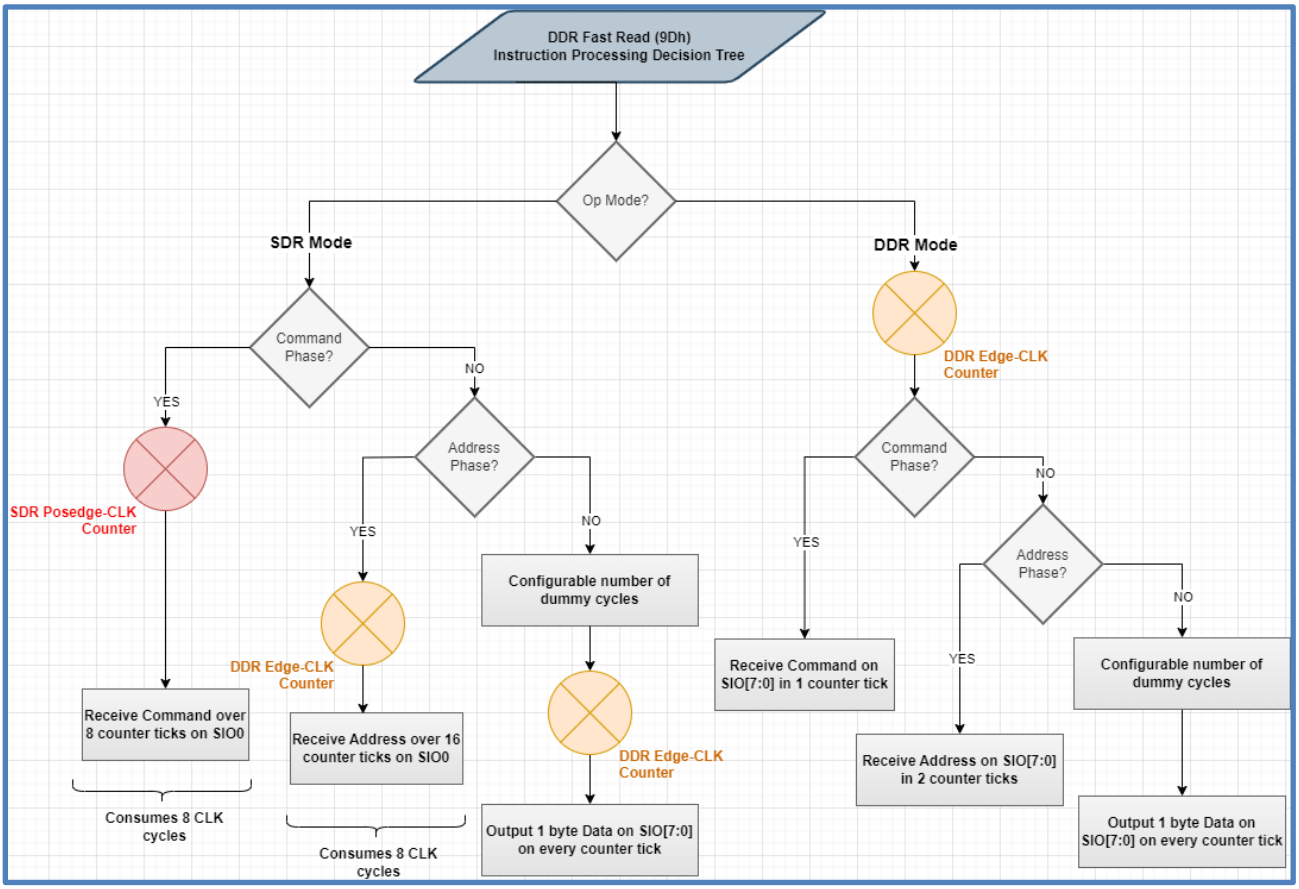

Figure 8 Data flow diagram for the DDR Fast Read (09Dh) instruction processing in the memory model

VI. RESULTS

The Cadence Octal DDR SPI Serial NAND Flash Memory Model has been adopted by the NXP Controller IP Design Team as the primary deliverable sign-off verification vehicle. The fast turnaround of the Verification IP allowed NXP design verification team to rapidly develop an exhaustive block level testbench around the NAND Flash Controller IP and achieve tape-out qualification for the new design against tight project deadline commitments.

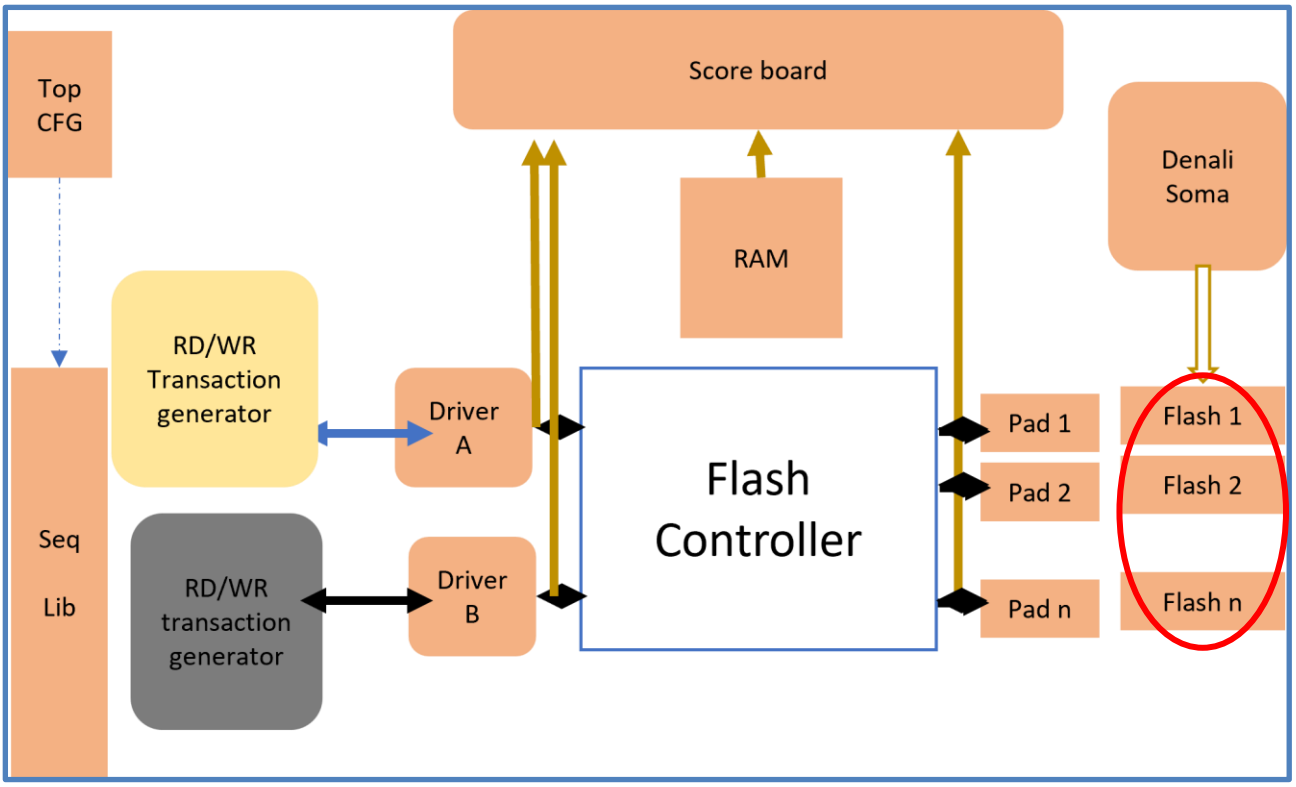

Figure 9 NXP Flash Controller IP block level testbench with the Octal DDR SPI NAND Flash Memory Model

The SPI NAND Memory Model was integrated into the test environment seamlessly. The model supports a full range of different density grades. The command processing can accurately adapt to the current density grade. The modular and dynamic implementation of the data path processing made it easy and efficient to add an extensive set of protocol checks and error injection capabilities. For instance, checks for incorrect register configuration by the Controller IP, specifically for registers which require specific values dependent on different ranges of operational frequencies. Also included is the ability for the Memory Model to exercise invalid data regions based on the data valid window (tDVW) timer; the memory model drove valid data during the valid window, and X's outside the window. Finally, the modularized implementation made it easy to implement the complete slew of checks for the AC timings of the signals driven by the Controller design IP.

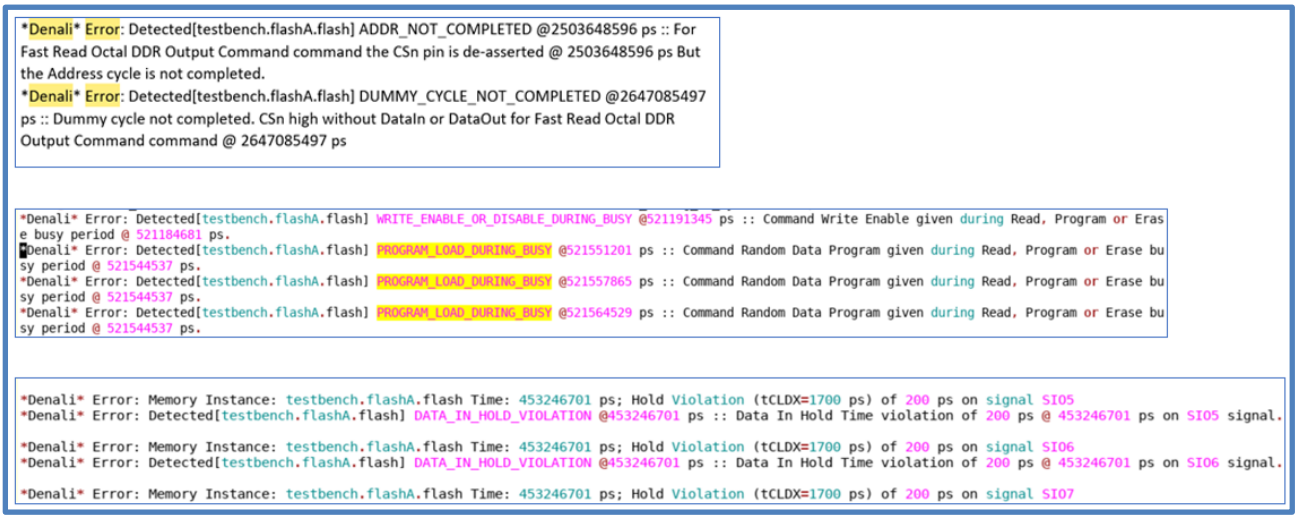

Figure 10 Protocol errors flagged by the Octal DDR SPI NAND Flash Memory Model during NXP test simulation

VII. Conclusion

State-of-the-art Serial NOR Flash as well as Serial NAND Flash verification models exist today that offer viable solutions for 1-bit SPI, 2-bit Dual SPI or 4-bit Quad SPI Serial NOR and NAND Flash devices. Not all of the models offer accurate

AC/Timing parameter support for Octal DDR SPI Serial Flash. No verification model exists today that offers support for the Octal DDR mode specifically or can be interconnected in any hierarchical manner to model the true Serial Octal DDR SPI NAND device. The reuse memory model presented in this paper offers an advanced and highly flexible memory verification methodology and addresses the specific verification requirements for the Octal DDR SPI Serial NAND Flash memory devices. It is successfully used at NXP to validate their Flash Controller IP against an exhaustive array of Winbond Octal DDR NAND device models. The solution has been identified as the only acceptable tape-out sign-off criteria by NXP.

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