2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION JAPAN

Solving Memory Subsystem Configurations Challenge with SV-Rand and Auto-Config Flow

Kaushal Vala, Krunal Kapadiya, Joseph Bauer, Shyam Sharma, Dharini SubashChandran, Ritesh Desai, Pooja Patel, Vatsal Patel

Cadence Design Systems

cadence

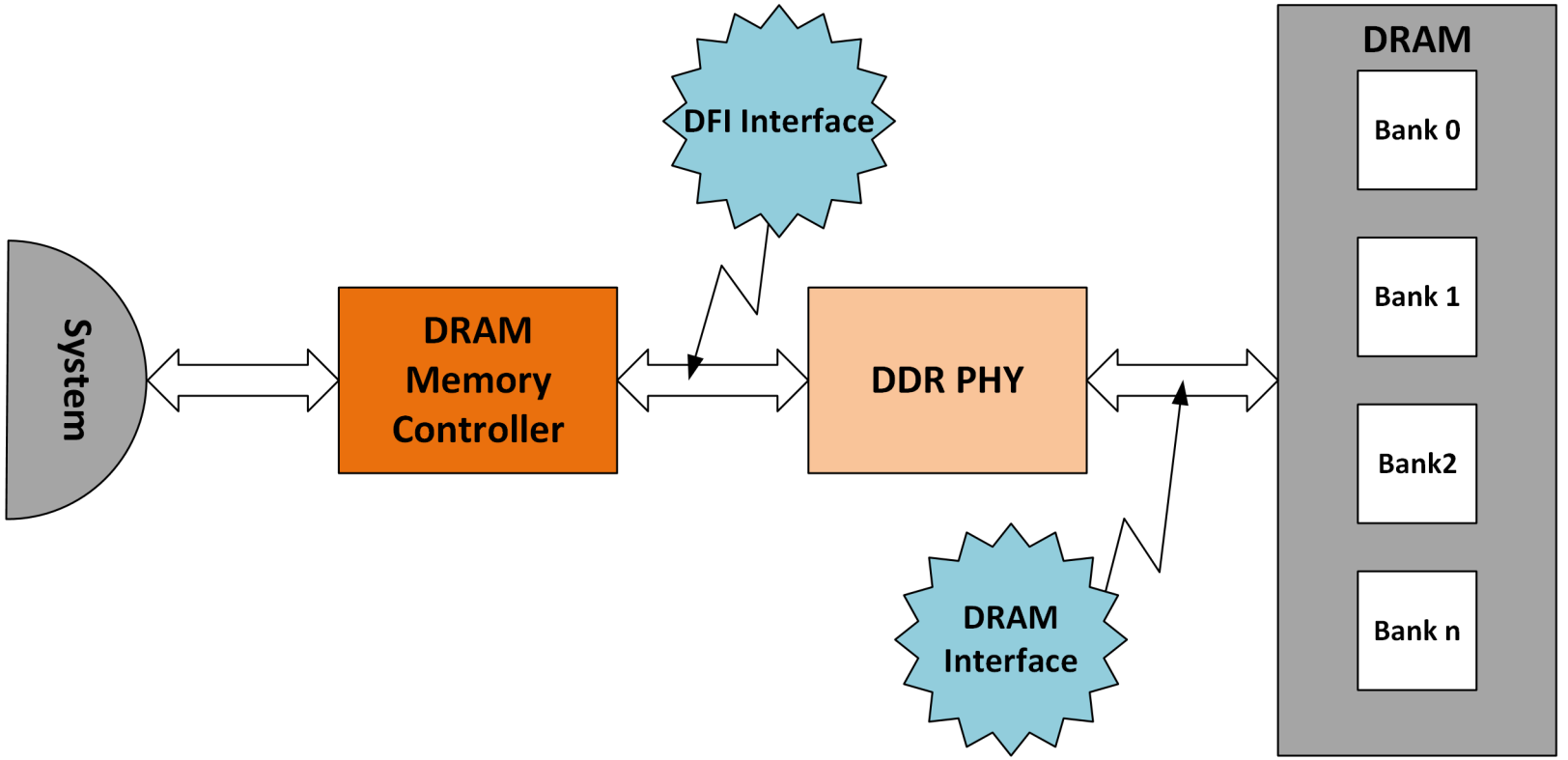
accellera SYSTEMS INITIATIVE

Agenda

- What is Memory Subsystem?
- Challenge
- Evolved SVRAND Solution
- Real Memory Part Configurability
- eMemory Parts Compliance Checklist
- Comparison of Flows
- Relational Database to SV Constraint
- SVRAND Flow
- Auto Configuration Layer
- Competitive Advantage
- Innovative Memory Technology
- Questions

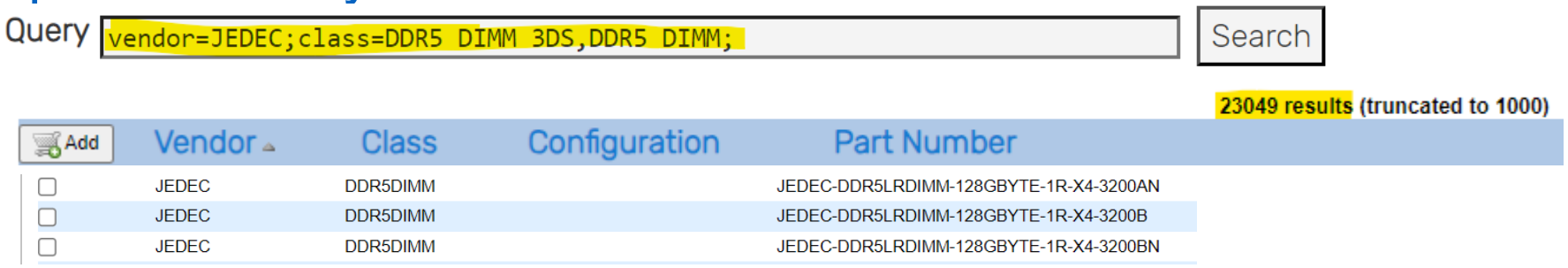
What is Memory Subsystem?

Simple DRAM Memory Subsystem



Challenge

- Protocol Compatibility to Thousands of Parts
  - https://ememory.cadence.com



MAINTANENCE

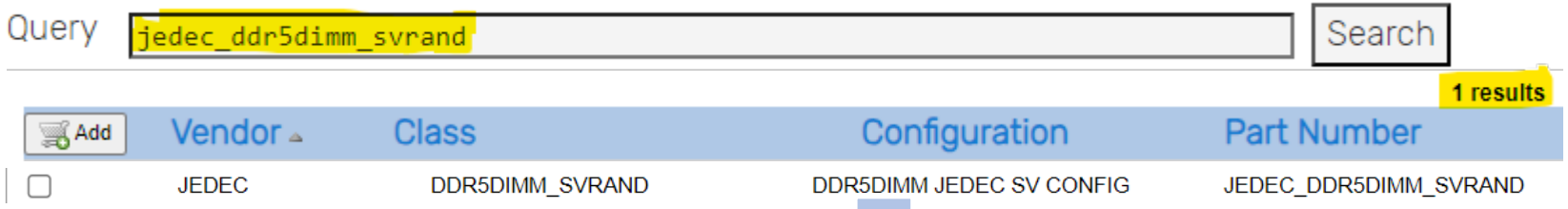
23049 results

COVERAGE Missing

15 Speeds X 5 Densities X 5 Stack heights [1,2,4,8,16 H] X 3 Data Widths [4, 8, 16] X 2 DIMM Widths [72/80 bits] X 4 DIMM Types [U/R/LR/MR-DIMM] X 2 Rank Layouts

Evolved SVRAND Solution

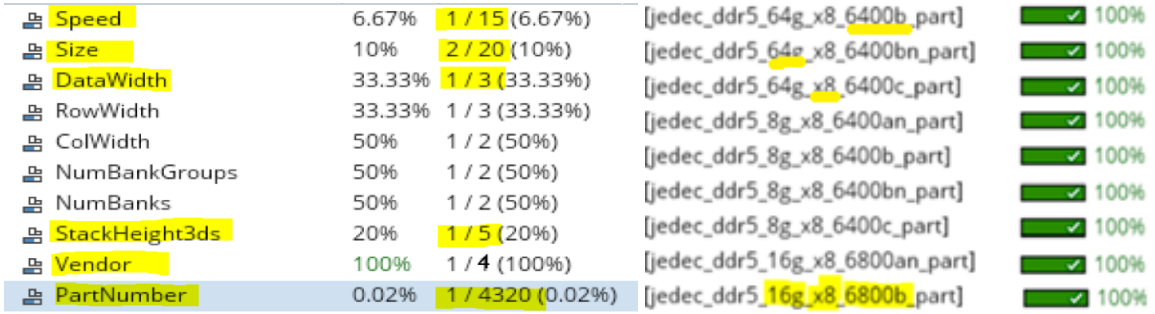
- Protocol Compatibility to Parts
  - https://ememory.cadence.com/pn/jedec_ddr5dimm_svrand



MAINTANENCE

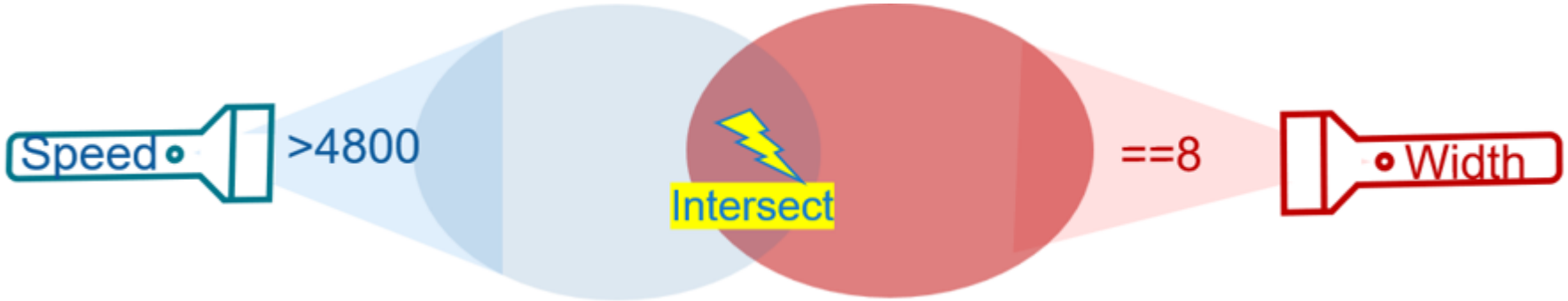
1 results

COVERAGE



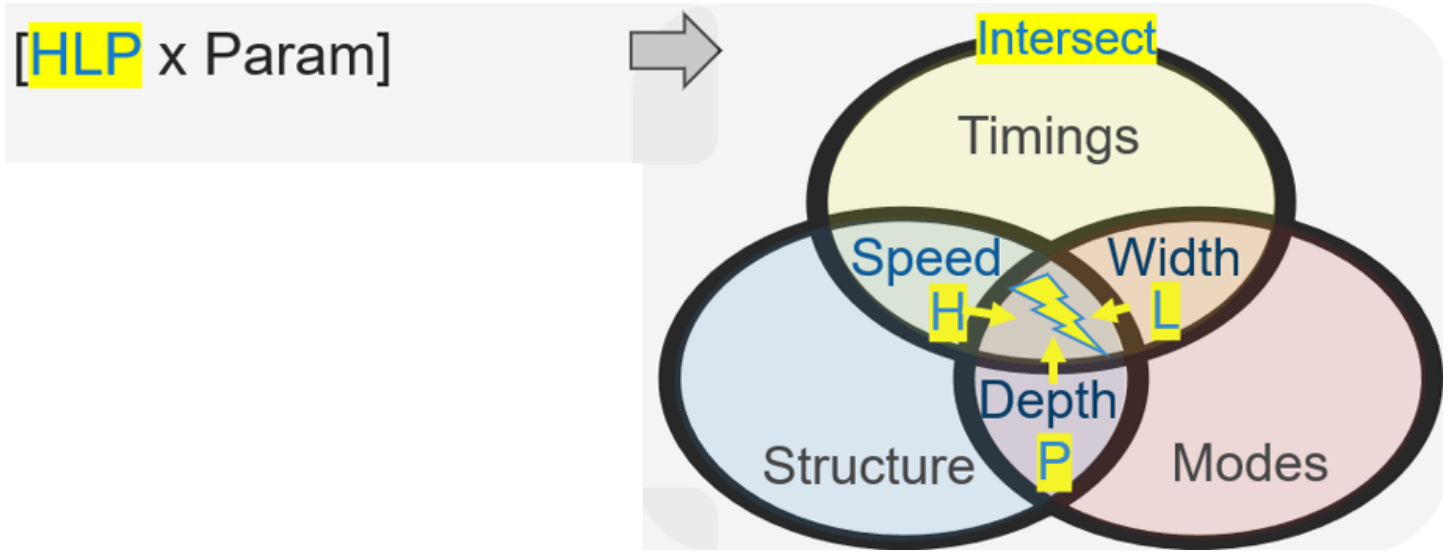
Real Memory Part Configurability

- SoC memory slot configurable to any real memory part
  - Fast, full hierarchy, even distribution resolution
  - Runtime memory part select config and create
  - Easy application scoping to supported speeds, sizes, types, etc.
  - Iterate feature scenarios over part types and/or parts



Real Memory Part Configurability Cont.

- All eMemory Parts in One Class : Native SystemVerilog Constraint set
  - Not a massive chunky queue of parts
  - Resolves to real parts Only
  - Cadence validated AND coverage verifiable eMemory parts match
  - All parameters, value sets, interdependencies, and hierarchy



eMemory Parts Compliance Checklist

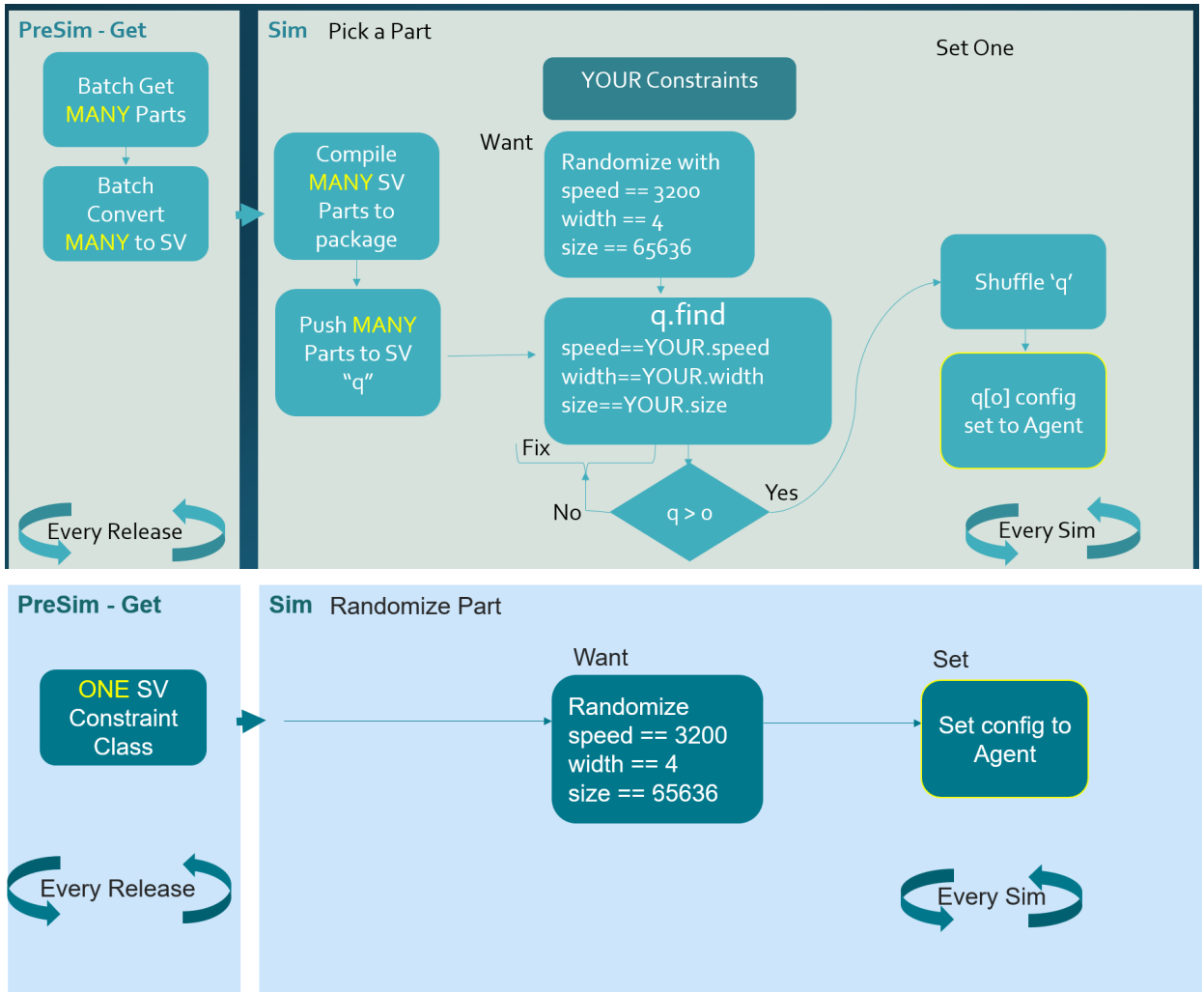
- Compliance compatibility - **Verifiable** to latest eMemory part sets
  - **Coverage**
    - Memory parts and High-Level parameters checklist
  - **Comprehensive**
    - Daily maintained and updated notifications
    - eMemory hosted
  - **Validated**
    - Validated eMemory match
    - All resolved configuration combination

Comparison of Flows

Query Part Select

- Versus -

SVRAND Generate



Relational Database to SV Constraint

- Relational metadata: .yaml file
  - Timing parameter
  - Timing value
  - High-Level Parameters: speed and width
- SV constraint equivalent: .sv file
  - Solve **order** constraints
  - Valid **value set** constraints
  - Legal **implication** constraints

YAML Metadata

```
  tfaw:
    8 ns:
    - speed: [7600]          HLPs these
      width: ['4', '8']      and those
    9 ns:
    - speed: [8000]          HLPs these
      width: ['4', '8']      and those
..
```

SV Constraints

```
constraint C_tfaw_valid { tfaw inside { 8,  9, .. }; }

constraint C_tfaw_legal__rate_width1 {
 ( ( rate == 7600 ) && ( width == 8 )) -> ( tfaw == 8 );
}

.. Similarly for other values ..
```

SVRAND Flow: Specific part selection

- Using constrain all high-level parameters
  - Input: DIMM selection randomized on all high-level parameters

```
JEDEC_RandSettings = new();
assert( JEDEC_RandSettings.randomize() with {
                                        kind == lrdimm;
                                        density == 128;
                                        prank == 2;
                                        width == 4;
                                        lrank == 1; // non-3ds
                                        rate == an3200;
                                        eccType == withEcc;
                                    } );
$cast( randSettings, JEDEC_RandSettings);
```

  - Output: Resolves single DIMM part

```
jedec_ddr5lrdimm_128gbyte_2r_x4_3200c
```

Auto Configuration Layer

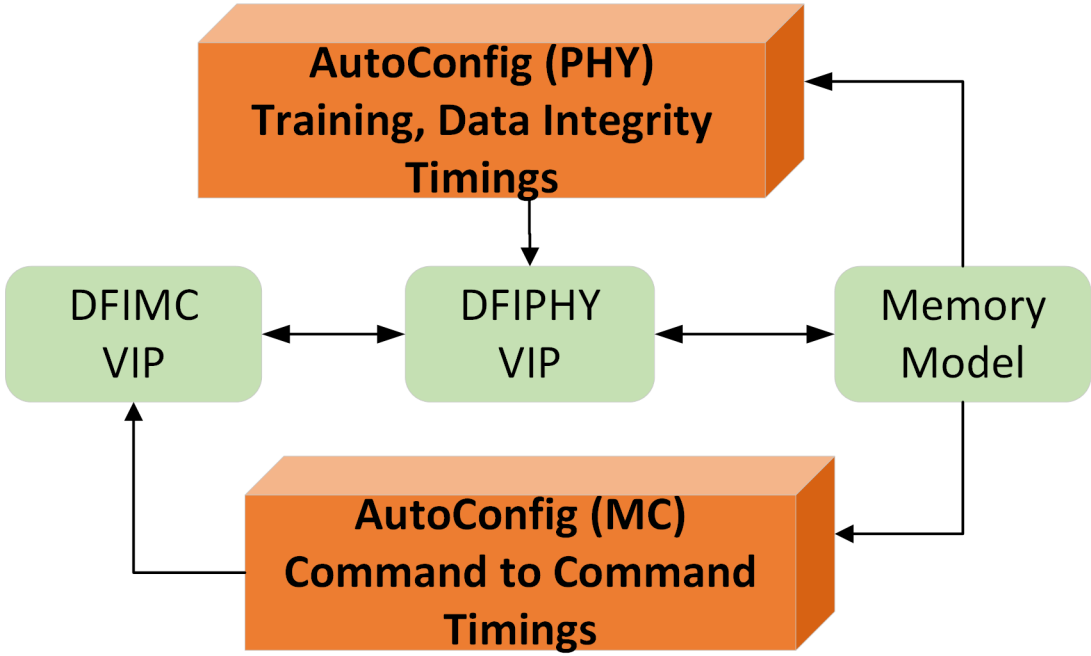
How it Works:

DFIMC VIP (Memory Controller):

- Command to Command Delay for any memory device
- VIP internally calculates and converts timings into DFI clock terms

DFIPHY VIP (PHY):

- Delays during training
- Setup/Hold timing



Competitive Advantage

- Proven 'SVRAND = eMemory'
- All parts eMemory matched and sim-validated with Model
- Effective, optimized, native, user-friendly way to verify thousands of valid configurations
- Overall configuration tasks cut by 30%
- Simplified maintenance for EDA provider and SoC developer
- Part compatibility coverage closure measured
- Widely adopted in industry
- Auto-Configuration technique reduces efforts up to 70% with 100% accuracy
- Generates minimum command delays in an exhaustive subsystem env

Innovative Memory Technology

- Differentiated!
  - Closure with speed, flexibility, confidence
- Deployed!
  - Top tier customers
  - Memory subsystem types
  - Transforms/applications
- Praises!
  - “Shorted configuration tasks”
  - “Glad to have SVRAND”
  - “Old fashioned method really hard”
  - “Super easy integration!!”
  - “I like the random config”

Questions