PSS beyond reuse: Streamlining the DV effort for a low power multi-core SOC

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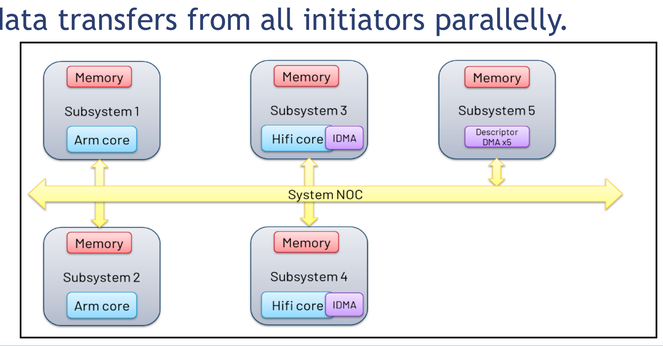
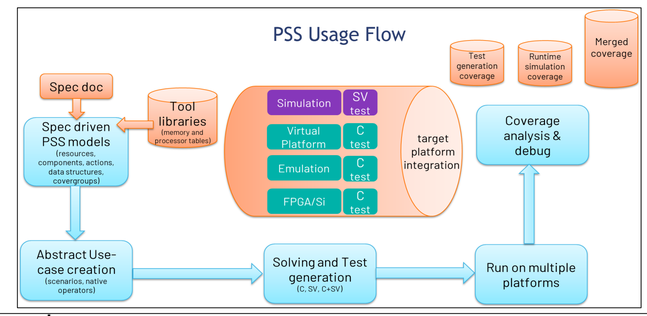
Problem Statement/Introduction

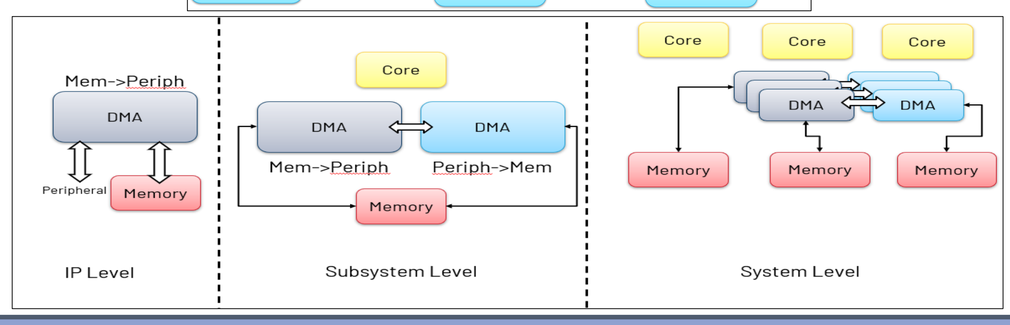
- Creating sufficient tests to verify today's complex designs is a key verification challenge, and this challenge is present from IP block-level verification all the way to SoC verification.
- In cases of multi core designs, the tests must be multi-threaded to handle the various core operations as well as drive stimulus to the UVM based testbenches.
- This work shows how PSS enables reusable test intent for power-aware multi-core SoCs, while accelerating DV through automated test generation, efficient regression, and detection of corner-case bugs in concurrent scenarios.
- The SoC features 4 processor cores—2 ARM and 2 Cadence Tensilica cores—along with multiple Descriptor DMA Engines. All cores and DMAs serve as the primary data movers in the system. There is a critical need to stress-test the environment with multiple concurrent data transfers from all initiators parallelly.



Proposed Methodology/Advantages

- System Methodology Library (SML) enables us to use CSV files to capture the processor and memory information of the system.
- The PSS generated tests at IP and subsystem levels are ported to system level, enabling complete reuse of the test intent without duplication of effort.



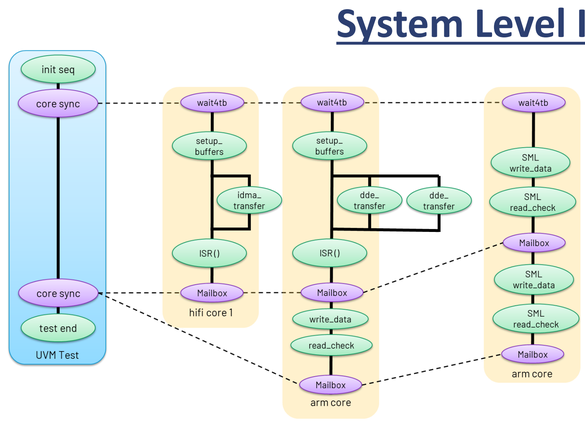


Modeling Details

The DMA IP supports multiple modes of transfer and sizes.

- Modes of transfer – Single mode, descriptor array, descriptor list, auto mode, trigger mode, descriptor on demand mode.
- Transfer size – 1 to 32 bytes
- Data array dimensions – 1D and 2D, with configurable array indices and increments on source and destination memories.
- Interrupts support in PSS model.
- A self-checker verifies DMA/memory transfers by comparing expected and actual data at the destination, reporting pass/fail
    - This helps offload score-boarding and shifts the verification effort from traditional DV to a PSS-driven model

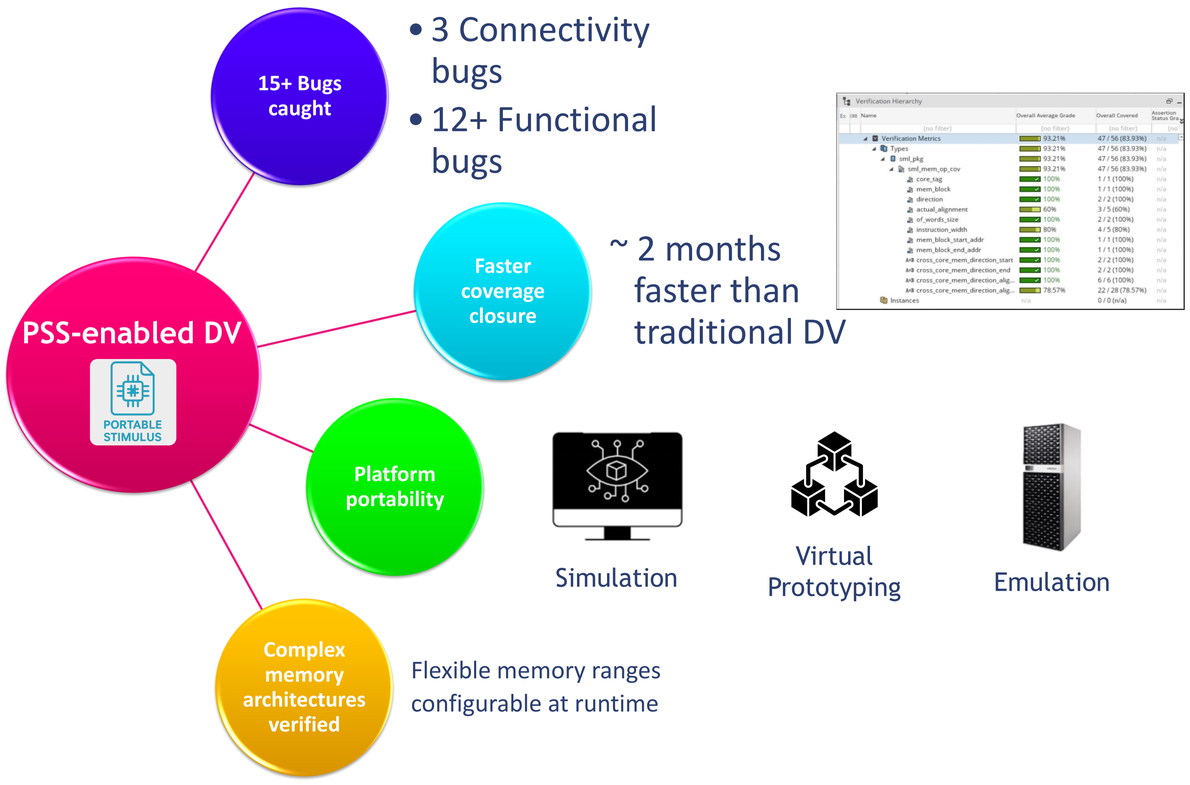
System Level Implementation




```
table:dma_reg_config
@package:dma_config_pkg, @size_const:NUM_DMA_DESC, @struct: dma_reg_config_s
#desc_inst,  #msize,  #psize, #xindex, #xincr, #yindex, #yincr
0,           1,       0,      5,       4,       0,       0
1,           2,       0,      8,       8,       2,       -3
2,           3,       0,      9,       16,      4,       -2
```

- Shown above is a system level scenario that is generated through PSS which exercises 3 cores in the system and multiple DMA engines.
- This truly captures the practical advantages of PSS in creating multi-threaded scenarios and handling complex sequencing of actions through these cores and DMAs.
- For generating multiple configurations of a scenario, test tables offer significant help.
    - Example would be to create multiple tests different of transfer size parameters, 1D and 2D array parameters, the PSS solver tool offers a robust CSV file input mechanism through which we can create multiple scenarios

Results



Conclusion

- PSS has helped us shorten the design verification cycle, with an estimated reduction of 50% of time spent in test generation for VP, FPGA and Emulation platforms.
- Streamlined DV with automated test-gen, coverage ranking, optimized regression list and run at real-time.
- Complex tests scenarios in designs with multiple cores has been made simple.
- Coverage with PSS enables left-shift metrics driven verification and regression optimization.
- Randomization of attributes is offloaded to the solver engine, thereby reducing the effort and time on the run time simulator.
- Future roadmap includes
    - Ongoing effort to model the low power scenarios in PSS
    - Post-Silicon adoption of PSS to generate scenarios for the tester
    - Working with the software team to align on a common driver library reusable through PSS.

REFERENCES

"Tackling the verification complexities of a processor subsystem through Portable stimulus" previous work presented at DVCON India 2023

"A Novel Approach for HW/SW Co-Verification: Leveraging PSS to Orchestrate UVM and C Tests" DVCON Europe 2024