

Problem Statement

Memory interfaces, including DDR, LPDDR, and HBM are becoming ubiquitous in SOCs

Analog features and training are becoming increasingly important for memory devices as

- I/O speeds go up to increase performance
- Interface voltage goes down to save power
- Multiple voltage rails are used to save power

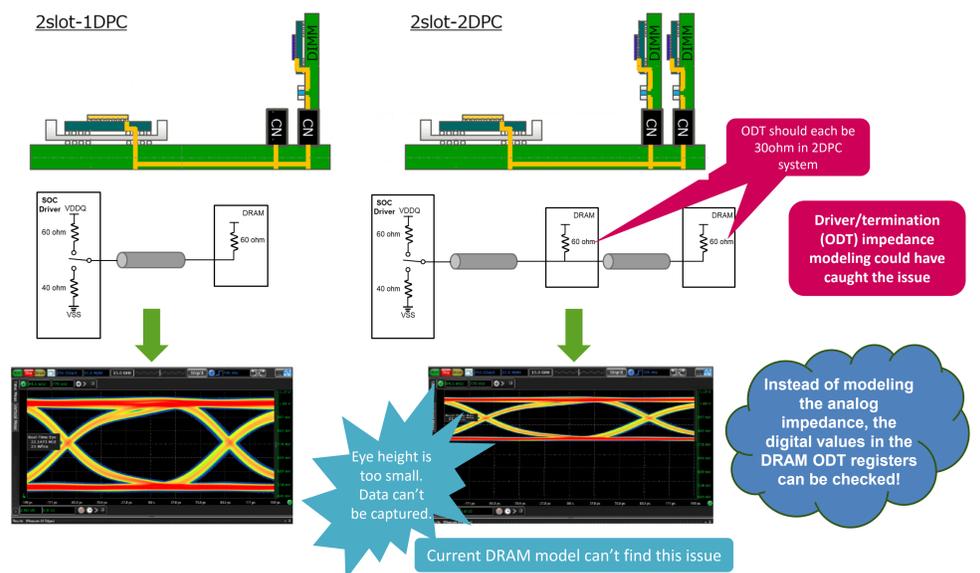
Need for Digital modeling of Analog features

- True analog modeling is very resource intensive
- Typical verification objective for these features is to test a digital state machine/algorithm
- Allows catching design bugs early in design cycle

DDR IP needs these features for

- Improved robustness of leading-edge designs
- Earlier detection/prevention of certain customer design issues (see example to the right)

Example customer design issue that needs analog verification



Complexity of Analog modeling in Digital simulation

Specification doesn't define the analog behavior accurately.

- Device characterization needs more information than what is captured in Specification.

Real device analog functionality is complex to model.

HDLs provide limited analog modeling support.

- Languages like SystemVerilog/systemC have limited modeling features for analog

Memory Models are C/C++ Based Verification IPs.

- Use VPI/DPI standard
- No direct SystemVerilog design access

Analog feature support added in Digital memory models

Drift modeling

- Read Data/Strobes can drift over time
- Define knobs to control randomization
- Allow different randomization patterns
- Beat to Beat, Command to Command and timing window constraints

Data eye modeling

- Use Setup/Hold time to define the data Eye.
- Check for data valid/transition regions

Dynamic Voltage and Frequency Scaling

- Define the voltage rail switch sequence.
- Capture the current rail value as a feature.
- Check for switch timings and allowed signal values during transition.

DFE

- Model typically used 2-tap or 4-tap DFE
- Capture the last N number of signal values to define the Data valid window
- Allow an N dimensional array for Setup/Hold/Pulse timings

VREF

- Capture Voltage reference level defined in mode registers to automatically adjust Setup/Hold/Pulse timings

Temperature and derating

- Model mode register temperature controls
- Allow for Refresh, and core timing parameter derating

PVT analog features

Drive and Registers

- Signal strength modeling
 - Model the System Verilog supported signal strength
 - Support signal resolution per SV Language Reference Manual for internal signals
 - Support scheduling and sampling of both signal logic and strength.
- Target and Non-Target On-Die Termination
 - Check Mode Register impedance settings
 - ODT on and off timings for Data phase for both target and non-target DRAMs
- ZQ Calibration
 - Calibration sequence and chronological order for start/stop and latch
 - Calibration timings
 - Training

Optimizations

- Identify power saving opportunities
 - Clocks toggling when in clock stop mode
 - CA bus changing when CS is not asserted
 - SR → <No Read/Write/MR access> → SR
 - Accessing only one PS for a long time
 - No activity but DRAM is in Idle (not SR) state

Analog features used by Cadence DDR IPs

- Device temperature and derating
- ZQ Calibration
- Target and Non-Target ODT checks
- DVFS modes
- Signal Strength for pulled up/down signals
- Read output randomization and drift

Conclusion

Verification of Analog features is a requirement for latest DDR PHY and MC IPs

DDR Verification IPs have developed modeling for a whole suite of analog features over the last few years

- protocols include LPDDR6/5X/5, DDR5 SDRAM/RCD/DB, HBM4/3, etc

Future enhancements include

- Extend these features to memory sub-system level and track analog settings across multiple device instances.
- Add additional power and scheduling optimizations.
- Provide more feedback on analog trainings like offset calibration etc
- Model temperature gradients.

REFERENCES

1. JEDEC. (2024). DDR5 SDRAM (JESD79-5C ed.). <https://www.jedec.org/standards-documents/docs/jesd79-5c>
2. JEDEC. (2023). LOW POWER DOUBLE DATA RATE (LPDDR) 5/5X (JESD209-5C ed.). https://www.jedec.org/document_search?search_api_views_fulltext=lpddr5