Novel Use of Symbolic Map Based Constraints for Synchronization Block Verification Using Formal Methods

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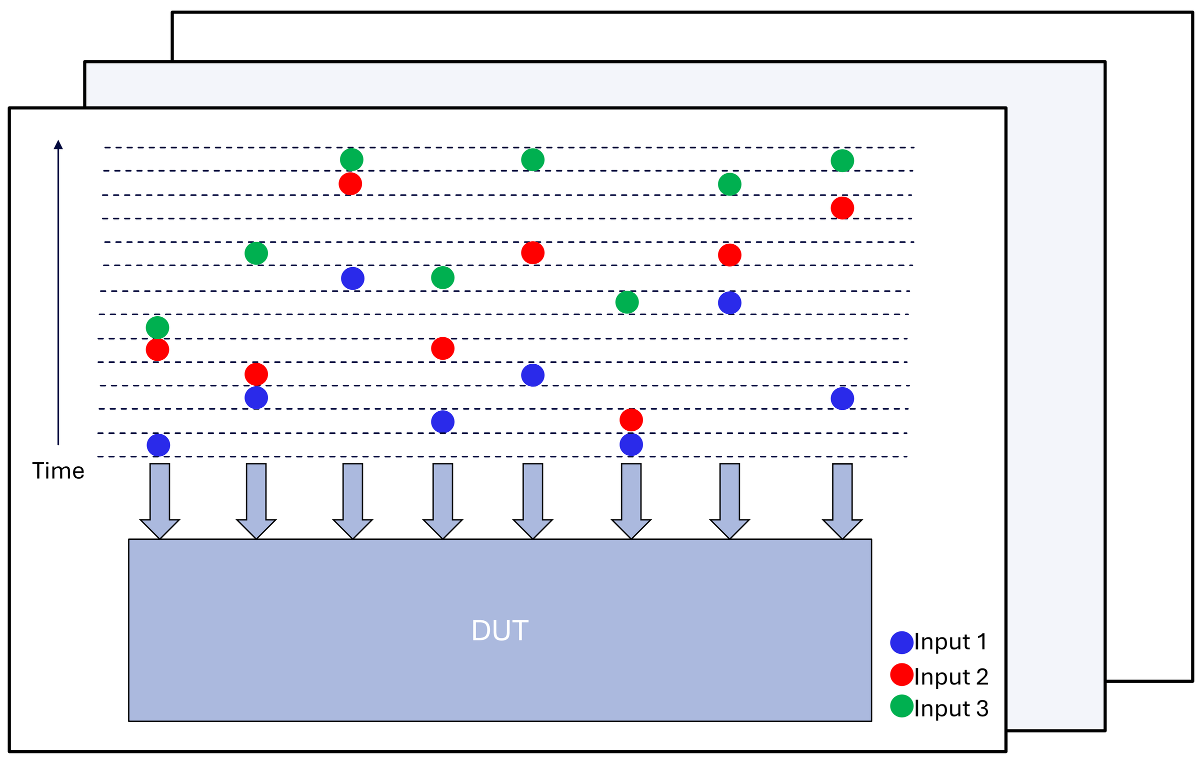
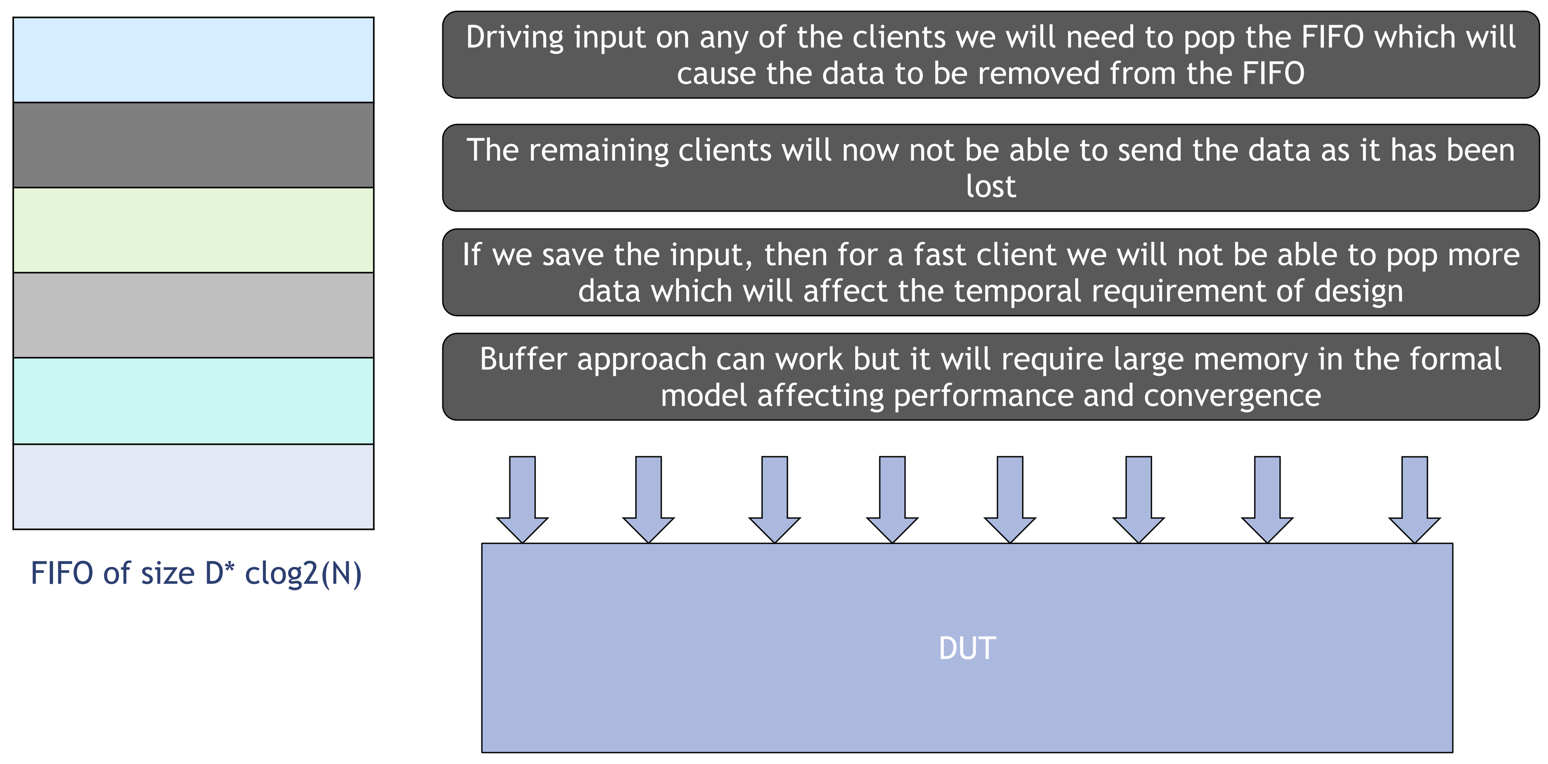
Problem Statement/Introduction



- Design requirement to get exact same sequence of inputs on all N interfaces but they can arrive temporally at different time
- FPV environment is good at randomizing the inputs at the interfaces but here we need to maintain strict ordering of inputs else design will hang
- Regular FIFO based or simple symbolic based inputs will not be useful in constraining the inputs

Why will a FIFO or Buffer-based approach will not work?

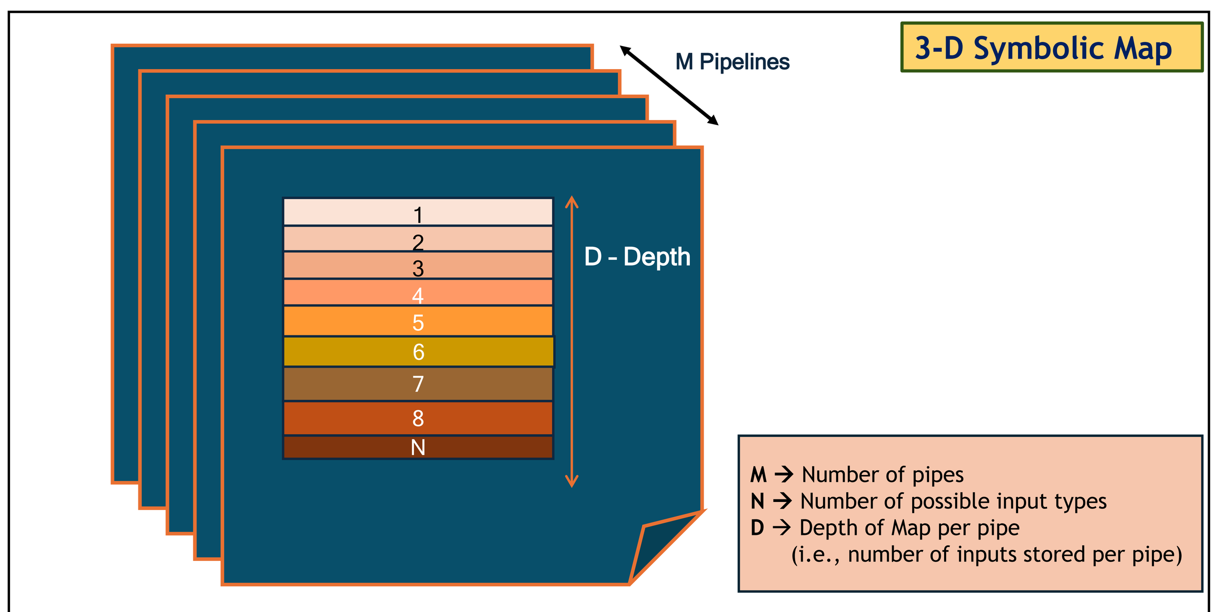


Why not a buffer-based approach?

- Buffer based approach involves addition of a buffer which contains a random sequence of inputs preloaded
- It would have ensured the completeness of the state space but have added a lot of complexity because of the number of flops needed thereby causing convergence issues and affect the performance of the formal testbench

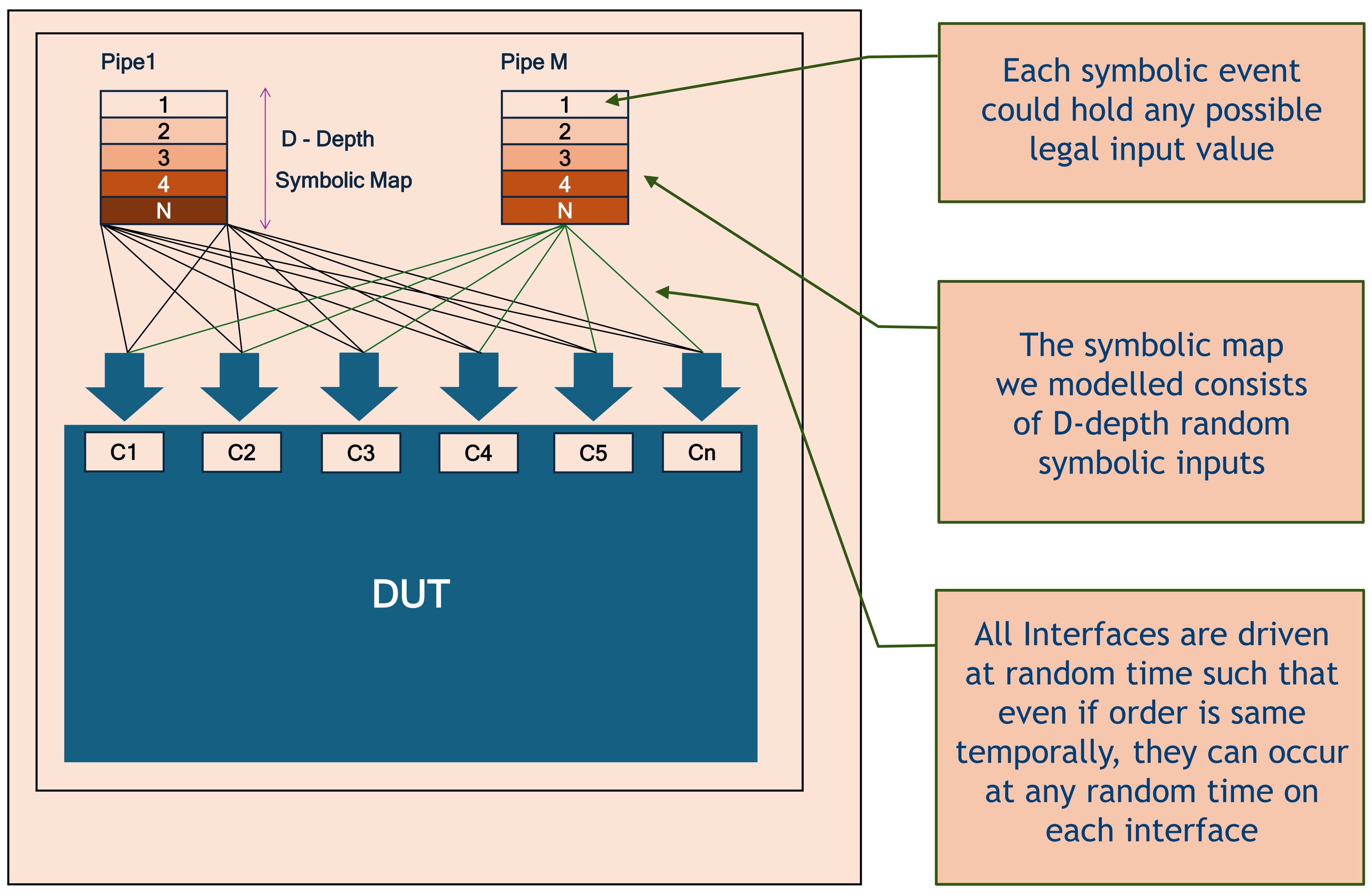
What is a Symbolic Map

- Symbolic Variable is a random constant variable which consist of a random legal values
- Symbolic map in our case is a 3-dimensional array of random constant legal values where
  - N is the number of legal inputs,
  - D represent the total number of outstanding inputs that the design can handle and
  - M represents the parallel streams or pipes of data that need to maintain ordering within the stream but can be random across the streams or pipes



Symbolic Map concept with a **random but stable input tracked across all pipes**

Implementation Details



Results Table

Using this methodology, we were able to verify the following total number of possible combinations of input sequences

Per Pipe, Per Client:

- ❑ Each of the **D** Map slots can hold any of the **N** input types.
- ❑ So, number of combinations per pipe per client: N^D

Per Client (Across M Pipes):

- ➢ Each pipe is independent, so combinations multiply:

  $(N^D)^M = N^{DM}$

- Allowing for temporal randomness allows extensive coverage of these N^{DM} combinations and provides good stress testing of design-under-test
- We ran this methodology on a legacy design which had seen multiple silicon, but we were able to find 2 legacy issues which were due to corner case scenarios

Conclusion & Future Work

- Using this methodology, we increased the coverage of possible combinations tested
- Using the symbolic map, we were able to keep the formal model light and ensure our checks reached the desired depth thereby helping us exercise all possible combinations
- In future we plan to create a reusable plugin and extend this methodology to generalize for N dimensions and allow variable depth across the N dimensions so that this methodology can be used for any case where strict ordering is required

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