Novel and optimized solution to accelerate gate level simulation for complex SOC

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Problem Statement/Introduction

At the forefront of digital design verification, Gate Level Simulation (GLS) is a critical technique in validating design accuracy at the most granular level.

However, the whole process comes with many challenges making GLS a difficult task to complete as detailed below

Challenges :

- Simulation performance and run time
- Debug complexity (initialization and x-propagation)
- Resource requirement(infrastructure and headcount)
- GLS closure within restricted time window

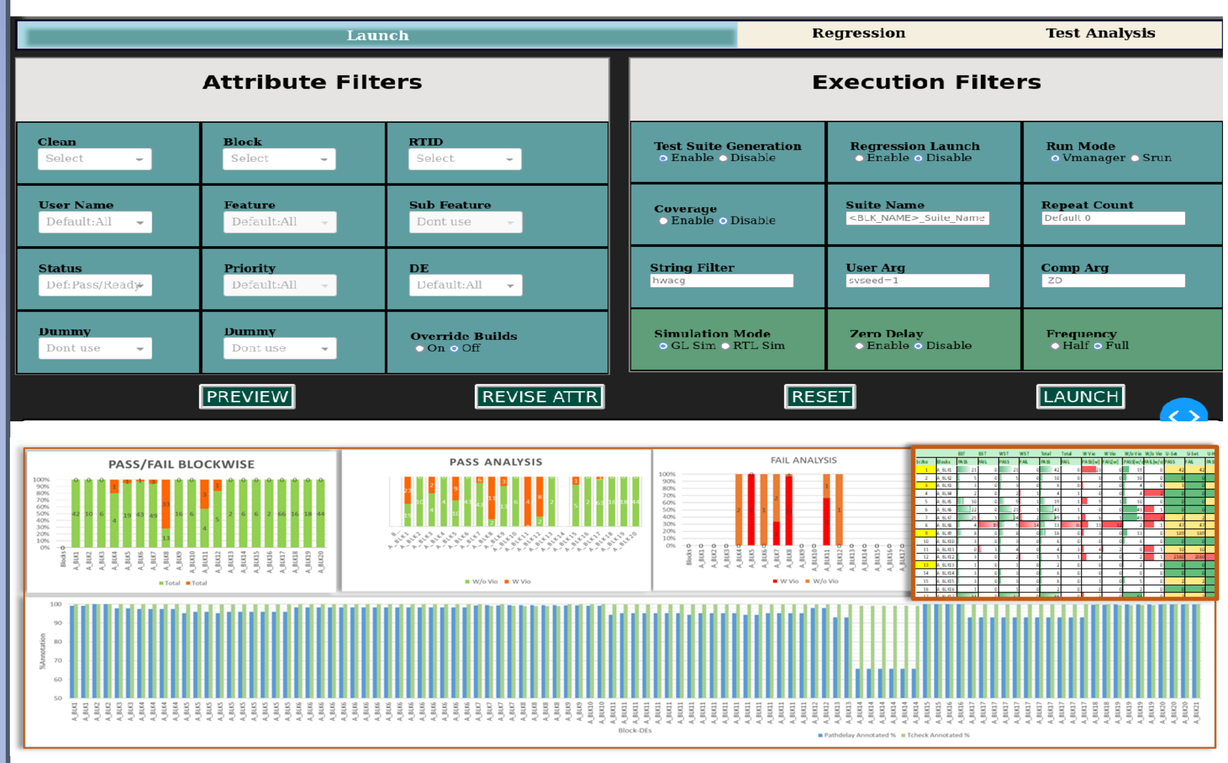
This paper represents methodologies/enhancements leading to optimize and accelerate the GLS closure addressing the above mentioned challenges.

Proposed Methodology/Advantages

Explored methodologies/enhancements:

- Dynamic timing check on/off during simulation – runtime reduction
- Enhanced MSIE flow(Multi Snapshot Incremental Elaboration)-reduction in compilation time and disks pace consumption
- Common save and restore snapshot adoption -expedite GLS simulation and debug complexity reduction
- Minimizing hierarchical reference updates between RTL and GLS-debug complexity reduction
- SDC(Standard Design Constraint) verification using TCV tool – GLS scope reduction
- Zero delay simulation – Early detection of test bench issues and netlist floating ports
- GLS regression automation-Drastic resource reduction(infrastructure and headcount)

Implementation Details/Diagram



Implementation Details/Flow Chart

Dynamic timing check on/off:

- Clean-up boot with timing check on –to ensure clean boot-up without timing violation
- Disable timing checks during boot only for rest of the test vector simulations
- As boot takes maximum time during GLS simulation, disabling timing during boot accelerates the simulation speed
- Achieved 30 % improvement over the normal GLS simulation runs

Save and Restore Methodology:

- Save and restore feature enables to create single/multiple snapshots up to the point of interest (Usually up to boot) which further can be used to run n number of simulations

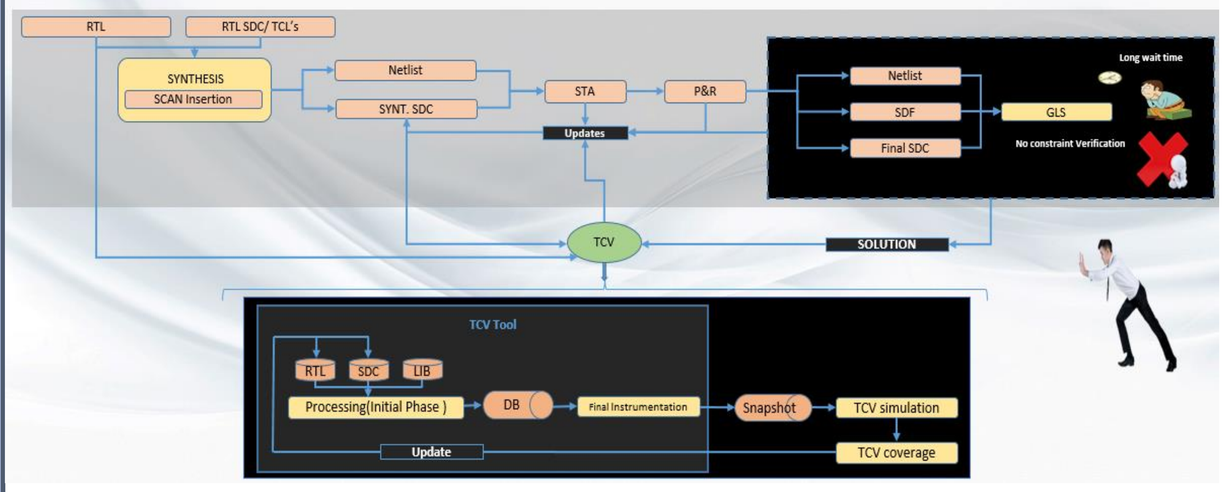
Enhanced MSIE(Multi Snapshot Incremental Elaboration) flow:

- Multi-view (Fake, RTL and Netlist) primary snapshot will be stored in a centralized place which can be used for all simulations
- This methodology saves the overall compile and elaboration time in addition to reduction in disk space consumption as single snapshot is shared across
- Rerun post failure netlist/sdffix as well can be benefitted due to shorter incremental compilation of the changed block only

Implementation Details/Diagram

SDC verification using Time Constrained Verification(TCV) (cadence)tool

- Standard design constraint file represents the timing, clock and other constraints the design has to follow
- GLS simulation is used to validate these timing constraints e.g. MCP(Multi cycle path) , False path
- Pre-qualifying these constraints in RTL simulation leads to reduced GLS vector selection



Resulat & Conclusion

RESULTS:

SNR	Run Time(Hrs)
Yes	00:08:40
No	05:07:19
Run Time Reduction by 97%	

Table-1

Dynamic Tcheck	Run Time(Hrs)
Yes	18:47:09
No	27:34:54
Run Time Reduction by 32%	

Table-2

Disk Space	Usage(TBytes)
Yes	60
No	34.2
Usage Enhancement 43%	

Table-3

Human Resource	Head Count
Yes	42
No	18
HC reduction 58%	

Table-4

The optimizations depicted in this presentation represent the below advantages

- Reduction of resource involvement in GLS simulation
- GUI based GLS regression flow
- Disk space reduction by 43% and Human resource reduction by 58%
- Reduction in simulation run time (TCV , ZD , Hybrid & Fullnet simulation)
- Dynamic timing check on/Off -Results in 32% run time improvement
- Enhanced MSIE flow
  Eliminates the need of compilation and elaboration [72.5% improvement]
  Reduction in disk space consumption [37%]
- Common Save and restore snapshot
- Simulation run time improvement by [87 %]
- Timing Constraint Verification(TCV) implementation
- First time GLS pass % improvement [60%]

REFERENCES

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[3] Singh Gagandeep , Gate-Level Simulation Methodology

[4] Cadence, *Save Restart and Dynamic Test Flows in UVM*