Advancing Early Enablement, Validation, and Signoff of Manageability IP for Seamless dGPU-Server Paring

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Problem Statement/Introduction

During early phase of dGPU, AIC or other PCIe based cards development, especially when those cards are mainly targeted to be paired with server integration, validation of Add-In-Management Card along with the SOC is the key for the product success. To note, server requires manageability feature for it's cards getting plugged in for seamless access of Telemetry/Manageability data.

This requires several HW/SW components, such as proper server drivers, AMC-BMC connection, necessary FWs to be ready at a very early stage to commence a full- fledged validation. This approach is generally not feasible as it requires all HW/SW components to be mature and ready and ends up in chicken-n-egg problem.

Hence to support early validation of these features when the FW/driver components are not ready, there was a need to develop a mechanism which can work with bare minimum dependencies and can help in debug critical issues thereby helping SoC, SW and boards team to left shift their development.

Proposed Methodology/Advantages

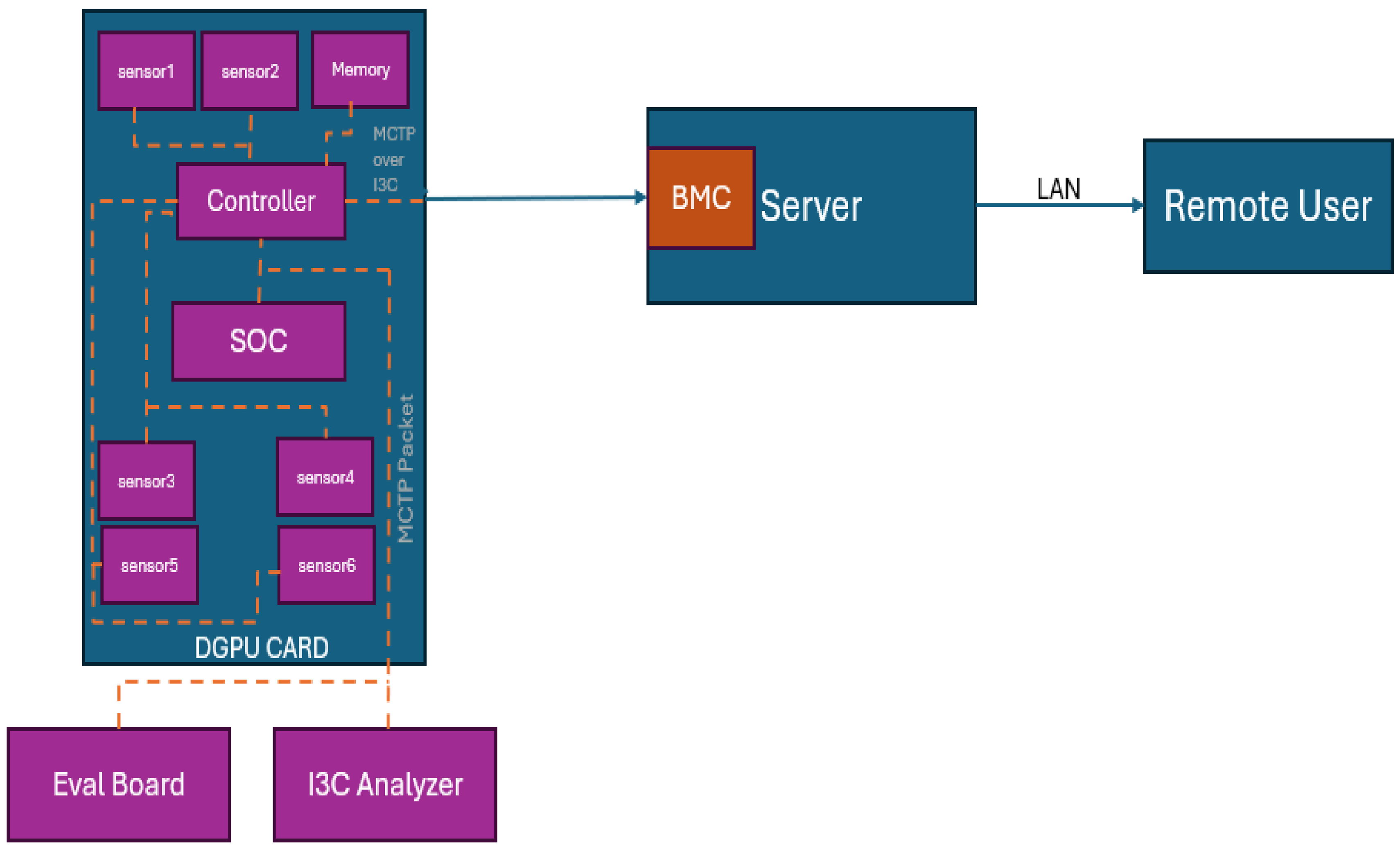
To support early enablement and validation of dGPU Telemetry with server, we developed a robust mechanism using exercisers to execute MCTP transactions and access telemetry data for dGPU SoC.

Two distinct exercisers were employed: an I3C exerciser configured in master and slave modes for encoding MCTP protocol packets, and an evaluation board equipped with the same chipset intended for customer, connected to a validation card with firmware mimicking MCTP transactions.

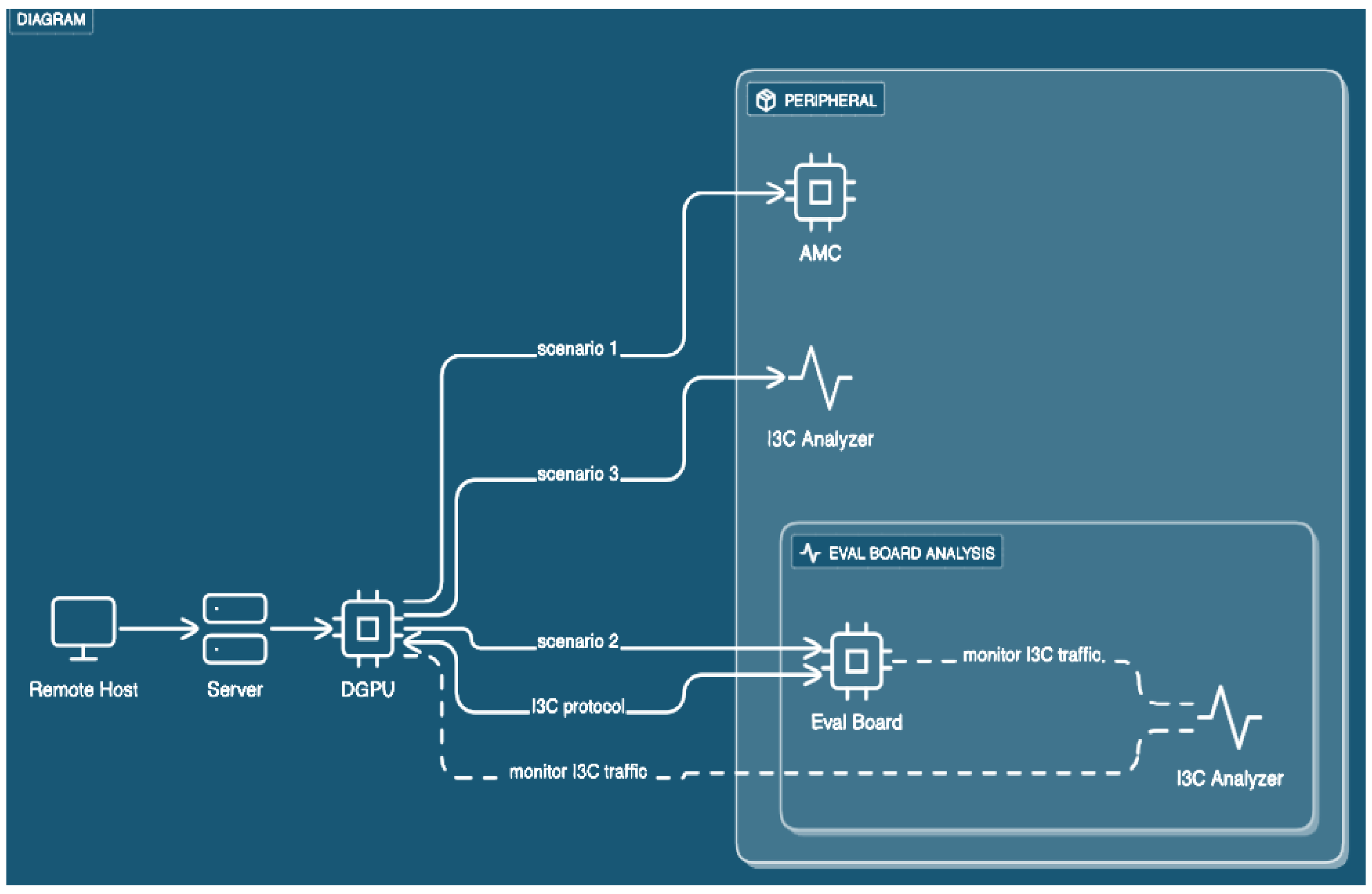
Platform Monitoring Telemetry (PMT) and Platform Environment Control Interface (PECI) payloads within Vendor-Defined Messages (VDM), the data acquisition process is streamlined, enhancing operational efficiency and reducing reliance on driver-based methods.

Utilizing the Exerciser as the master device and the graphics card as the slave, MCTP vendor-defined formats are employed to capture telemetry data, providing a robust framework for managing dGPU resources in server environments.

Implementation Details/Diagram



Implementation Details/Flow Chart



Results Table

During the planning phase of dGPU validation, early requirements called for the exposure of I3C master headers to facilitate MCTP transactions. Initially, these headers were connected to an exerciser that transmitted synthetic MCTP payloads to access telemetry data.

After integrating feedback and resolving dGPU firmware bugs, the exerciser was replaced with a more advanced evaluation board. This board was equipped with the same firmware as the manageability card, accurately replicating the customer scenario.

This work helped in finding 3 critical bugs. Using MCTP VDM packets along with exerciser helped in debugging several other FW issues. The usage of evaluation board with exact same chipset as of customer, helped in early stage customer enablement.

Overall, this approach facilitated the early development of manageability and dGPU firmware, informed reference board designs, and exposed several bugs and limitations.

Conclusion

01 The implementation of MCTP over I3C represents a significant advancement in server manageability, particularly in environments utilizing dGPUs.

02 By addressing the challenges of integrating dGPUs with servers and providing a robust framework for telemetry data acquisition, this work contributes significantly to the development of high-performance computing solutions, particularly for PCIe-based discrete GPUs, AICs, and other PCIe-based cards.

03 This work lays the groundwork for scalable, out-of-band manageability solutions resilient to platform topology changes and late-binding device configurations. Future research will aim to optimize MCTP transaction throughput validation, Validation of advanced telemetry classes, and security protocols like Security Protocol and Data Model (SPDM).

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